G.10 Vol. II

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Advanced TIROS-N Program

NOAA-KLM System Design Report (SDR)

Vol. 2

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Preface

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4.7 COMMUNICATIONS SUBSYSTEM

The Communications Subsystem is depicted in Figure 4.7-l and is comprised of the components listed in Table 4.7-l. The subsystem has two sets of communications links (ascent and operational) which are summarized in Figures 4.7-2 and 4.7-3 and Tables 4.7-2 and 4.7-3, respectively. The following summary describes the relationship of the above described equipment to the communications links:

- S-Band Transmitting Equipment - Three directional S-Band Antennae (SBA-1, -2, and -3), and three S-Band Transmitters (STX-1, -2, and -3) provide the routine S-Band down-link services in operational orbit. These downlink services consist of HRPT, GAC playback, TIP playback, and LAC playback data as listed in Table 4.7-3. SBA-1 and STX-1 transmit the lowest of the three frequencies, while SBA-3 and STX-3 transmit the highest.

- S-Band Omni Antennae (SOA-1, -2) and STX-2 provide real-time telemetry to the NOAA-CDA stations if required postlaunch.

- S-Band Onmi Antennae (SOA-3, -4) and STX-4 provide launch real-time telemetry to the NASA tracking station at WTR, to the ARIA aircraft and to the Air Force Satellite Control Facility (SCF).

- Either S-Band link, the NOAA-CDA compatible or the Air Force SCF compatible, can be operated in any spacecraft emergency in either boost or orbit mode.

- Command Receiving Equipment - S-Band Omni Antennae (SOA-5, -6), RF Hybrid (RFH), GRD Filter Network (GFN) and G-STDN Receiver/Demodulator (GRD) provide all command reception.

- VHF Telemetry Equipment - The BDA, RF Filter (RFF-1), and Beacon Transmitter (BTX-1 or BTX-2) provide the TIP real-time data listed in Tables 4.7-2 and 4.7-3.

- The directional VHF Real-Time Antenna (VRA), RF Filter (RFF-1), and VHF Real-Time Transmitter (VTX-1 or -2) provide the APT data in Table 4.7-3.

- Antennae and RF Filters for Payload Instruments - The directional UHF Data Collection System Antenna (UDA), Data Collection System/Search and Rescue Processor Diplexer (DPD), and RF Filter (RFF-2) provide the antenna and electromagnetic interference (EMI) isolation for the government-furnished Data Collection System (DCS) listed in Table 4.7-3.

  The UDA, DPD, and Filter RFF-3 provide the corresponding service for the government-furnished Search and Rescue Processor (SARP-M).

  The directional Search and Rescue Receiving Antenna (SRA), the directional Search and Rescue L-Band Antenna (SLA), and RF Filters RFF-3, -4, and -5 provide the corresponding services for the government-furnished Search and Rescue Repeater (SARR).

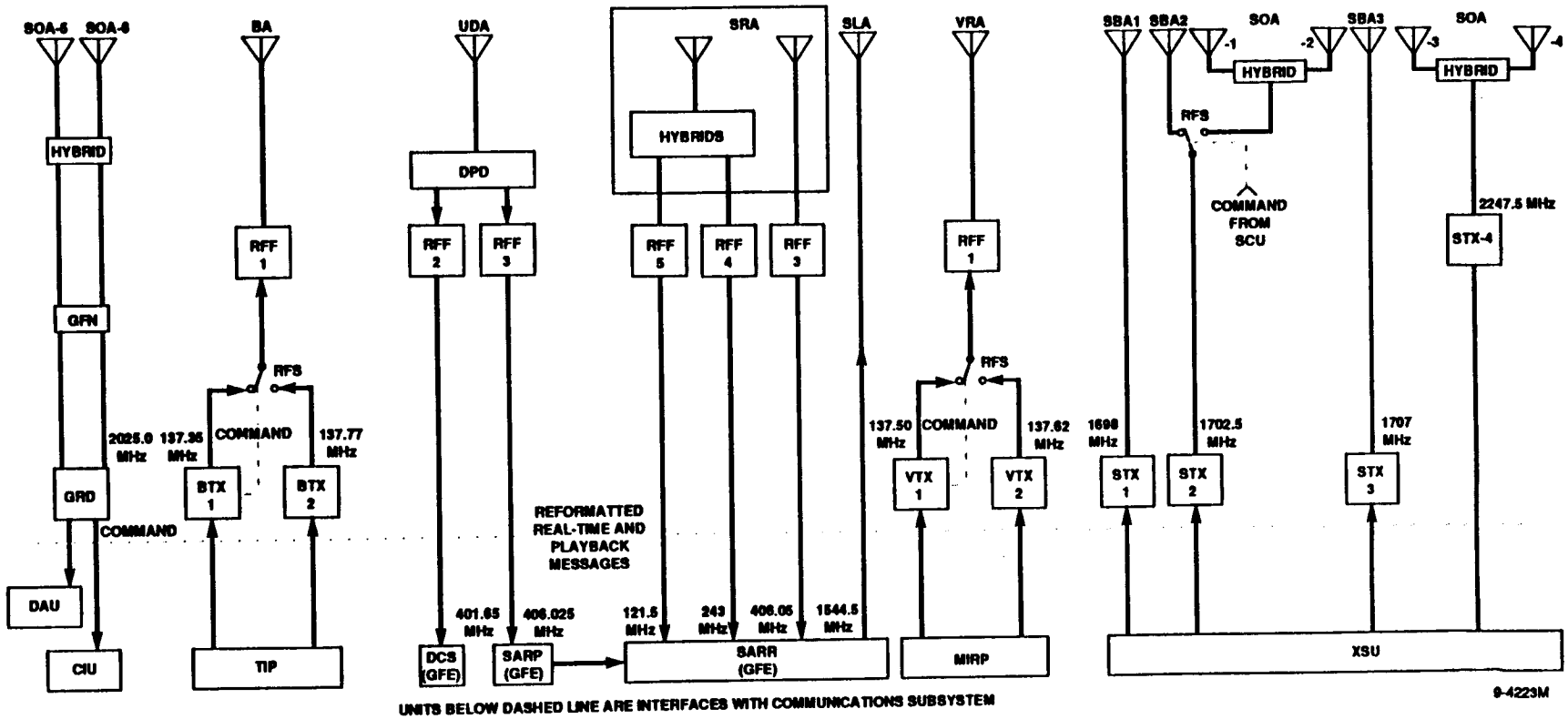


Figure 4.7-1. Communication Subsystem Block Diagram

TABLE 4.7-1, COMMUNICATIONS SUBSYSTEM COMPONENTS

Number Required	Name	Performance Specification	Source
1	VHF Beacon Antenna (BDA)	PS-2280284	ASD
2	Command Receiver/Demodulator (GRD)	PS-2629937	Loral
1	(VHF Beacon) RF Filter (RFF-1)	PS-2629708-l	Wavecom
1	(VHF Beacon) RF Switch (RFS)	3261703	Transco
2	VHF Beacon Transmitter (BTX)	PS-2629724	Loral
1	VHF Real-Time Antenna (VRA)	PS-2280287	ASD
1	(VHF Real-Time) RF Filter (RFF-1)	PS-2629708-l	Wavecom
1	(VHF Real-Time) RF Switch (RFS)	3261703	Transco
2	VHF Real-Time Transmitter (VTX)	PS-2629726	Loral
3	S-Band Antenna (SBA)	PS-2280286	ASD
1	(S-Band) RF Switch (RFS)	3261703	Transco
4	S-Band Transmitter (STX)	PS-3265453	ASD
1	UHF Data Collection System Antenna (UDA)	j-2280285	ASD
1	(UHF DCS) RF Filter (RFF-2)	PS-2629708-2	Wavecom
1	(SARP-M) RF Filter (RFF-3)	PS-2629708-3	Wavecom
1	DCS/SARP-M Diplexer (DPD)	2298020	Wavecom
1	SARR L-Band Antenna (SLA)	PS-2297967	ASD
1	(SARR 406 MHz) RF Filter (RFF-3)	PS-2629708 3	Wavecom
1	(SARR 243 MHz) RF Filter (RFF-4)	PS-2629708-4	Wavecom
1	(SARR 121.5 MHz) RF Filter (RFF-5)	PS-2629708-5	Wavecom
1	SARR Receiving Antenna (SRA)	PS-2297743	ASD
2	S-Band Omni Antennae (SOA-1, -2)	H-2288274	ASD
2	S-Band Omni Antennae (SOA-3, -4)	PS-2628492	ASD
2	S-Band Omni Antennae (SOA-5, -6)	PS-3284970	ASD

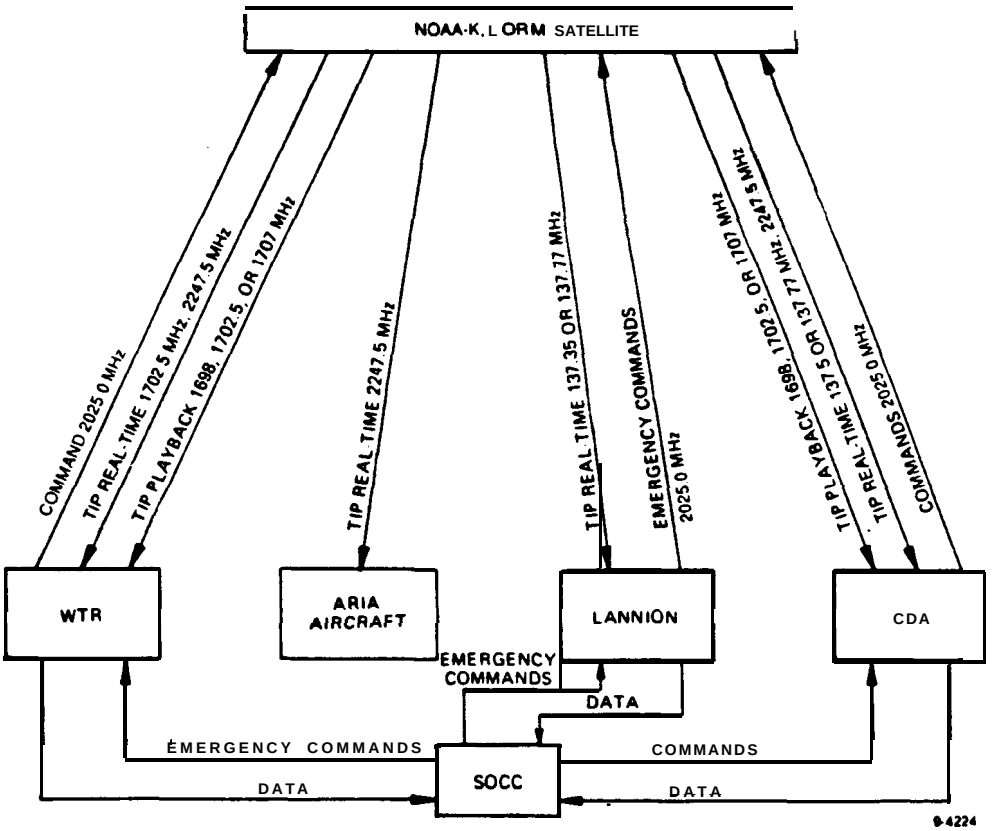


Figure 4.7-2. Ascent and Early-Orbit RF Communications Link Summary

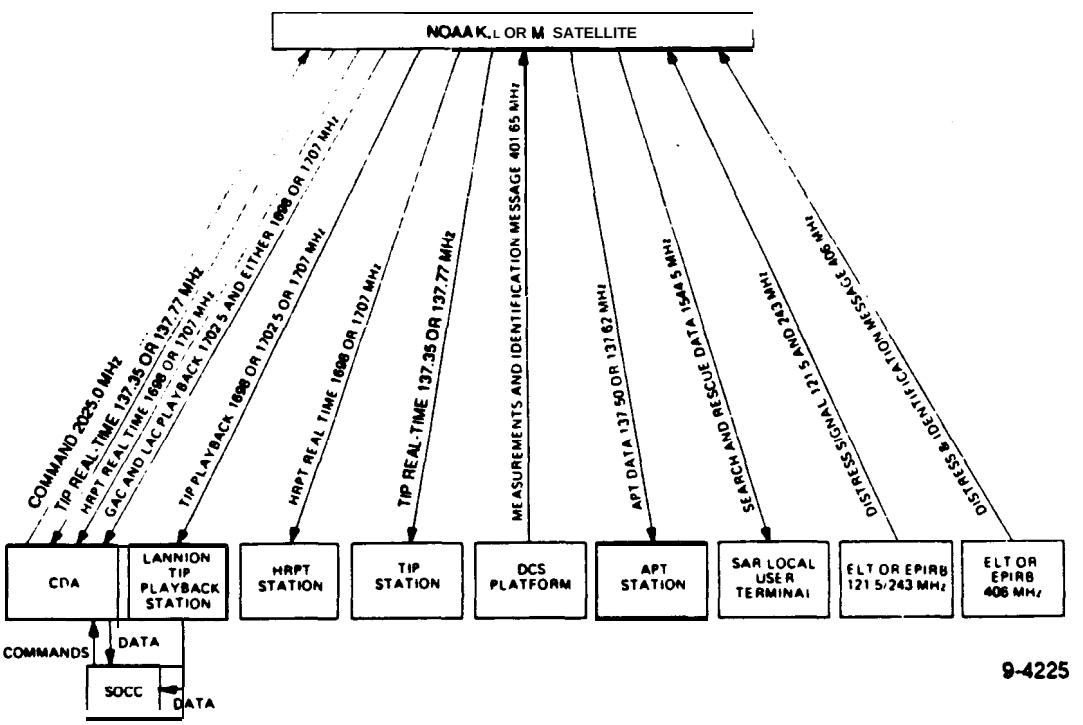


Figure 4.7-3. Operational RF Communications Link Summary

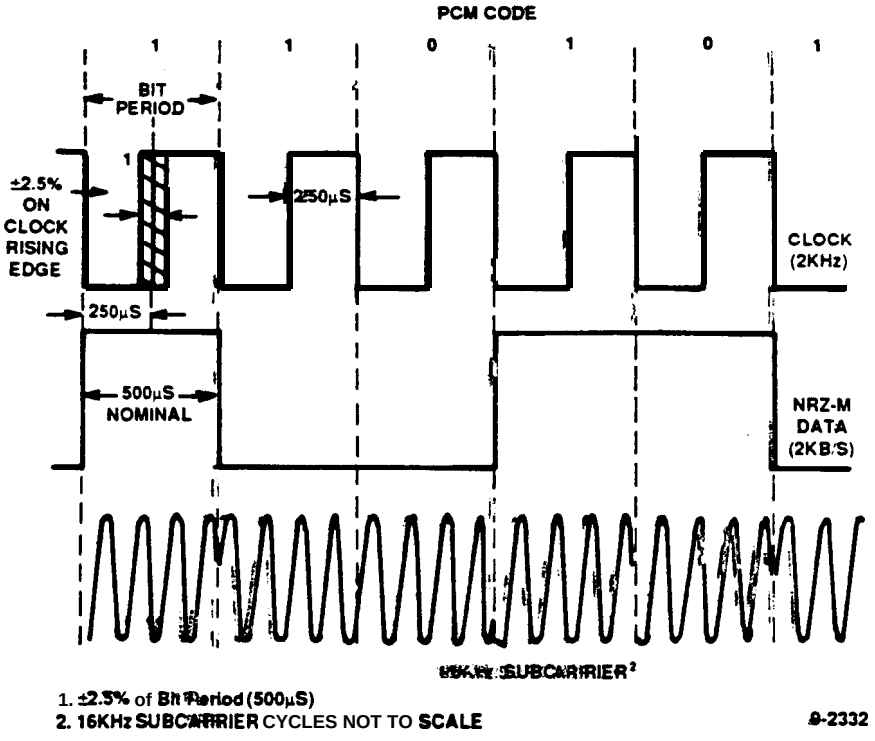


Figure 4.7-4. Command Data Wave E orm

The subsequent sections describe the performance of the Communications Subsystern in the two sets of communications links,

4.7.1 COMMUNICATIONS LINKS

4.7.1.1 Ascent and Early-Orbit Links

4.7.1.1.1 General Communications Requirements

During the Titan launch, the tasks of the Communications Subsystem begin on the launch pad at satellite turn-on and end when NASA/NOAA releases the early-orbit support stations from their support (normally one day after launch). It is anticipated that the French government station at Lannion, France, will provide such support. In addition, NASA may opt to extend support by the Advanced TIROS-N Aerospace Ground Equipment (ATNAGE II) and the NASA tracking station at the WTR from their coverage of powered flight and the first WTR pass, to include additional early orbits. The following discussion assumes ATNAGE II/WTR support will end after the first WTR pass.

The prelaunch communications requirements are to provide command and real-time TIP telemetry links to the ATNAGE II.

The powered flight and coast requirements are to provide real-time TIP data to the NASA station at WTR and to the ARIA aircraft.

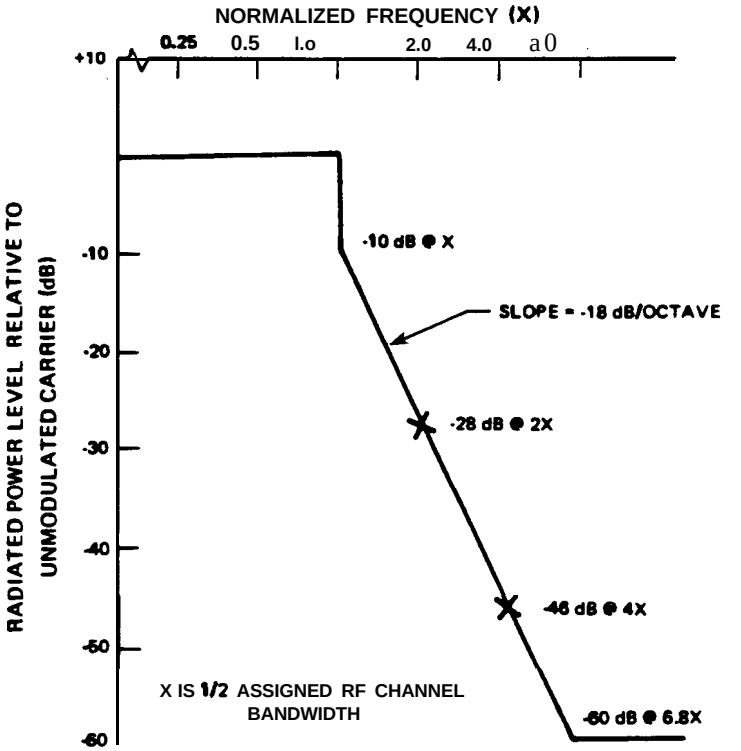
TABLE 4.7-2. ASCENT AND EARLY-ORBIT COMMUNICATIONS LINK CHARACTERISTICS SUMMARY

Link	Ground Facility	Frequency	Modulation	Bit Rate	EIRP at Satellite Value	Coverage Measurement Polarization	Region Centered at the satellite	Satellite Polarization	Spectrum Control Characteristics
S-Band Command	NAGE (pre-launch), CDA Lannion (emergency)	2025.0 MHz	BPSK (NRZ-M) (Figure 4.7-4)	2 kbps	-79 dBm (from CDA)	RCP	Direction of line-of-sight to the Ground Facility	RCP	Not Applicable
S-Band TIP Real-Time	NOAA-CDA Station	1702.5 MHz	PSK, Split-Phase Level Data	8320 bps or 16,640 bps	+26 dBm	RCP/LCP diversity	93% of Sphere	RCP (+X) LCP (-X)	Figure 4.7-5
	Air Force SCF	2247.5 MHz	Phase modulated bi-phase	Same as above	+24 dBm	RCP	95% of Sphere	RCP (+X, -X)	Figure 4.7-5
S-Band TIP Playback	WTR, CDA	1702.5 MHz	Same as above	332.7 kbps	+37 dBm	RCP/LCP diversity	63° Half-angle Cone About +X Axis	LCP.	Figure 4.7-5
VHF TIP Real-Time	CDA, Lannion	137.35 or 137.77 MHz	Same as above	8320 bps	+9.5 dBm	RCP	90% of Sphere	Linear	Figure 4.7-5

TABLE 4.7-3. OPERATIONAL LINK SUMMARY

Link	Data Contents	Ground Facility	Frequency	Modulation
S-Band Command	Satellite commands	CDA	2025.0 MHz	BPSK, NRZ-M (Figure 4.7-4)
VHF TIP Real-Time	Housekeeping telemetry and payload data from all meteorological instruments except AVHRR	CDA, TIP Stations	137.35 or 137.77 MHz	PSK, Split-Phase-Level Data
HRPT	Full-resolution AVHRR data plus concurrent TIP data	CDA, HRPT Stations	1698 or 1707 MHz	Same as above
GAC Playback LAC Playback	Global reduced-resolution AVHRR data plus TIP data stored on satellite tape recorders Tape-recorded-replica of HRPT data	CDA	1702.5 MHz and either 1698 or 1707 MHz	Same as above or PSK, NRZ-Level Data
TIP Playback	Tape-recorded-replica of TIP real-time data	Lannion, TIP Playback Station	1698 or 1702.5 or 1707 MHz	PSK, Split-Phase-Level Data
APT	Reduced-resolution, geometrically-corrected analog video from two of the five AVHRR channels, selected by command	CDA, APT Stations	137.50 or 137.62 MHz	AM/FM Analog Data
DCS Uplink Messages*	Environmental measurements, identification, and a frequency reference for Doppler navigation; from unattended platforms	DCS Platforms	401.65 MHz	PSK, Split-Phase-Level Data (Figure 4.7-6) (Table 4.7-4)
SAR 121.5 MHz Uplink Signals, 243 MHz Uplink Signals*	Frequency reference for Doppler navigation from downed aircraft and buoys launched from sunken ships. Aircraft instruments are Emergency Locator Transmitters (ELT's); buoy instruments are Emergency Position Indicating Radio Beacons (EPIRB's)	121.5/243 MHz ELT's and EPIRB's	121.5 MHz ±6 kHz 243 MHz ±12 kHz	AM (Figures 4.7-7 and 4.7-8) (Table 4.7-5)
SAR 406 MHz Uplink Messages Received Separately by SARR 406 MHz Channel and by SARP-M*	Same as above but, with improved frequency stability, and modulation containing identification of the aircraft or ship	406 MHz ELT's and EPIRB's	406.05 MHz ±80 kHz	PSK, Split-Phase-Level Data (Figures 4.7-9 and 4.7-10) (Table 4.7-5)
SARR Downlink*	Transponded frequency-multiplexed SAR uplink signals and messages from all three uplink frequencies, preserving uplink phase for Doppler tracking by ground stations; also 406 MHz messages reformatted and tagged with time and Doppler measurements by the SARP-M; the SARP-M data transmitted in near-real-time and also cyclically from SARM.	SAR Local User Terminals	1544.5 MHz	PM (Figure 4.7-11) (Table 4.7-6)

*DCS, SARP-M and SARR characteristics are in the form of antenna gain referred to DCS, SARR, and SARP-M RF ports.



SERVICE	X (kHz)
S-BAND	3500 kHz
APT	25 kHz
VHF TIP	30 kHz

NOTES:

- 1660-1670 MHz AND 1720-1721 MHz RADIO ASTRONOMY BANDS: LESS THAN -236 dBW/m^{2}Hz - TRANSLATES TO -72 dBW/3 kHz EIRP AT THE SATELLITE.
- 1664.3-1664.7 MHz SMS/GOES BAND: LESS THAN 1 dB DEGRADATION TRANSLATES TO LESS THAN -30 dBW/3 kHz EIRP AT THE SATELLITE.

6-0403

Figure 4.7-5. Spectrum Control Characteristics (S-Band, APT, and VHF TIP)

The early-orbit requirements are as follows:

- Recovery of recorded TIP telemetry by playback of the satellite tape recorders.
- Provide continuous real-time telemetry limited only by ground station contacts.
- Provide limited command capability only by ground station contacts.
- Provide the playback capability in operational orientation, with +X axis directed at the nadir.
- Provide the command and real-time data capabilities in any satellite attitude.

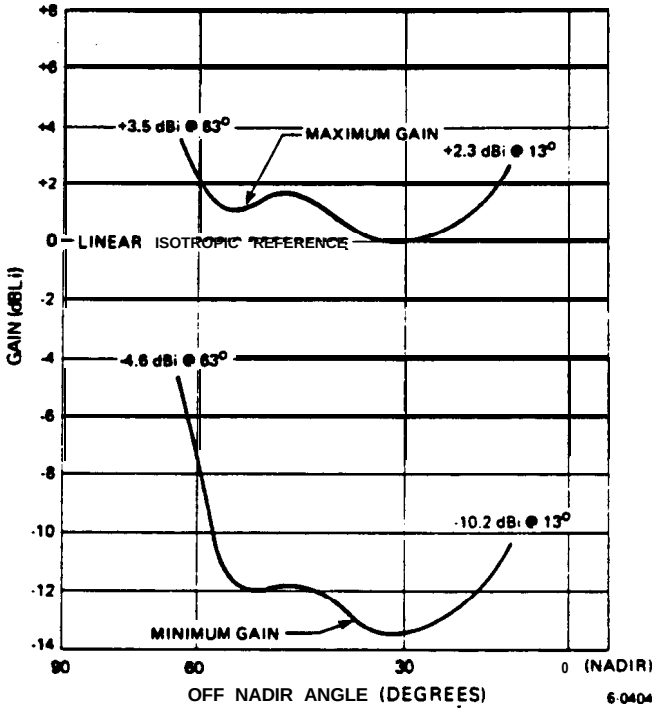


Figure 4.7-6. Net Gain at DCS Receiver RF Interface Connector

TABLE 4.7-4. MAXIMUM EM1 LEVEL INTO THE DCS RF INTERFACE CONNECTOR

Frequency (MHz)	Maximum Signal (dBm)
10 to 370	-20*
370 to 396	-60
396 to 401.61	-125
401.61 to 406.69	-145
401.69 to 406.0	-125
406 to 430	-60*
430 to 1000	-20
1000 to 10,000	0

*In addition, the signal shall not exceed -60 dBm at the following discrete frequencies:

31.080 MHz
339.488 MHz
406.796 MHz

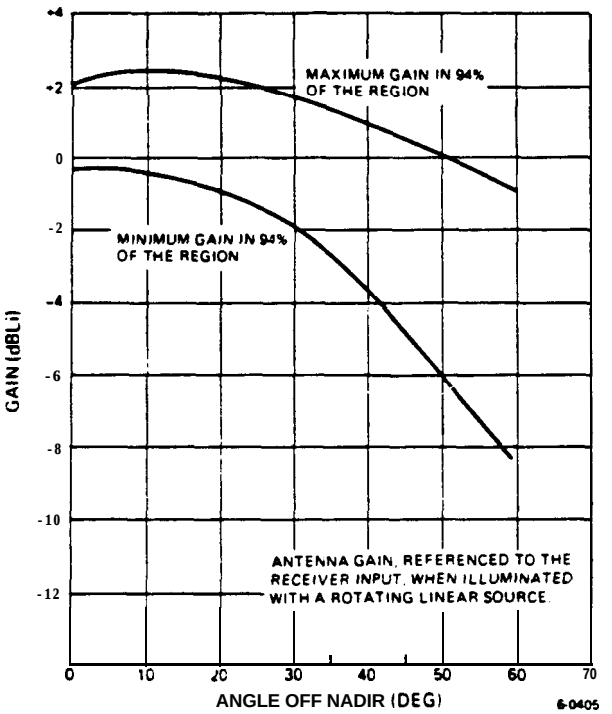


Figure 4.7-7. Net Gain at SARR 121.5-MHz Receiver RF Interface Connector

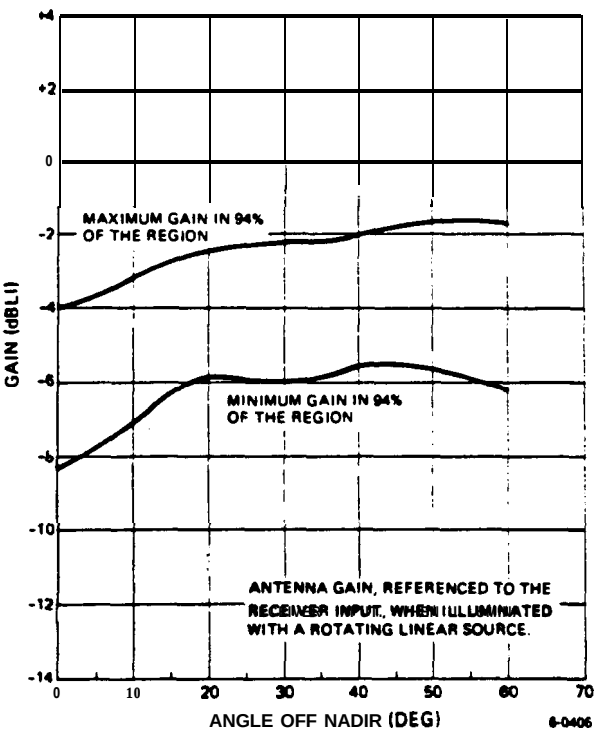


Figure 4.7-8. Net Gain at SARR 243-MHz Receiver RF Interface Connector

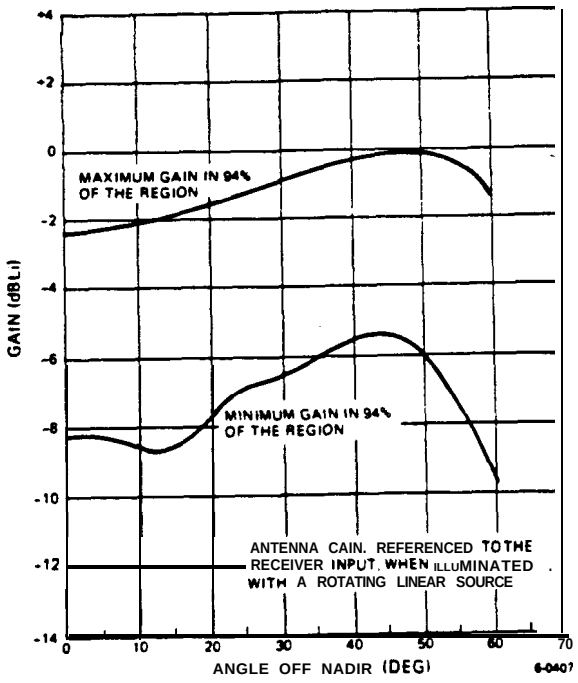


Figure 4.7-9. Net Gain at SARR 406.05 MHz RF Interface Connector

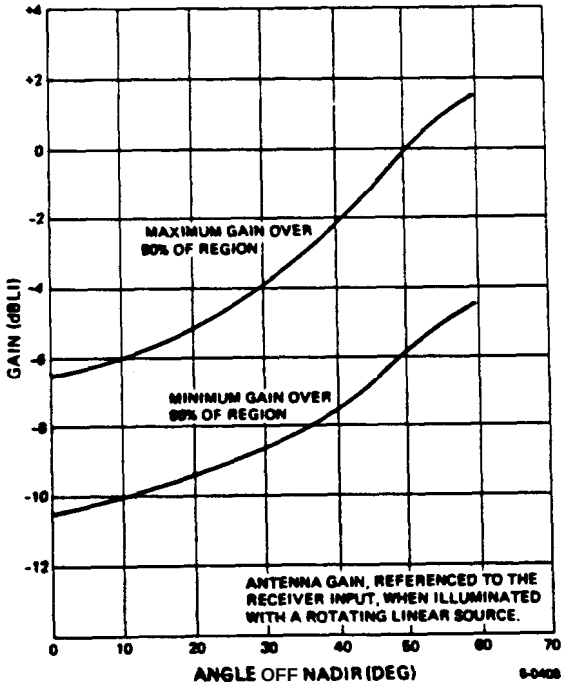


Figure 4.7-10. Net Gain at SARP-M Receiver RF Interface Connector

TABLE 4.7-5. MAXIMUM SATELLITE TRANSMITTER POWER LEVELS INTO THE SARP-M AND SARR RECEIVER RF INTERFACE CONNECTORS

Center Frequency	Frequency Band (MHz)	Limit Maximum (dBm)
SARR 243 MHz	1 to 15	0
	15 to 228	-20
	228 to 236	-60
	236 to 240	-100
	240 to 242.925	-125
	242.925 to 243.075	-145
	243.075 to 246	-125
	246 to 250	-100
	250 to 258	-60
	258 to 1000	-20
	1000 to 10000	0
SARR 121.5 MHZ	1 to 15	0
	15 to 114	-20
	114 to 118	-60
	118 to 120	-100
	120 to 121.45	-125
	121.45 to 121.55	-145
	121.55 to 123	-125
	123 to 125	-100
	125 to 129	-60
	129 to 1000	-20
	1000 to 10000	0
SARR 406.050 MHz	1 to 15	0
	15 to 375	-20
	375 to 385	-60
	385 to 401	-100
	401 to 405.9	-125
	405.9 to 406.2	-145
	406.2 to 411	-125
	411 to 425	-100
	425 to 435	-60
	435 to 1000	-20
	1000 to 10000	0
SARP-M 406.025 MHz	1 to 15	0
	15 to 375	-20*
	375 to 385	-60
	385 to 401	-100
	401 to 405.985	-125
	405.985 to 406.065	-145
	406.065 to 411	-125
	411 to 425	-100
	425 to 435	-60
	435 to 1000	-20
	1000 to 10000	0

*The signal level at the SARP/receiver input terminals shall not exceed -60 dBm at the following frequencies:

343.211 MHz ±0.5 kHz
400.846 MHz ±0.5 kHz
411.253 MHz ±0.5 kHz

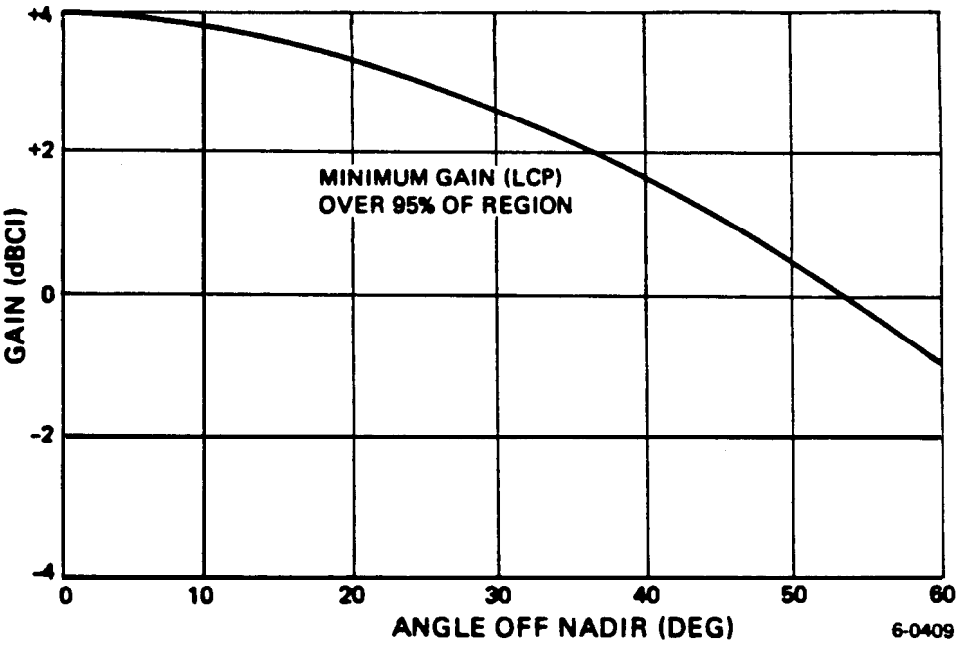


Figure 4.7-11. Antenna Gain for 10-Watt 1544.5-MHz Transmitter at SARR Interface Connector

TABLE 4.7-6. MAXIMUM LEVELS OUT OF THE SARR TRANSMITTER RF INTERFACE CONNECTOR*

Band	Frequent y	Maximum Permissible Conducted Level Out of SAR Repeater
ATN Command	148 to 154 MHz	-85 dBm/40 kHz (1)
DCS	394 to 406 MHz	-105 dBm/40 kHz (1)
SAR, 121.5 MHz	121.5 ±1 MHz	-105 dBm/40 kHz (1)
SAR, 243 MHz	243 ±2 MHz	-105 dBm/40 kHz (1)
SAR, 006 MHz	406 ±5 MHz	-105 dBm/40 kHz (1)
GOES	1694.3 to 1694.7 MHz	-82 dBm/Hz (2)
Radio Astronomy	1660 to 1670 MHz and 1720 to 1721 MHz	-82 dBm/Hz (2)
ATN Transmitter Spec - following IRIG Telemetry Standard Document 106	10 kHz to 10 GHz	-30 dBm/1 MHz (2)
ATN Transmitter Spec - Compatibility with STDN S-Band Command	2020 to 2120 MHz	-40 dBm/1 MHz (2)

(1) Discrete spurs. Measure in indicated bandwidth.
(2) Power level is total power measured in indicated bandwidth.

- This is a requirement on the GFE SARR.

4.7.1.1.2 Early-Orbit Ground Station Contacts

The contact times available to the system are shown in Figure 4.7.1-1. This illustration shows the loci of 5-degree elevation angles from the ground stations, and plots time from ascending node versus longitude of ascending node. The maximum time shown is one orbital period. The ground stations shown are the same three that will operate the satellite throughout its life: the Command and Data Acquisition (CDA) stations at Wallops Island, Va., and Fairbanks, Alaska; and the French government station at Lannion, France. In the illustration, the satellite track is vertical from the bottom to the top, reappearing at the bottom displaced to the left by the earth's rotation in one satellite orbit period, approximately 23 degrees.

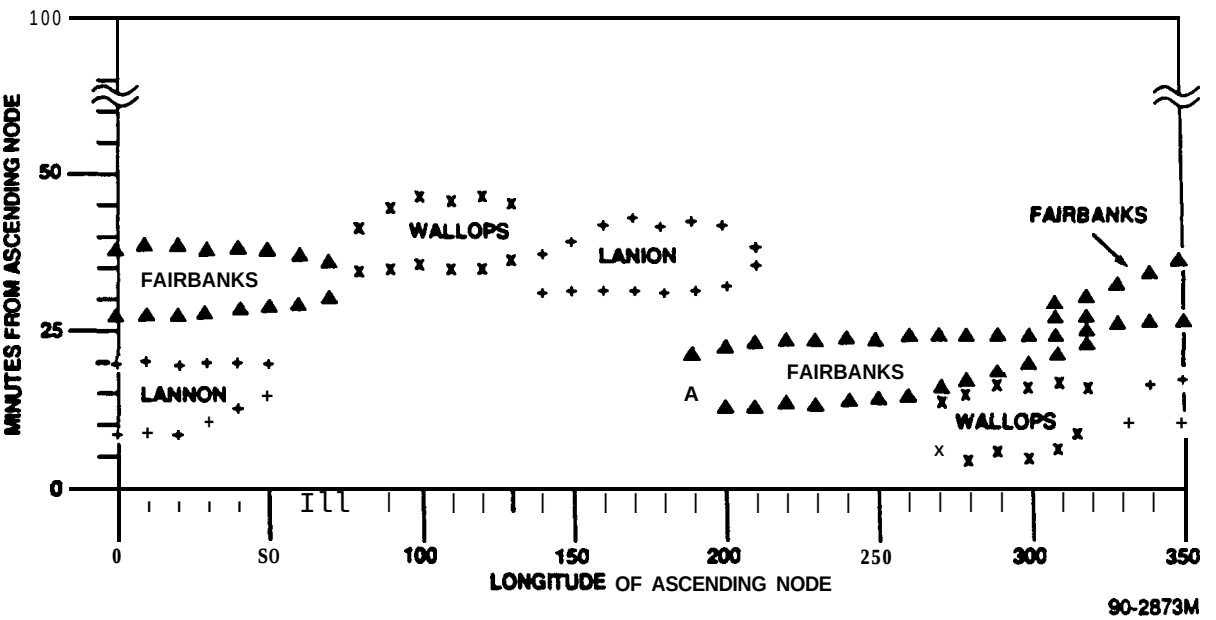


Figure 4.7.1-l. Ground Station Contact in 450-nmi Orbit

The contact time available in a particular orbit is the time difference between entry into and exit from one of the contours shown. An orbit whose vertical motion intersects none of the contours is "blind" to the system; none of the stations will contact the satellite in that orbital period. Study of the illustration shows the following:

- Contact times are up to 12 minutes long.
- Approximately 5% of the orbits are blind.
- Approximately 25% of the orbits are blind to the CDA stations.

4.7.1.1.3 Ascent and Early Orbit Operations

On the launch stand, the BTX, STX, and Command links are all closed with the ATNAGE II, as part of final checkout. The RF paths connecting the satellite with the ATNAGE II consist of radiation through RF windows in the ascent shroud and the NASA antennas, amplifiers, and transmitters as shown in Figure 4.7.1-2.

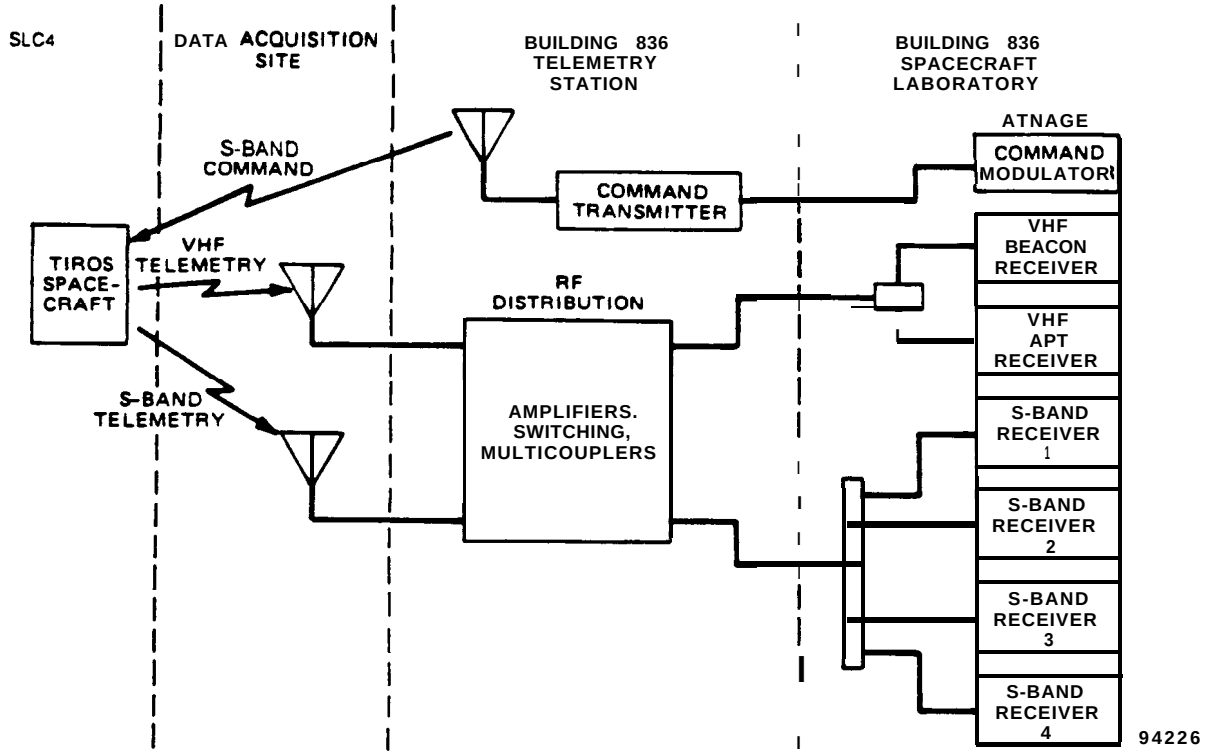


Figure 4.7.1-2. RF Paths Between the Satellite and the ATNAGE II at WTR

During ascent, the satellite transmits TIP real-time data at the 16,640-bps boost rate, via STX-4 and SOA-3, -4, to the ATNAGE II and to ARIA aircraft. The RF path to the ATNAGE II is the same as in the S-Band portion of Figure 4.7.1-2. All other satellite transmitters are OFF. The GRD is ON throughout the life of the satellite, but is unused during ascent as no commands are sent during this period.

After the satellite achieves mission orbit and attitude, on-board software commands reduce the TIP bit rate to the orbital bit rate of 8,320 bps, turn on one BTX, and switch STX-2 to SBA-2. The BTX provides real-time TIP data to CDA and Lannion. At the first pass over WTR, stored commands play back TIP data from a satellite tape recorder to the ATNAGE II via STX-2 and SBA-2.

Routine operations thereafter (in the early orbits) consist of real-time TIP data to CDA and Lannion via a BTX, TIP data playback to CDA via an STX, and commands from CDA. The available contact times allow for real-time data on approximately 95% of all orbits, real-time routine commands on approximately 75X of all orbits, and playback to CDA on approximately 75% of all orbits.

Playback time for one stored orbit is 2-1/2 minutes, allowing 1 minute for acquisition results in 3-1/2 minutes required for each orbit. The contact times available plus the satellite capability of parallel playback on two STXs simultaneously allows recovery of all TIP data, including that from multiple-blind orbits.

In an emergency, Lannion can command the satellite in response to requests from the Satellite Operations Control Center (SOCC). Emergency commands are available on approximately 95% of all orbits. In addition, in an emergency the TIP data may be transmitted via STX-2 and SOA-1, -2 to the CDA stations or via STX-4 and SOA-3, -4 to the CDA stations or SCF stations either in orbit or boost rates.

4.7.1.1.4 Ascent RF Link Analyses

The signal strength history at the NASA station at WTR during the launch of TIROS-N is shown in Figure 4.7.1-3. A similar history is expected for NOAA-K and up.

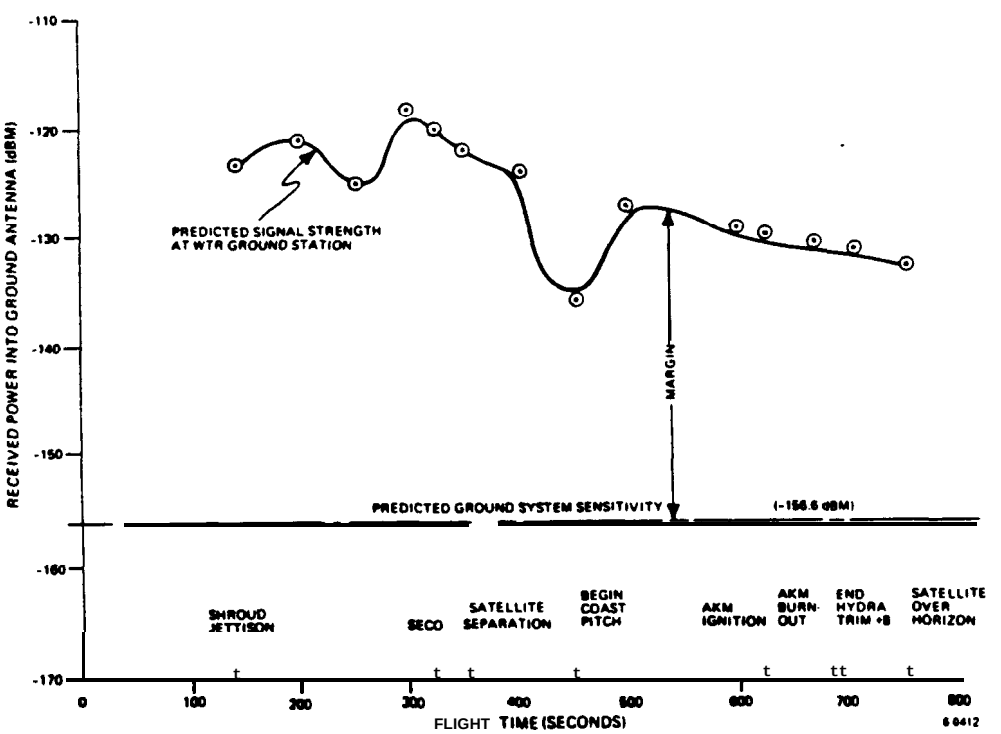


Figure 4.7.1-3. TIROS-N Boost Telemetry Signal Strength at WTR

The results of link analyses for the command and real-time telemetry links active in the early orbits are presented in Tables 4.7.1-1 and 4.7.1-2. All the links shown assume random satellite attitude and use satellite antenna-gain values that are met or exceeded over 90% of the sphere. The source of the antenna-gain values is the ATN measurements program carried out during 1979.

TABLE 4.7.1-1. S-BAND COMMAND LINK ANALYSIS (RANDOM SATELLITE ATTITUDE)

Item	Value	Source
Frequency	2025.0 MHz	S-480-25
Transmitter Power	+60 dBm	IS-2285557
Pointing Loss	-0.1 dB	IS-2285557
Ground Antenna Gain	+39.1 dBci	IS-2285557
EIRP at the Ground	+99.0 dBm	IS-2285557
Path Loss	-167.7 dB`	450 nmi, 0" elevation
Polarization Loss	-0.5 dB	IS-2285557
Satellite Antenna Gain, 85.5% of the Sphere	-1.0 dBci	Measurements in the ATN program
Satellite Insertion and VSWR Losses	-4.1 dB	IS-2285557
Command Bit Rate	2 kbps	IS-2285557
Received Power	-74.3 dBm	Calculated
Command Sensitivity, BER=10^{-6}	-108 dBm	IS-2285557
Margin	+33.7 dB	Calculated

TABLE 4.7.1-2. VHF BEACON REAL-TIME LINK ANALYSIS (RANDOM SATELLITE ATTITUDE)

Item	Value	Source
Frequency	137.35 MHZ or 137.77 MHz	S-480-25
Transmitter Power	+30 dBm	IS-2285557
Filter, Switch, Diplexer, Cable Losses	-2.7 dB	IS-2285557
VSWR Loss	-0.8 dB	IS-2285557
Satellite Antenna Gain, 90% of the sphere, assuming RCP Receiver	-17 dBci	Measurements in the ATN program
EIRP at the Satellite	+9.5 dBm	Calculated
Path Loss	-145.8 dB	450 nmi, 0' elevation
Ground Antenna Gain	+27.6 dBi	IS-2285557
Modulation Loss	-0.7 dB	IS-2285557
Bit Rate	-39.2 dB	8320 bps
System Spectral Noise Density	-156.4 dBm/Hz	IS-2285557
Demodulator Loss	-3.0 dB	IS-2285557
E_b/N_o	+13.8 dB	Calculated
Required E_b/N_o for BER=10^{-6}	+10.5 dB	Theory
Margin	+3 dB	Calculated

The playback link to the CDA stations is omitted from the analysis since it is stronger than the GAC/LAC playback link presented in Section 4.7.1.2 owing to the lower bit rate. Other than this lower bit rate, these two links are identical.

4.7.1.2 Operational Links

4.7.1.2.1 Communications Requirements

The communications requirements during the operational mode are as follows:

- Provide VHF real-time telemetry to CDA stations and to independent local users designated "Standard TIP Stations".
- Provide VHF command capability from CDA stations.
- Provide Global Area Coverage (GAC), Local Area Coverage (LAC), and stored TIP data playbacks to the CDA stations at S-Band.
- Provide S-Band TIP stored data playbacks to the Lannion ground station.
- Provide High-Resolution Picture Transmission (HRPT) data at S-band to the CDA stations and to independent local users designated "Standard HRPT Stations".
- Provide VHF Automatic Picture Transmission (APT) data to the CDA stations and to independent local users designated "Standard APT Stations"..

In each of the above services, the Communications Subsystem has one interface at RF and another at baseband. In the services listed below, the Communications Subsystem has only RF interfaces and provides only passive components. In each of these cases, the Communications Subsystem serves a transmitter or receiver that is part of a government-furnished instrument. The subsystem provides an RF path to or from the instrument. These services are as-follows:

- Provide an antenna and EM1 isolation for the receiver of the Data Collection System (DCS).
- Provide an antenna and EM1 isolation for each of three receivers in the Search and Rescue Repeater (SARR).
- Provide an antenna for the transmitter of the SARR.
- Provide an antenna and EM1 isolation for the receiver in the Search and Rescue Processor (SARP-M).

All the services listed apply only when the satellite is earth-oriented with the +X axis directed at the nadir.

4.7.1.2.2 Operational Mode Ground Station Contacts

The ground station contacts to the CDA and Lannion stations are shown in Figure 4.7.1-1. No other ground station contacts are shown in the illustration

because the other stations are not under NOAA/NASA control, and in some cases their locations are unknown.

4.7.1.2.3 Operational Mode Orbit Operations

The CDA stations issue all commands to the satellite. The Communications Subsystem requires no routine commands except to turn on or off the operational S-Band transmitters for playbacks. The transmission management includes one BTX, one VTX, and either STX-1 or -3 on full time. One or two more STX's are activated only for playbacks to one of the three stations listed above. Only the CDA stations recover LAC and GAC data. The orbit is blind to the CDA stations for up to three orbits in a row, as shown in Figure 4.7.1-1. The capability for parallel playback permits the CDA stations to recover a 2-1/2 minute playback of GAC data and simultaneously one of equal length of LAC data for each orbit. The Lannion station is required to collect TIP playbacks only on those orbits that are blind to the CDA stations.

4.7.1.2.4 Operational Mode Link Analyses

Tables 4.7.1-3 through 4.7.1-6 present the results of the analyses for links in which the transmitters or receivers of the Communications Subsystem are involved. Those services in which the subsystem provides only passive components are described by the antenna pattern and EM1 isolation data presented in Table 4.7-3. All the links covered by Tables 4.7.1-3 through 4.7.1-6 provide positive link margin throughout the region from which the elevation angle to the satellite exceeds 5" except the VHF real-time TIP links. The regions served by these links are shown graphically in Figure 4.7.1-4. All the link calculations used antenna gain and ellipticity measurements made in the ATN program.

TABLE 4.7.1-3. S-BAND COMMAND LINK ANALYSIS (OPERATIONAL ORBIT)

Item	Value	Source
Frequency	2025.0 MHz	S-480-25
Transmitter Power	+60 dBm	IS-2285557
Pointing Loss	-0.1 dB	IS-2285557
Ground Antenna Gain	+39.1 dBci	IS-2285557
EIRP at the Ground	+99.0 dBm	IS-2285557
Path Loss	-167.7 dBm	450 nmi, 5° elevation
Polarization Loss	-0.5 dB	IS-2285557
Satellite Antenna Gain, 63" Half Angle Cone About +X	-1.0 dBci	Measurements in the ATN program
Satellite Insertion and VSWR Losses	-4.1 dB	IS-2285557
Command Bit Rate	2 kbps	IS-2285557
Received Power	-74.3 dBm	Calculated
Command Sensitivity, BER=10^{-6}	-108 dBm	IS-2285557
Margin	+33.7 dB	Calculated

TABLE 4.7.1-4. VHF BEACON REAL-TIME LINK ANALYSIS (OPERATIONAL ORBIT)

Item	CDA Station TIP Station	Standard	Source
Frequency	137.35 MHz or 137.77 MHz	137.35 MHz or 137.77 MHz	i-480-25
Transmitter Power	+30 dBm	30 dBm	IS-2285557
Filter, Switch, Diplexer, Cable Losses	-2.7 dB	-2.7 dB	IS-2285557
VSWR Loss	-0.8 dB	-0.8 dB	IS-2285557
Satellite Antenna Gain Minus Path Loss in Region Shown in Figure 4.7.1-4 (Note 1)	-166.1 dB	-153.7 dB	Yeasurements in the ATN program. 450 nmi, elevation angles from the ground annotated on Figure 4.7.1-4.
Ground Antenna Gain	+27.6 dBi	+16.0 dBci	IS-2285557
Polarization Loss	0 dB	-1.1 dB	CDA stations - see Note 2. TIP stations - IS-2285557
Modulation Loss	-0.7 dB	-0.7 dB	IS-2285557
Bit Rate	-39.2 dB	-39.2 dB	IS-2285557
System Spectral Noise Density	-165.4 dBm/Hz	-165.7 dBm/Hz	IS-2285557
Demodulator Loss	-3.0 dB	-3.0 dB	IS-2285557
E_b/N_o	+10.5 dB	+10.5 dB	Calculated
Required E_b/N_o for BER = 10^{-6}	+10.5 dB	+10.5 dB	Theory
Margin	0 dB	0 dB	Calculated

NOTES: (1) Regions shown in Figure 4.7.1-4 were selected for combinations of satellite antenna gain and path loss that yield 0-dB margin in each link. Satellite antenna gain figures used assume RCP receiver, understating performance with the CDA stations which have polarization diversity receivers. No total power gain data available from ATN program.

(2) Only the RCP component was used in the EIRP calculation, although the CDA stations have diversity receivers.

TABLE 4.7.1-5. S-BAND DOWNLINK ANALYSIS (OPERATIONAL ORBIT)

Item	CDA Station	Lannion TIP Playback Station	Standard HRPT Station	Source
Frequency	1698 MHz or 1702.5 MHz or 1707 MHz	1698 MHz or 1707 MHz or 1707 MHz	1698 MHz or 1707 MHz	S-480-25. Note: links carried out for the 1707-MHz case which has the lowest satellite EIRP
Transmitter Power	+38.0 dBm	+38.0 dBm	+38.0 dBm	IS-2285557
Cable Losses	0.5 dB	0.5 dB	0.5 dB	IS-2285557
VSWR Loss	-0.2 dB	-0.2 dB	-0.2 dB	IS-2285557
Satellite Antenna Gain, Edge of 63° Half-Angle Cone About +X	-0.1 dBci	-0.1 dBci	-0.1 dBci	IS-2285557
EIRP at the Satellite	+36.0 dBm	+36.0 dBm	+36.0 dBm	Calculated
Path Loss	-166.2 dB	-166.2 dB	-166.2 dB	450 nmi, 5° elevation
Polarization Loss	-0.2 dB	-0.5 dB	-0.5 dB	CDA: IS-2285557; Lannion & HRPT station: 8 dB measured ellipticity in ATN program into assumed 2 dB ellipticity ground antenna
Fading and Rain Loss	-0.4 dB	-0.4 dB	-0.4 dB	IS-2285557
Ground Antenna Gain	+46.8 dBi	+31 dBci	+31 dBci	IS-2285557
Modulation Loss	-0.7 dB	-0.7 dB	-0.7 dB	IS-2285557
Pre-mod Filter Loss	-1.2 dB	-0.2 dB	-0.4 dB	IS-2285557
Adjacent Channel Interference	-3.0 dB	0 dB	-1.2 dB	IS-2285557
Bit Rate	-64.2 dB	-55.2 dB	-58.2 dB	IS-2285557; 2.6616 Mbps, 337.2 kbps, 665.7 kbps, respectively
System Spectral Noise Density	-175.4 dBm/Hz	-175.4 dBm/Hz	-175.4 dBm/Hz	IS-2285557
Demodulator Loss	-3.0 dB	-3.0 dB	-3.0 dB	IS-2285557
E_b/N_0	+19.3 dB	+16.2 dB	+11.8 dB	Calculated
Required E_b/N_0 for BER=10^{-6}	+10.5 dB	+10.5 dB	+10.5 dB	Theory
Margin	+8.8 dB	+5.7 dB	+1.3 dB	Calculated

TABLE 4.7.1-6. VHF APT REAL-TIME LINE ANALYSIS (OPERATIONAL ORBITS)

Item	CDA Stations	Standard APT Stations	Source
Frequency	137.50 MHZ or 137.62 MHz	137.50 MHz or 137.62 MHz	S-480-25
Transmitter Power	+37.0 dBm	+37.0 dBm	IS-2285557
Filter, Switch, Cable Losses	-1.3 dB	-1.3 dB	IS-2285557
VSWR Loss	-0.8 dB	-0.8 dB	IS-2285557
Satellite Antenna Gain, 63" Half-Angle Cone about +X	-1.4 dBci	-1.4 dBci	Measurements on ATN program
EIRP at the Satellite	+33.5 dBm	+33.5 dBm	Calculated
Path Loss	-144.3 dB	-144.3 dB	450 nmi, 5" elevation
Ground Antenna Gain	+27.6 dBi	+10 dBci	IS-2285557
Polarization Loss	-0.2 dB	-0.7 dB	CDA: IS-2285557; APT Station: measured 10 dB worst-case VRA ellipticity on ATN into assumed 2 dB antenna
IF Bandwidth	-47.8 dB/Hz	-47.0 dB/Hz	IS-2285557
Required CNR	+12.0 dB	+12.0 dB	IS-2285557
System Noise Spectral Density	-165.4 dBm/Hz	-163.2 dBm/Hz	IS-2285557
CNR	+34.2 dB	+14.7 dB	Calculated
Margin	+22.2 dB	+2.7 dB	Calculated

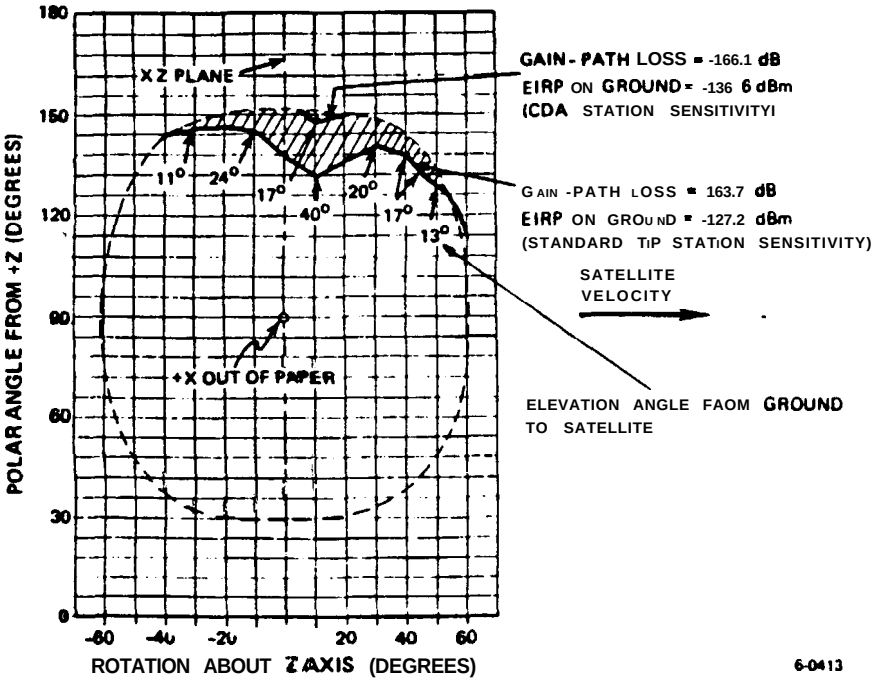


Figure 4.7.1-4. VHF Beacon Coverage Areas for Positive Link Margin (Operational Orbit)

4.7.2 COMMUNICATIONS SUBSYSTEM COMPONENT DESCRIPTION

4.7.2.1 S-Band Transmitters (STX-1, -2, -3, -4)

The STXs, designed and built by ASD, are high-efficiency, all solid-state units which employ PM modulation directly at S-Band. A photograph of the STX is shown in Figure 4.7.2-l. STX-1, -2, and -3 characteristics are summarized in Table 4.7.2-l and STX-4 in Table 4.7.2-2. A functional block diagram of the STX is shown in Figure 4.7.2-2 and the STX electrical interfaces are depicted in Figure 4.7.2-3.

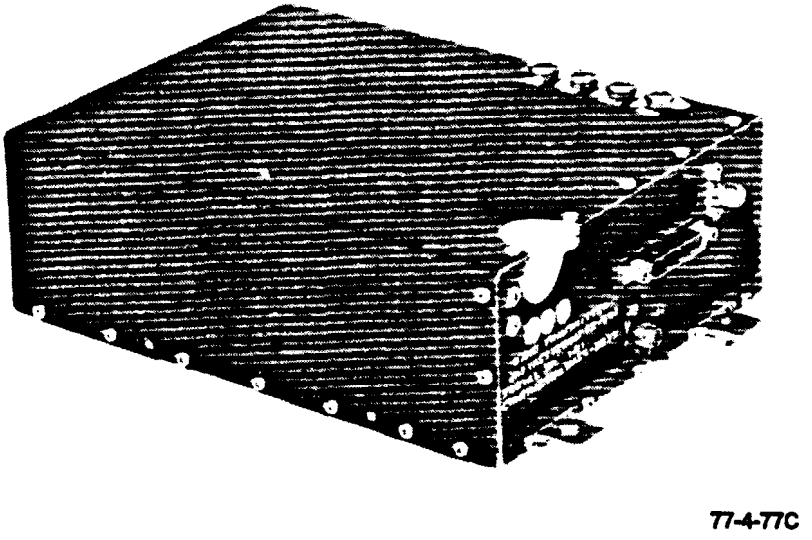


Figure 4.7.2-l. S-Band Transmitter (STX)

TABLE 4.7.2-l. S-BAND TRANSMITTER CHARACTERISTICS (STX-1, -2, -3)

Parameter	Value
Modulation	
• Type	PSK
• Input	8320 bps split-phase-level 16,640 bps split-phase-level, 332.7 kbps split-phase-level 1.3308 Mbps split-phase-level 2.6616 Mbps NRZ-level between 0 ±0.3 volt and 4.5 ±0.7 volts
• Modulation Sensitivity	135" ±5% in response to above level changes
• Pre-Modulation Filter	Flat ±1 dB dc to 1.5 MHz Flat +1, -3 dB, 1.5 MHz to 2.4 MHz -30 dB/octave roll-off starting at 3.5 MHz
• Linearity	±0.2 radian deviation from a straight line through end points of modulator voltage vs. RF phase
• Demodulated Rise and Fall Times	Between 85 ns and 200 ns
• Demodulated Overshoot	25% of steady-state step
• Demodulated Asymmetry	3%
Output Frequency	STX-1: 1698 MHz STX-2: 1702.5 MHz STX-3: 1707 MHz
Frequency stability	±0.002%
Spurious phase modulation	Less than 12° from 100 Hz to 200 Hz in a transparent PM receiver; less than 3" rms jitter in a phase-locked loop with 30-Hz bandwidth
Incidental Amplitude Modulation	5%
Output Power, EOL	6.35 watts
Turn-On Time	6 seconds
Power Requirements	
• 28 v ±2%	915 mA
• 10 v ±2%	10 mA

TABLE 4.7.2-l. S-BAND TRANSMITTER CHARACTERISTICS (STX-1, -2, -3) (Continued)

Parameter	Value
Conducted Emissions	
• Broadband	-30 dBm, 10 kHz to 10 GHz
• Narrowband	-40 dBm/1 MHz 148 to 154 MHz 394 to 406 MHz 2020 to 2120 MHz -34 dBm/3 kHz - radio astronomy -6 dBm/3 kHz - GOES band
• Occupied Band	-60 dBc/3 kHz beyond 4.5 MHz from carrier, with random 2.6616 Mbps modulation; 98% of power within 2.5 MHz of carrier with same modulation
Size (inches)	6.4 x 4.9 x 2.1
Weight (lb)	2.2
Temperature (°C)	-5 to +45
Useful Life (100% duty)	2.5 years minimum

The output frequency is generated by a microwave oscillator which feeds a linear S-Band phase modulator. The digital data signal is shaped by a pre-modulation 0.05 degree equiripple phase lowpass filter with a 3-dB bandwidth of 2.4 MHz. This filter is the primary means of controlling the transmitter RF spectrum. The S-Band signal out of the modulator is amplified by a four-stage power amplifier. The first three stages operate Class A, while the final stage operates Class C with a collector efficiency of 52 percent. The final stage drives an isolator-lowpass filter which provides open/short circuit protection as well as attenuation of transmitter harmonics to greater than 68 dB below the carrier. The nominal power output of the STX is 8 watts.

The transmitters operate off the 28-volt bus and have internal solid-state power switches which control the on-off operation based on logic-level signals received from the CIU. Following the power switch, a series regulator is used to generate the +15 volts required by the microwave oscillator and modulator-driver circuits. The output of the power switch is directly fed to the power amplifier stages. The three STX's operate at different{-frequencies: STX-l at 1698 MHz, STX-2 at 1702.5 MHz, and STX-3 at 1707 MHz.

4.7.2.2 VHF Real-Time Transmitters (VTX-l, -2)

The VTX-1 and VTX-2 transmitters are manufactured by Loral Data Systems-Conic. An outline drawing of the VTX is shown in Figure 4.7.2-4 and the characteristics are summarized in Table 4.7.2-3. A functional block diagram of the VTX is shown in Figure 4.7.2-5 and the VTX electrical interfaces are depicted in Figure 4.7.2-6.

TABLE 4.7.2-2. S-BAND TRANSMITTER CHARACTERISTICS (STX-4)

Parameter	Value
Modulation	
• Type	PSK
• Input	8320 bps Split Phase Level 16,640 bps Split Phase Level 332.7 kbps Split Phase Level 1.3308 mbps Split Phase Level 2.6616 mbps NRZ-L
• Modulation Sensitivity	135' ±5%
• Linearity	Same as STX-1, -2, and -3
Output Frequency	2247.5 MHz
Frequency stability	±0.002%
Residual phase modulation	12°/RMS or less
Incidental Amplitude Modulation	5%
Output Power, EOL	5.25 watts
Turn-On Time	6 seconds
Power Requirements	
• 28 V ±2%	925 mA
• 10 v ±2%	10 mA
Conducted Emissions	
• Narrowband	Same as STX-1, -2, -3
• Narrow or Broadband	Same as STX-1, -2, -3
Size (inches)	Same as STX-1, -2, -3
Weight (lb)	Same as STX-1, -2, -3
Temperature (°C)	Same as STX-1, -2, -3
Useful Life (100% duty)	Same as STX-1, -2, -3

The VTX is fundamentally a frequency modulated VHF transmitter. Referring to the block diagram, the VCXO operates at 22 MHz which is frequency modulated and doubled to 45 MHz. The signal is multiplied to 137 MHz and bandpass filtered prior to amplification to 5.2513 watts by the Class C power Amplifier. The power amplifier is followed by a final low pass filter and lumped constant

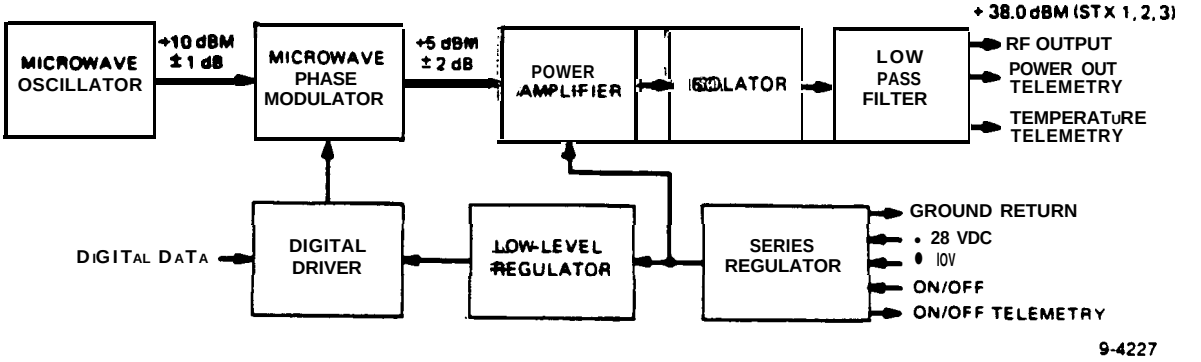


Figure 4.7.2-2, S-Band Transmitter Block Diagram

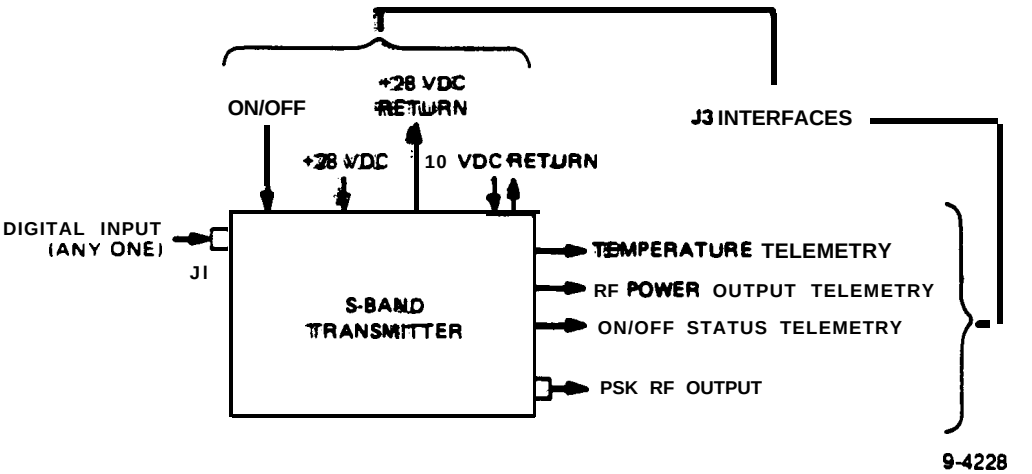


Figure 4.7.2-3 S-Band Transmitter Interfaces

isolator for mismatch protection, The output LPF additionally provides loop coupling for RF sampling for the RF telemetry and ALC outputs. The ALC output provides feedback to the main regulator for control of the driver and PA voltage, maintaining the voltage between 18 and 22 Vdc thereby maintaining the nominal 5.25W RF output. The modulation buffer is a unity gain amplifier providing buffering and isolation of the modulator input to the VCXO.

4.7.2.3 VHF Beacon Transmitter (BTX-1, -2)

The BTX-1 and BTX-2 transmitters are also manufactured by Loral Data Systems/ Conic and are similar in design with the VTX-1, -2. An outline drawing of the BTX is shown in Figure 4.7.2-7 and the characteristics of the BTX are summarized in Table 4.7.2-4. A functional block diagram of the BTX is shown in Figure 4.7.2-8 and the associated electrical interfaces depicted in Figure 4.7.2-9.

The BTX is a nominal 1W EOL watt phase modulated VHF transmitter. Referring to the block diagram, the oscillator employs a third overtone crystal at 45

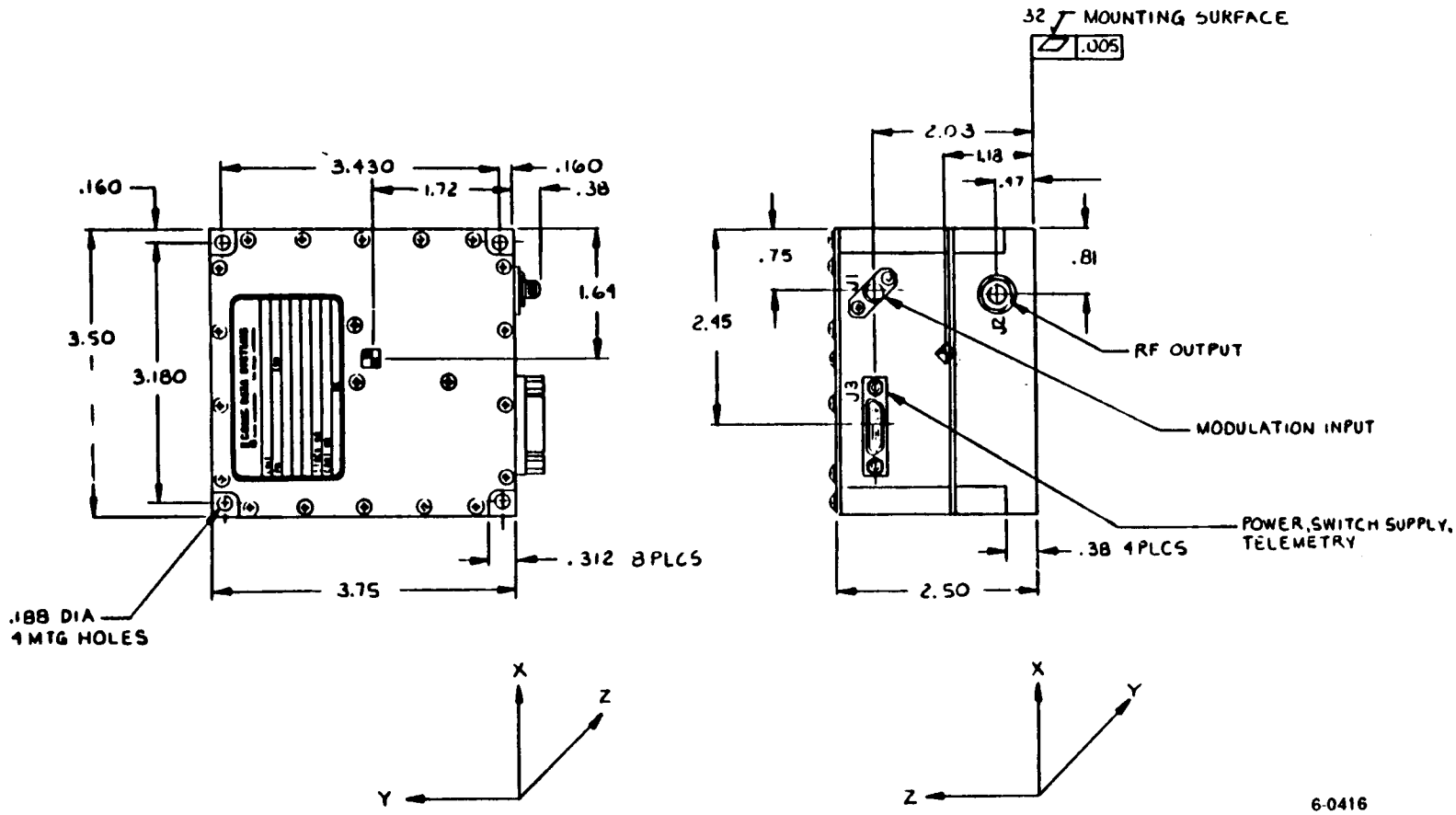


Figure 4.7.2-4. VHF Real-Time Transmitter Outline Drawing

TABLE 4.7.2-3. VHF REAL-TIME TRANSMITTER CHARACTERISTICS

Parane ter	Value
Modulation	
• Type	FM
• Modulation Sensitivity	2.8 V p-p at input produces 34 kHz p-p deviation
• Peak Frequency Deviation	±18.7 kHz
• Deviation Linearity	±600 Hz about best-fit straight line through ±18.7 kHz range
Frequency Response	±0.5 dB from 0.1 to 4.8 kHz
. Input	2.4-kHz amplitude-modulated subcarrier at 2.8 V p-p
Output Frequency	137.500 MHz (VTX-1) 137.620 MHz (VTX-2)
Frequency Stability	~0.002%
Residual FM	340 Hz p-p
Harmonic Distortion	2.5% when modulated with 2.4 kHz and carrier deviates ±17 kHz
Amplitude Modulation	5% when carrier deviates ±17 kHz
Output Power	
• BOL	5.5 watts minimum
• EOL	5.0 watts minimum
Turn-On Time	
• Meets Power Spec	10 seconds
• Meets Frequency Stability	30 seconds
Power Requirements	
• 28 V ±2%	0.72 ampere exclusive of switched 28 V output
• 10 v ±2%	0.01 ampere
Switched 28 V Output for RF Switch	120 mA pull-in 30 mA hold-in
Conducted Emissions	
• Narrowband	-25 dBm - dc to 10 GHz
• Narrow or Broadband	-45 dBm/3 kHz - radio astronomy -40 dBm/1 MHz - DCS -70 dBm/40 kHz - 128.16 ±1 MHz
• Occupied band	-60 dBc beyond 40 kHz from carrier, maximum frequency deviation
Size (inches max)	2.0 H x 3.5 W x 3.75 D
Weight	1.75 lb maximum
Temperature	-5° to +45°C
Useful life (100% duty)	2.5 years minimum

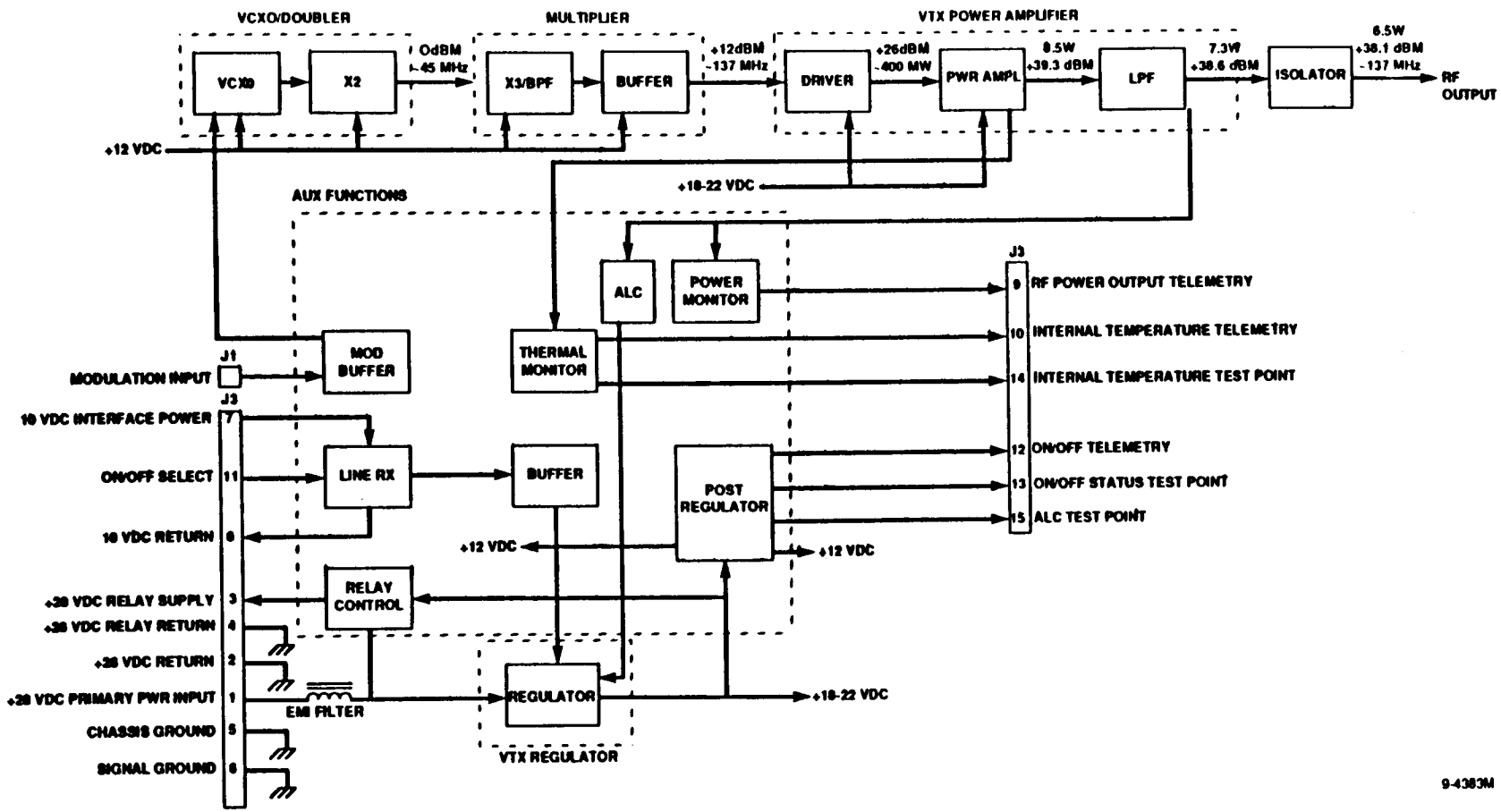


Figure 4.7.2-5. VHF Real-Time Transmitter Block Diagram

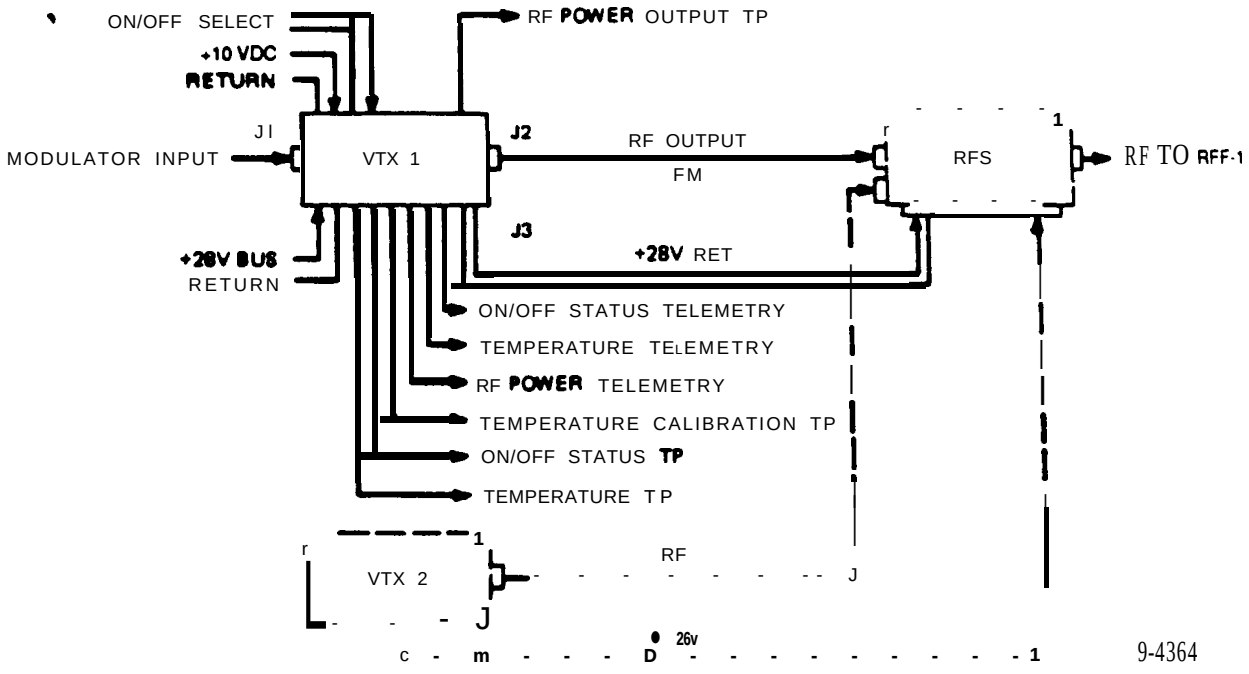


Figure 4.7.2-6. VHF Real-Time Transmitter Interfaces

MHz which is fed to a varactor controlled phase modulator. Following phase modulation of the crystal frequency, the signal is multiplied to 137 MHz with lowpass filtering and amplified to two watts by a Class C power amplifier. As in the VTX the output of the power amplifier is fed to a low pass filter and isolators with an RF sample provided for RF telemetry and ALC. The TTL level square wave modulation input is level translated clamped and filtered by a lowpass filter prior to phase modulation of the exciter signal.

4.7.2.4 G-STDN Command Receiver-Demodulator (GRD)

The GRD, supplied by Loral/Conic, consist6 of three interwired, stacked aluminum housings, one for the receiver, one for the detector, and one for the demodulator. An outline drawing of the GRD is shown in Figure 4.7.2-10 and the GRD characteristics are summarized in Table 4.7.2-5. A GRD functional block diagram and the GRD electrical interfaces are presented in Figure6 4.7.2-11 and 4.7.2-12, respectively.

The GRD is powered continuously when the spacecraft is "ON". It receives RF inputs from the Omni Antennas, SOA-5, -6.

Figure 4.7.2-11 shows the redundancy and automatic crossover that are provided by signal cross-strapping from both S-Band receiver6 to both the demodulators. Because of this redundancy and wiring arrangement, plus the use of high-reliability parts, the GRD meet6 or exceeds a probability of successful operation of 0.997 after 2 years in earth orbit. Furthermore, the GRD contains no single-point failure modes which would result in a loss of command function.

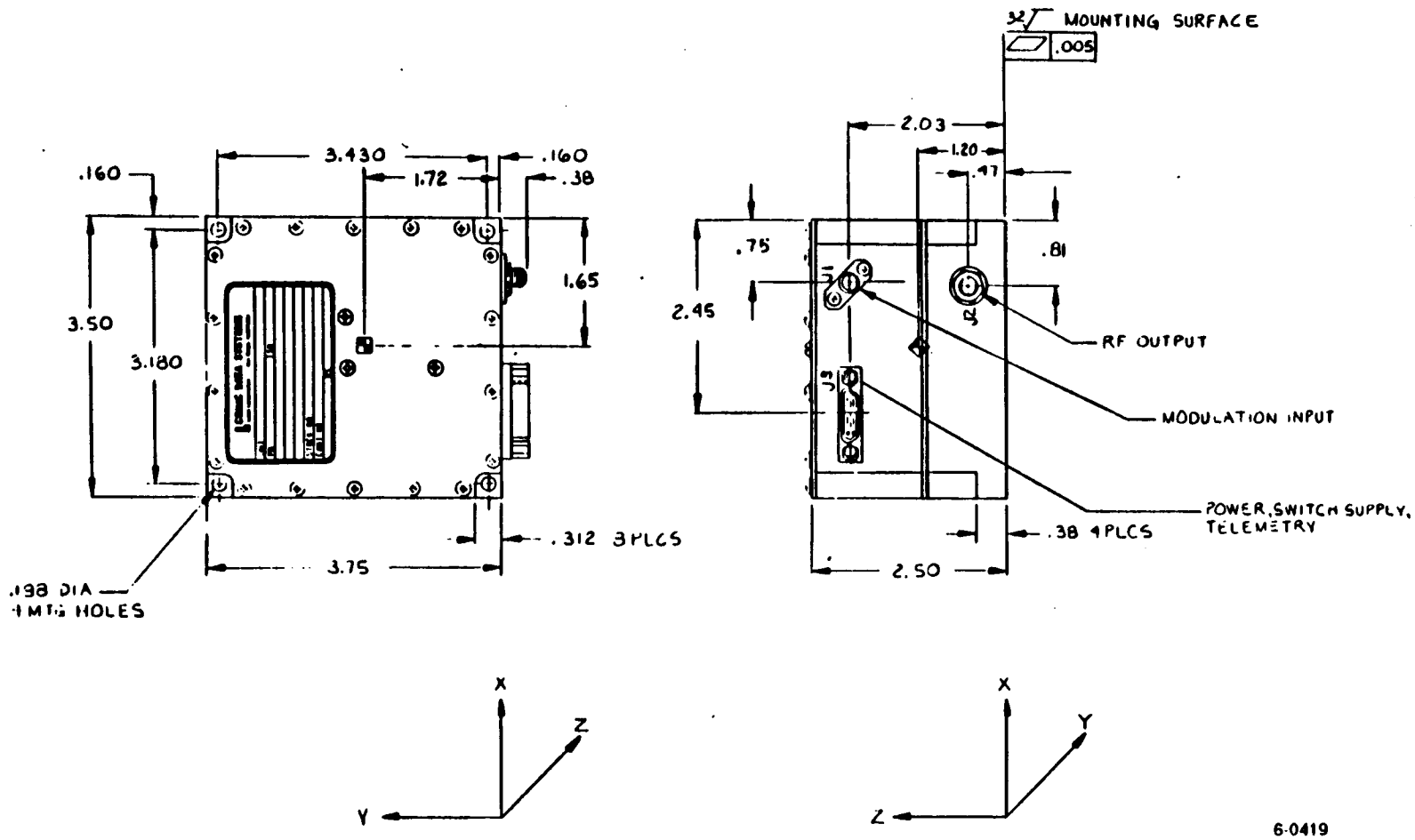


Figure 4.7.2-7. VHF Beacon Transmitter Outline Drawing

TABLE 4.7.2-4. BEACON TRANSMITTER CHARACTERISTICS

Parameter	Value
Modulation	
• Type	PSK
• Modulation Sensitivity	135 ±4 degrees p-p phase change in response to logic level change at input
• Input	8320 bps split-phase-level data 3 ±0.3 volt and 4.5 ±0.7 volts Input voltage drives logic gate in BTX
• Pre-Modulation Filter	Flat ±0.5 dB 100 Hz to 9 kHz -3 dB between 16 and 22 kHz -42 dB/octave above 22 kHz
• Linearity	±3° deviation from a straight line through end points of modulator input voltage vs RF phase
• Demodulated Rise and Fall Times	10 to 30 microseconds
• Demodulated Overshoot	25 percent of steady-state step
• Demodulated Bit Asymmetry	3 percent (pulse width error/bit period)
Output Frequency	137.35 MHz (BTX-1) 137.77 MHz (BTX-2)
Frequency Stability	±0.002%
Spurious Phase Modulation	1.5" rms in an ideal phaselocked-loop receiver with 30-Hz loop bandwidth
Incidental Amplitude Modulation	3%
Output Power	1.0 watt
Turn-On Time	
• Meets Power Specs	10 seconds
• Meets Frequency Stability Specs	30 seconds
Power requirements	
• 28V_ +2%	272 mA exclusive of switched 28 V output
• 10V ±2%	10 mA
Switched 28 V output for RF Switch	120 mA pull-in 30 mA hold-in
Conducted Emissions	
• Narrowband	-25 dBm dc to 10 GHz
• Narrow or Broadband	-45 dBm/3 kHz - radio astronomy -40 dBm/1 MHz - DCS -70 dBm/40 kHz - VHF command -40 dBm/40 kHz - 128.16 ±1 MHz
• Occupied Band	-60 dBc/3 kHz beyond 100 kHz from carrier, with random 8320 bps modulation
Size (inches)	2.0 H x 3.5 W x 3.75 D
Weight	1.75 lb maximum
Temperature	-5°C to ±45°C
Useful life (100% duty)	2.5 years minimum

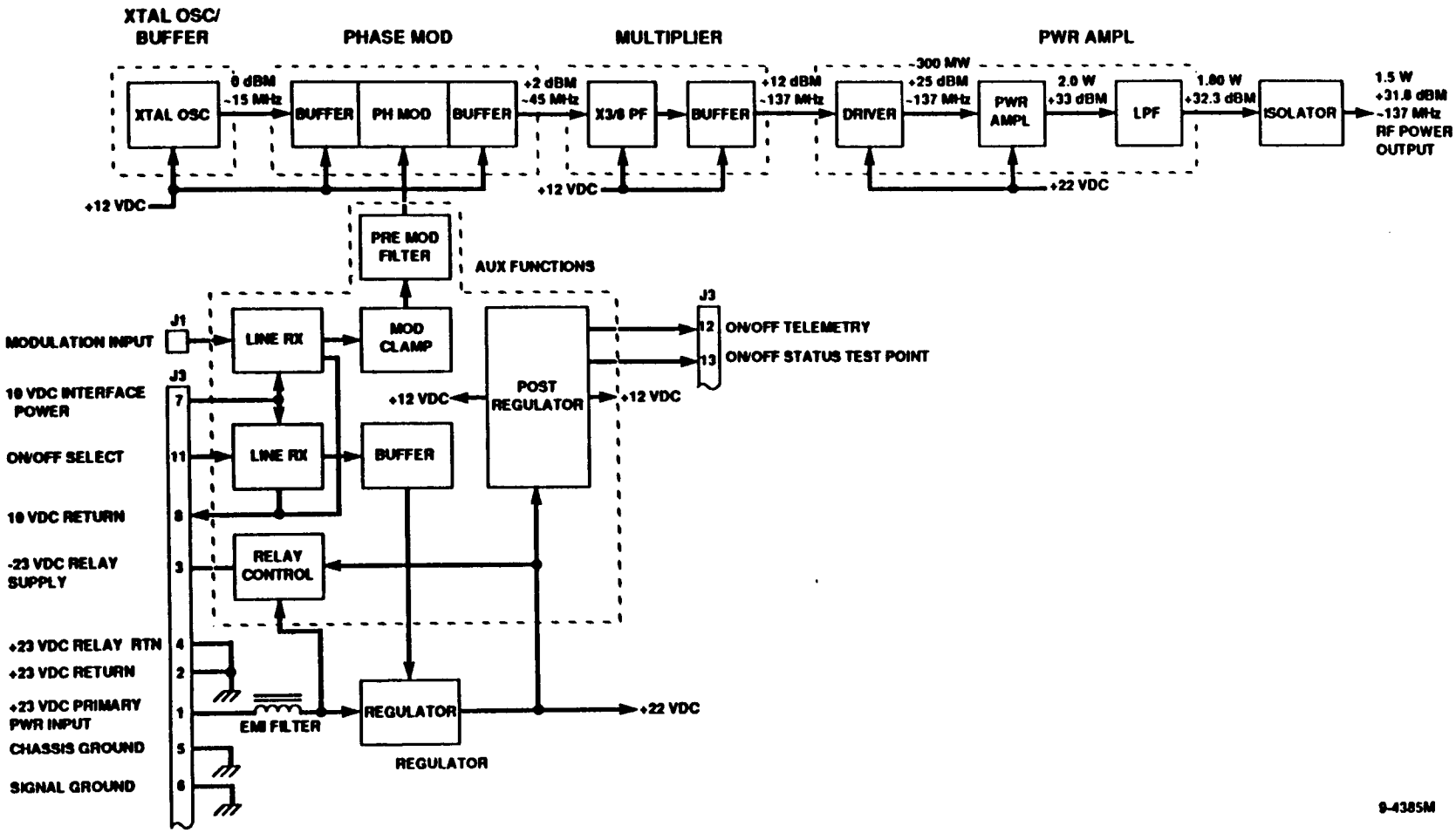


Figure 4.7.2-8. Beacon Transmitter Block Diagram

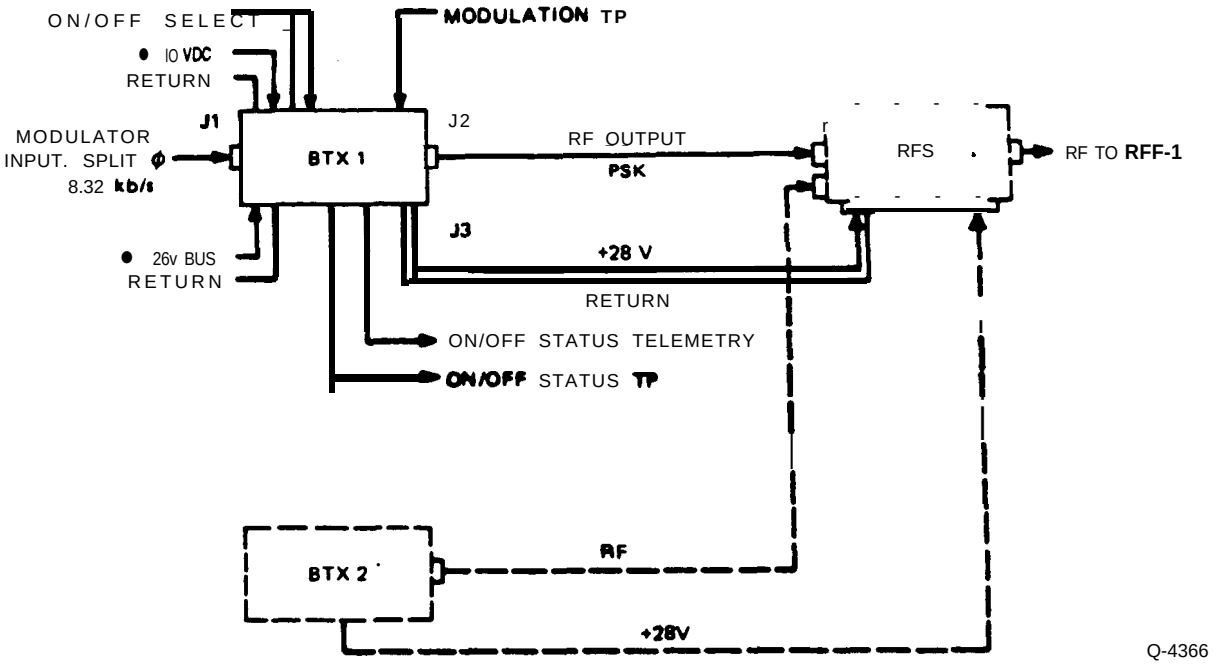


Figure 4.7.2-9. Beacon Transmitter Interfaces

The GRD will remain in the standby mode until it senses an RF signal strength greater than -118 dBm at either or both RF inputs. In this standby condition, the GRD disconnects power from the demodulator output stages.

Upon receiving a signal that is equal to or greater than the above, and with the proper subcarrier modulation, the GRD applies power to the demodulators. The GRD is then capable of processing data at 10^{-6} BER or better, and is in its fully operational mode.

The GRD receives and processes NRZ-M commands. These command signals are first modulated onto a 16.0 kHz subcarrier and then transmitted to the spacecraft. The subcarrier is then modulated onto a 2025.0 MHz carrier and then transmitted to the spacecraft. Two level states representing a 1 or 0, are sent singularly in a series of patterns to represent the desired command message.

The GRD receiver is a dual-conversion superheterodyne design, with the phase locked loop for carrier acquisition and tracking. The detected subcarrier output from each receiver is coupled to both demodulators. Each demodulator detects and locks on to a subcarrier from one of two receivers. It then demodulates the subcarrier and extracts the NRZ-M command data. The demodulator also generates and outputs a synchronous clock for cross-strapping. The demodulator contains a 10 Hz oscillator which is used to control the alternate sampling of each of the receiver/detector outputs until one demodulator locks-up. This oscillator insures that the demodulator will lock within 250 ms upon application of a receiver input.

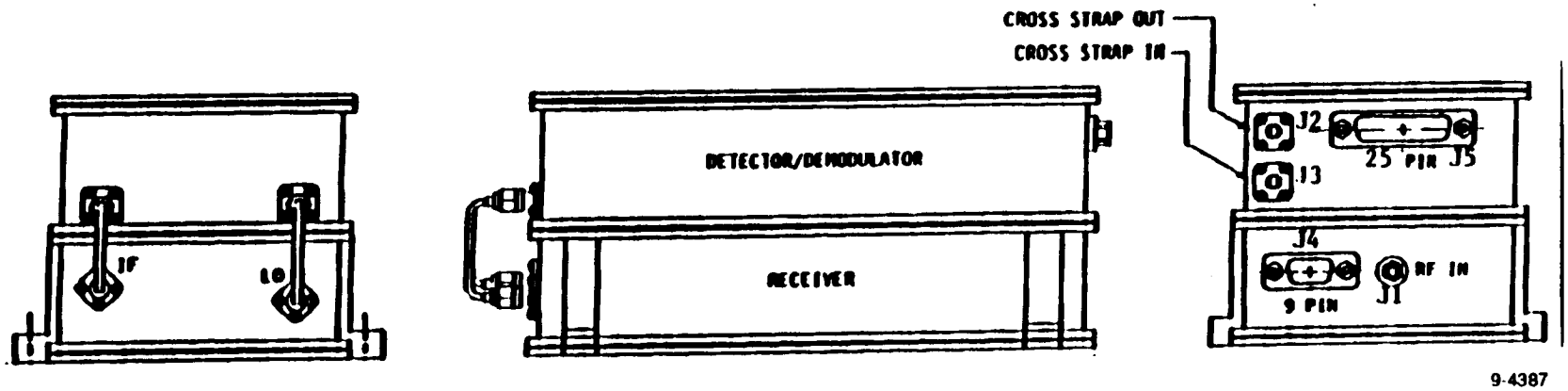


Figure 4.7.2-10. G-STDN Command Receiver-Demodulator

TABLE 4.7.2-5. COMMAND RECEIVER-DEMODULATOR CHARACTERISTICS

Parameter	Value
Carrier Frequency	2025.0 ±0.061 MHz
Sensitivity for BER=10^{-6}	-118 dBm
Receiver Sensitivity	-127 dBm (approx.)
Noise Figure (max.)	6.0 dB
Preselector Bandwidth . 3 dB	 25 MHz, max
Acquisition Time (Carrier)	9.0 sec
Deactivation Time	50 ms, max
Carrier Modulation	PM
Modulating Waveform • Subcarrier • Bit Rate	 16.0 kHz 2 kbps
Power Requirements . 28 V ±2% • 10 v ±2%	 200 mA operational mode 10 mA
Redundancy	2 receiver/demodulator pairs, powered independently; cross strapping via external cables
Size (inches)	3.2 H x 4.35 W x 7.93 D
Weight	8.6 lb (combined weight)
Temperature	-5' to +45°C
Useful Life (100% duty)	5 years minimum

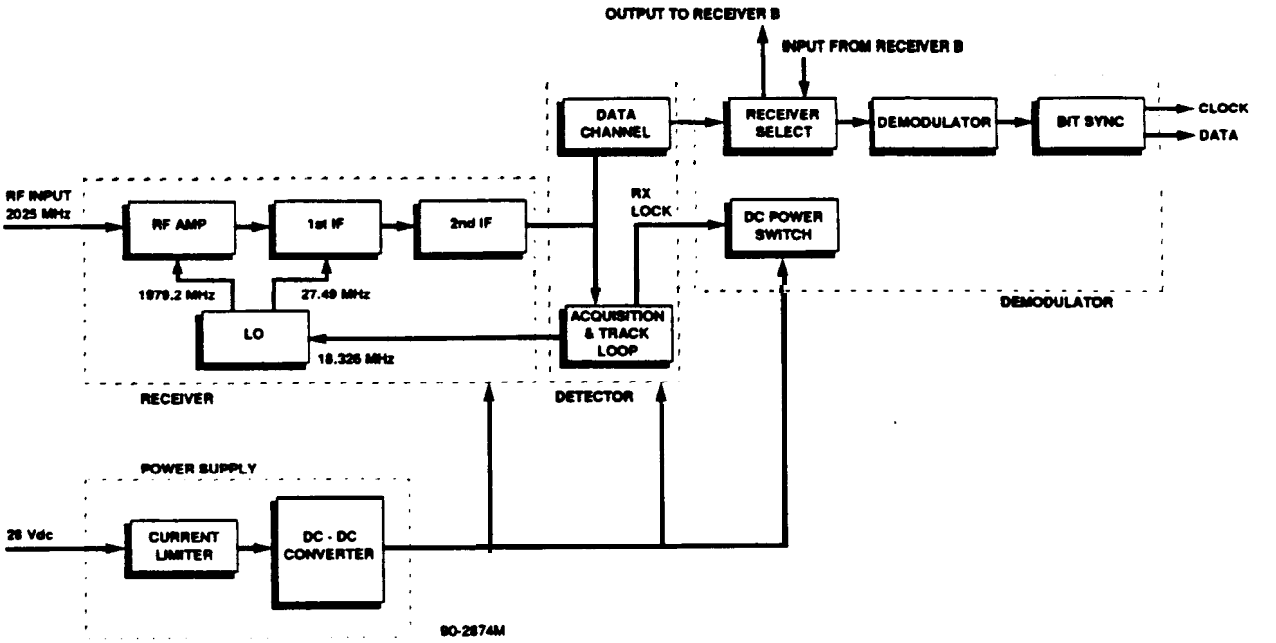


Figure 4.7.2-11. G-STDN Command Receiver-Demodulator Block Diagram

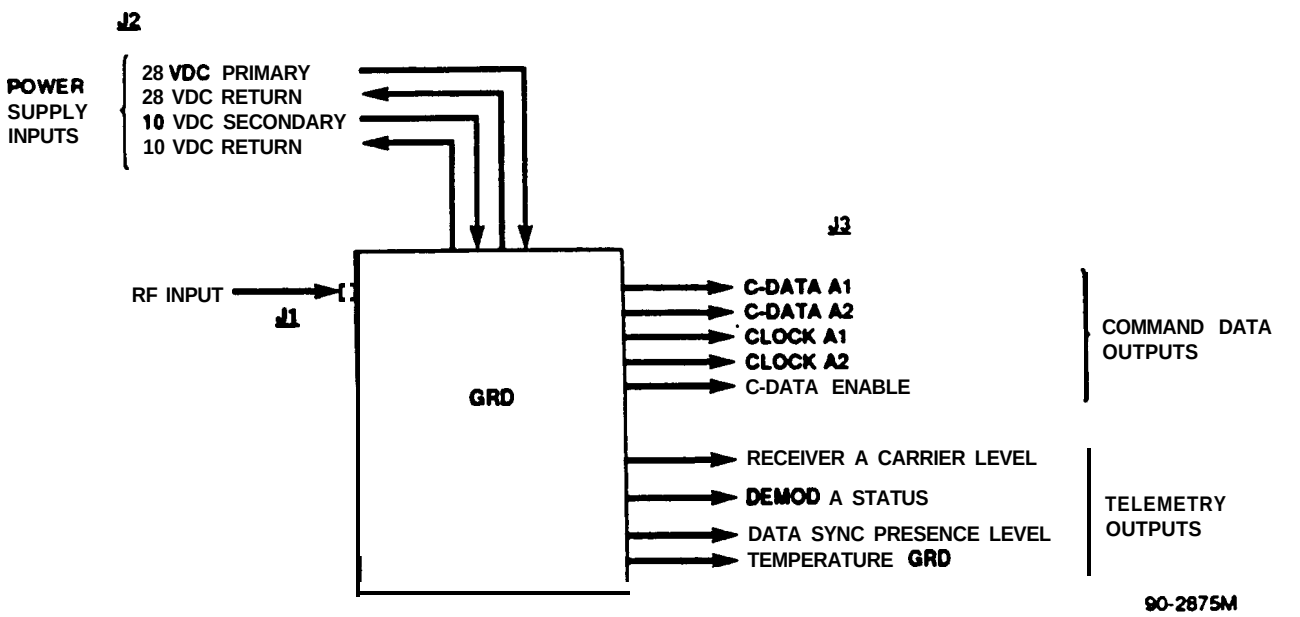
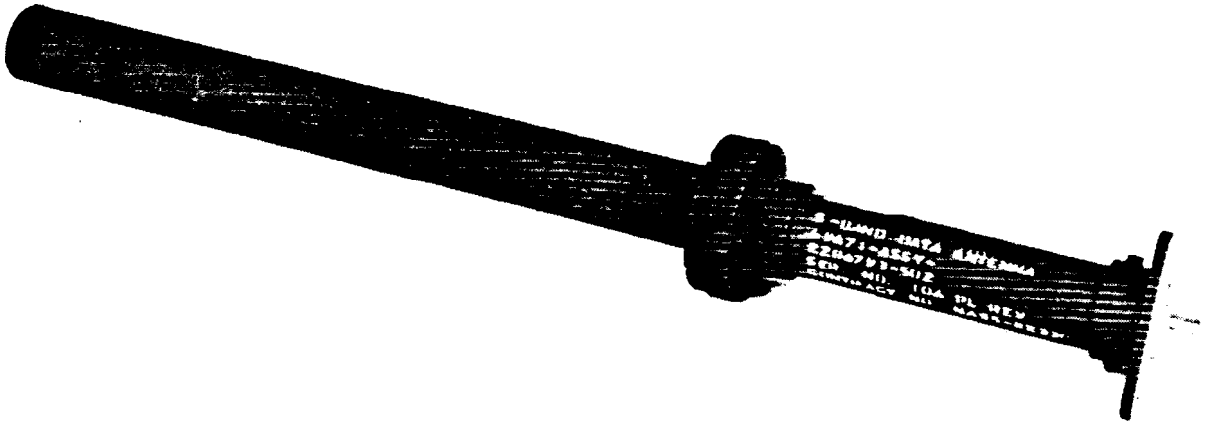


Figure 4.7.2-12. G-STDN Command Receiver-Demodulator Interfaces (Each Unit)

4.7.2.5 Deleted

4.7.2.6 S-Band Antenna (SBA-1, -2, -3)

The SBA, designed and fabricated at ASD, is a self-phased, resonant quadrifilar antenna with a bifolium pattern. A photograph of the SBA is shown in Figure 4.7.2-13 and the SBA characteristics are summarized in Table 4.7.2-6.



81-1-161C

Figure 4.7.2-13. S-Band Antenna

The quadrifilar is a four element helical antenna with the elements driven in phase quadrature. The antenna is comprised of the radiating elements and a balun. The four helical elements produce a bifolium (shaped-conical) pattern. The helical design is 1-1/2 turns and 1-1/4 wavelengths. The sense (right hand or left hand) of circular polarization is determined by the direction in which the elements are wound. Designs for both right-hand and left-hand circular polarization are obtained by reversing the direction of element winding.

TABLE 4.7.2-6. S-BAND ANTENNA CHARACTERISTICS

Parameter	Value
Frequency	1698 to 1707 MHz
Polarization • SBA-1 & SBA-3 • SBA-2	 RCP LCP
Coverage	63" half-angle cone
Gain (free-space measurement)	See Figure 4.7.2-14
Ellipticity (free-space measurement)	4.5 dB
Nominal Impedance	50 ohms
VSWR, 1692.5 to 1712.5 MHz	1.5:1
Power Handling	18 watts - from one atmosphere pressure to hard vacuum
Weight	0.7 lb, excluding mounting hardware
Temperature	-71' to +60°C

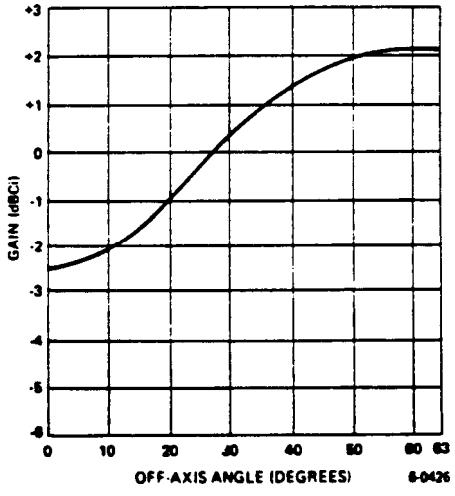
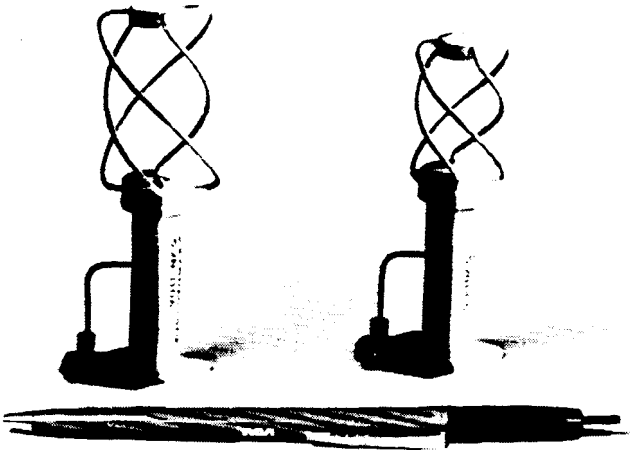


Figure 4.7.2-14. S-Band Antenna Free-Space Minimum Gain

4.7.2.7 S-Band Omni Antenna (SOA)

The SOA is designed and built by ASD. A photograph is shown in Figure 4.7.2-15. The characteristics of the antennules of SOA are summarized in Table 4.7.2-7. The SOA-1, -2 are an array of two elements, one Right-Hand Circular (RHC) element illuminating the earthward hemisphere (+ x or nadir axis), and the second Left-Hand Circular (LHC) element illuminating the anti-earth



74-3-60C

Figure 4.7.2-15. Antennules for the S-Band Omni Antennas

TABLE 4.7.2-7. S-BAND OMNI ANTENNULE CHARACTERISTICS

Parameter	Value
Frequency (MHz)	
SOA-1, -2	1702.5
SOA-3, -4	2247.5
SOA-5, -6	2025.0
Bandwidth (%)	1 . 0
Polarization	
SOA-1, -2	RCP, LCP
SOA-3, -4	RCP, RCP
SOA-5, -6	RCP, RCP
Ellipticity, within 63" of Axis (dB)	6
Gain	Figure 4.7.2-16
Normal Impedance (ohms)	50
VSWR	1.5:1
Power Handling, One Atmosphere to Hard Vacuum (watts)	10
Size (inches)	
SOA-1, -2	1.1 Dia x 3.6 L
SOA-3, -4	0.91 Dia x 3.65 L
SOA-5, -6	0.91 Dia x 3.65 L
Weight (ounces)	Less than 4
Temperature (°C)	-50 to +100°

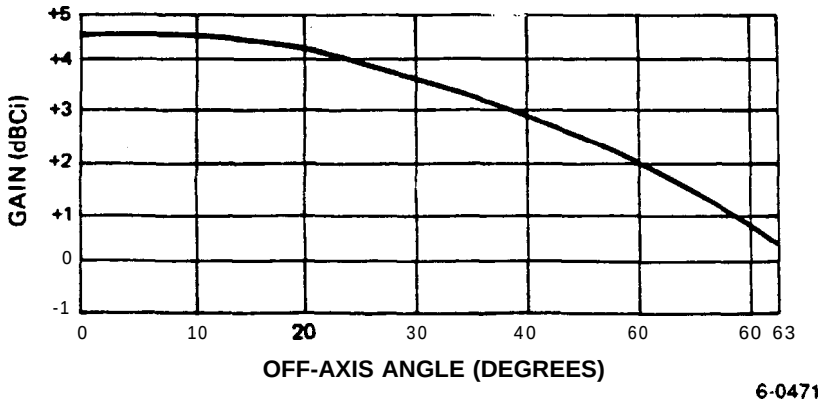


Figure 4.7.2-16. S-Band Omni Antennule Free-Space Minimum Gain

hemisphere (-x or anti-nadir axis). This arrangement reduces the destructive interference the two antennule patterns produce in the Y-Z plane by allowing simultaneous observation by RCP and LCP receivers. SOA-3, -4, -5 and -6 are all RHC elements illuminating the +X and -X axis.

Each element is a one-half turn, one-half wavelength resonant, self-phased, quadrifilar radiator. Quasi-isotropic coverage is achieved by simultaneously feeding the two elements from the two isolated output ports on a hybrid power splitter. Quasi-isotropic coverage is enhanced by the use of the polarization-diversity CDA and Stadan receivers, which will optimally receive RHC, LHC or linearly polarized signals.

4.7.2.8 VHF Real-Time Antenna (VRA)

The VRA, designed and built by ASD, is a 1/2-turn, 1/2-wavelength resonant quadrifilar antenna. A photograph of the VRA is shown in Figure 4.7.2-17; the VRA characteristics are summarized in Table 4.7.2-8.

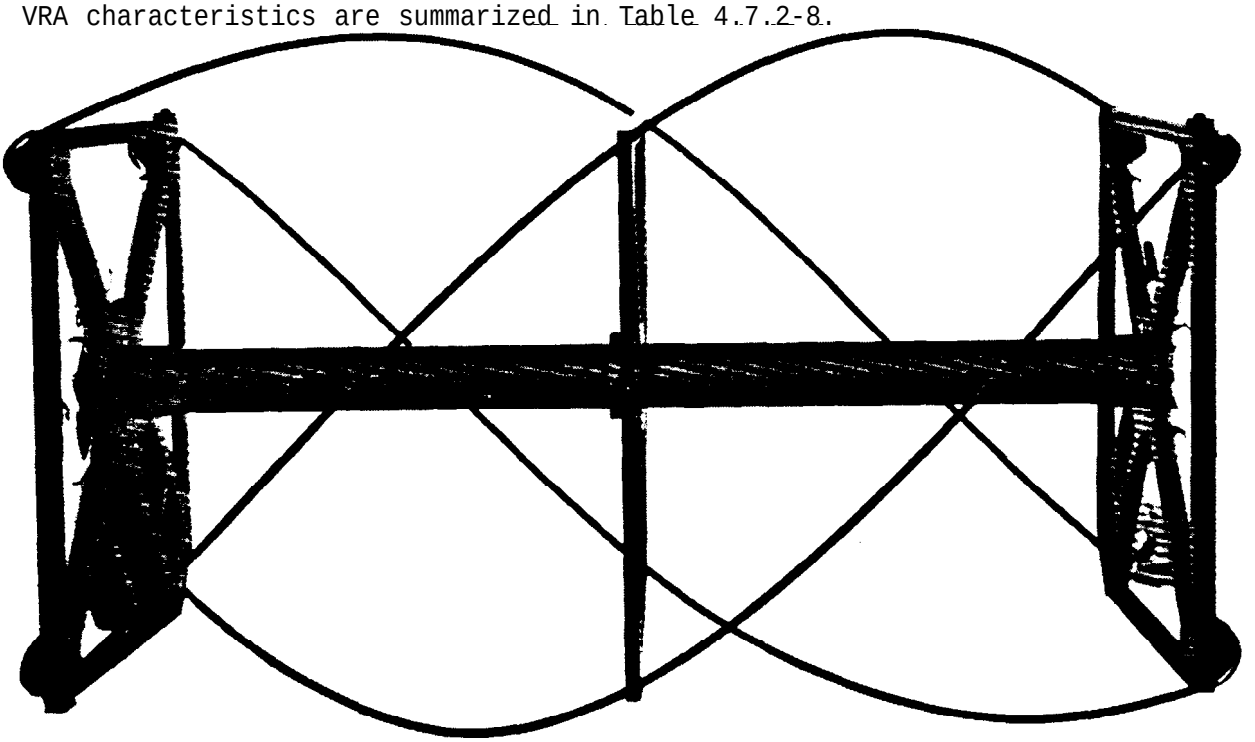


Figure 4.7.2-17. VHF Real-Time Antenna 81-1-160C

TABLE 4.7.2-8. VRA CHARACTERISTICS

Parameter	Value
Frequency Range	136 to 138 MHz
Polarization	RCP
Coverage	63" half-angle cone
Ellipticity (free-space measurement)	4.0 dB over coverage region
Gain (free-space measurement)	See Figure 4.7.2-18
Nominal Impedance	50 ohms
VSWR	1.5:1
Power Handling	18 watts - one atmosphere to hard vacuum
Size (inches)	13.8 Dia x 20.2 L
Weight	2.8 lb, excluding mounting hardware
Temperature	-80" to 64°C

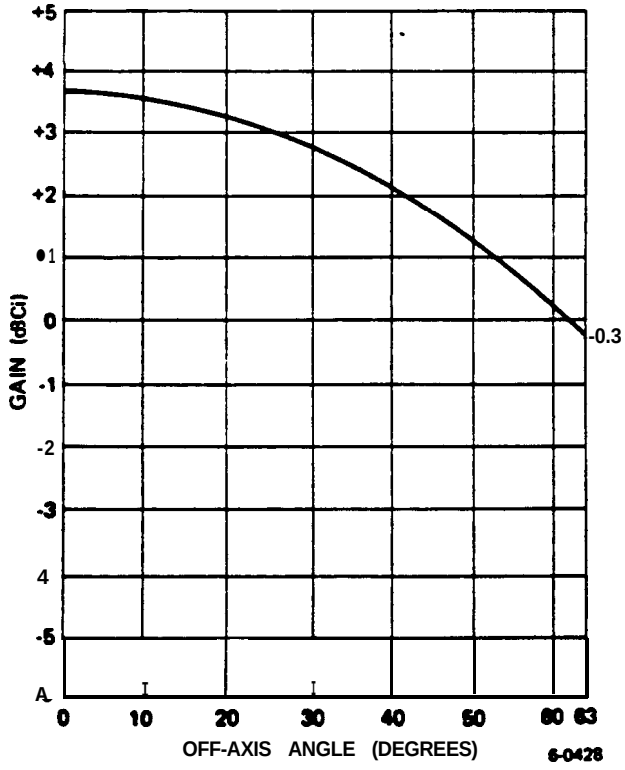
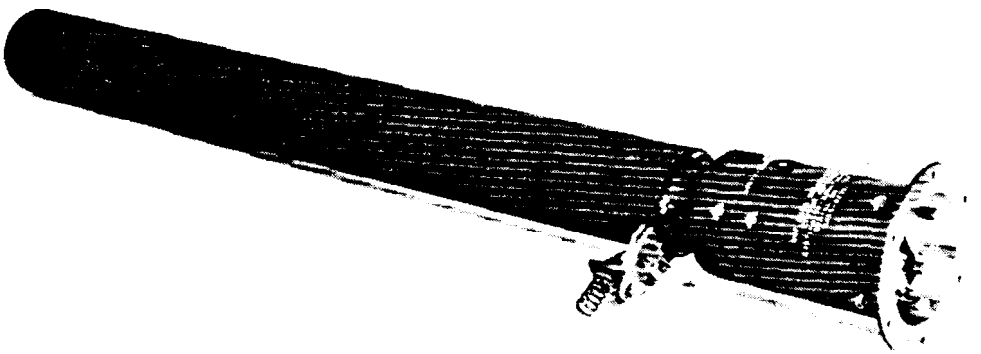


Figure 4.7.2-18. VRA Free-Space Minimum Gain

The feed system consists of a 90" hybrid at the base of the antenna plus two infinite baluns to the feed points located at the apex. Mechanically the VRA is a 90% open structure using fiberglass spreaders and a fiberglass central tube. RG 316 flexible coax inside the fiberglass tube provides the infinite baluns of the feed network. Because of its size, the VRA must be stowed at launch and deployed after arrival to an operational orbit. The antenna provides a right-hand, circularly polarized, cardioid-shaped pattern, with a nominal nose gain (along the nadir) of 4.7 dBci. The nominal gain at 63-degree off the nadir is 0 dBci.

4.7.2.9 UHF Data Collection System Antenna (UDA)

The UDA, designed and built by ASD, is a 1-1/2 turn 1-1/4 wavelength quadrifilar antenna. A photograph of the UDA is shown in Figure 4.7.2-19; the UDA characteristics are summarized in Table 4.7.2-9.



81-1-68C

Figure 4.7.2-19. UHF Data Collection System Antenna

It is composed of a radiating structure and a feed network. The radiating structure consists of four helical elements wound on a thin-walled dielectric tube. Electrically, the UDA is equivalent to the SBA's and thus provides a RHC polarized bifolium pattern with a nominal nadir gain of -2.5 dBci, and a nominal 63-degree, off-nadir gain of +2.5 dBci.

When the elements are excited in phase quadrature by the feed network, the desired bifolium pattern is realized. The UDA output drives both the DCS and the SARP-M via the DCS/SARP-M Diplexer (DPD). Mechanically, the UDA is

TABLE 4.7.2-9. UHF DATA COLLECTION SYSTEM ANTENNA CHARACTERISTICS

Parameter	Value	
	DCS	SARP-M
Frequency	401.65 ±1.0 MHz	406.025 ±1.0 MHz
Polarization	RCP	RCP
Coverage	63' half-angle cone	60" half-angle cone
Ellipticity, Free-Space Measurement	4.5 dB over coverage region 1.5 dB on-axis	Implicit in minimum/ maximum gain characteristics
Gain, Free-Space Measurement	Figure 4.7.2-20A	Figure 4.7.2-20B
Nominal Impedance	50 ohms	50 ohms
VSWR	1.5:1	1.5:1
Size (inches)	3.1 Dia x 36.5 L	
Weight	'2.5 lb	
Temperature:		
• Housing/hybrid network	-75' to +61°C	
• Radiating assembly	-75° to +108°C	

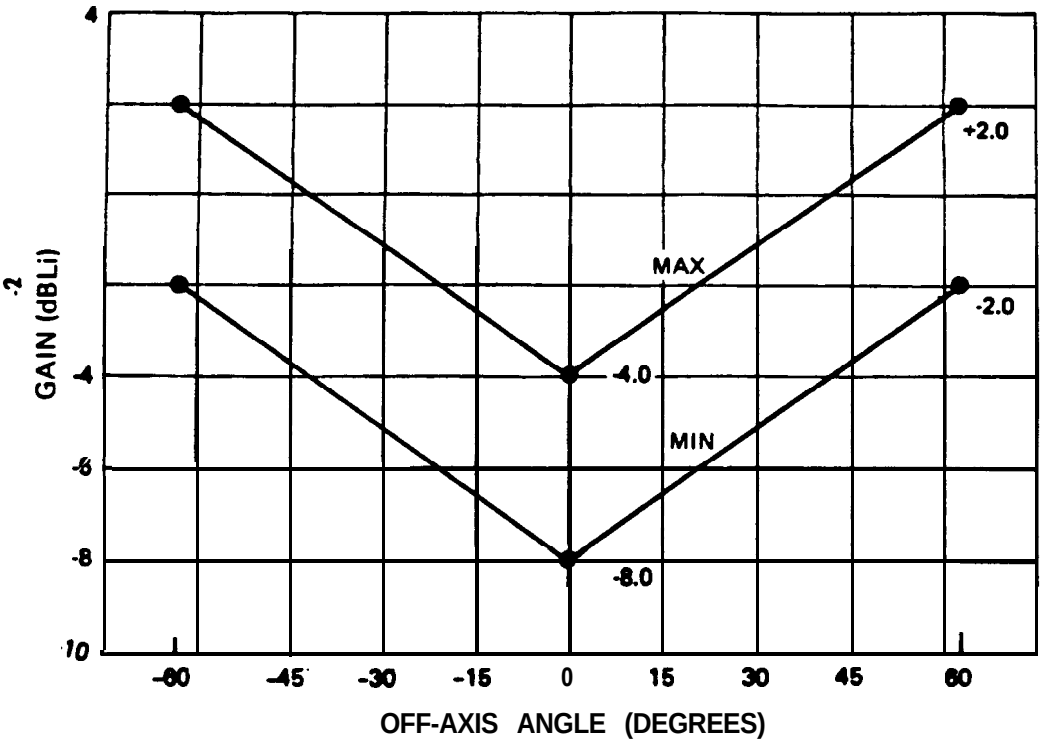
approximately four times the size of the SBA's, as it is designed to operate at 401 MHz and 406 MHz. Because of its large size (36-inch length), the UDA is stowed for launch and deployed after the spacecraft is placed in orbit.

4.7.2.10 VHF Beacon Antenna (BA)

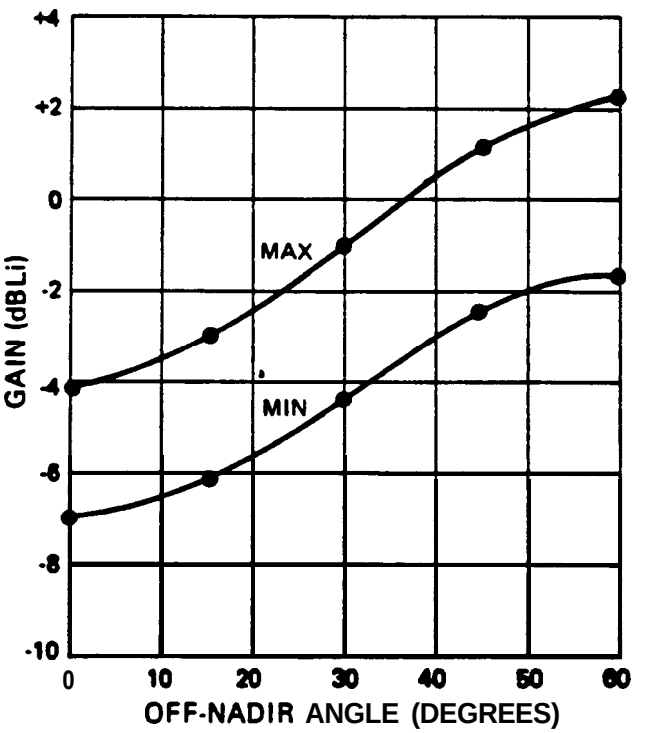
The BA, designed and built by ASD, is a dipole, fixed-mounted parallel to the satellite 2 axis and approximately 1/10 wavelength from Panel No. 1. A photograph of the BA is shown in Figure 4.7.2-21; the BDA characteristics are summarized in Table 4.7.2-10.

The antenna is a balanced dipole resonant at the beacon frequency. The feed network is a 180' hybrid plus two stub transmission lines used to match the antenna element impedance to each output port of the hybrid.

The antenna is double tuned with a choke arrangement and use of a stub in the input line for the final matching trim as shown in Figure 4.7.2-22. The shorted coax sections add series inductance at the beacon frequency. Proper adjustment



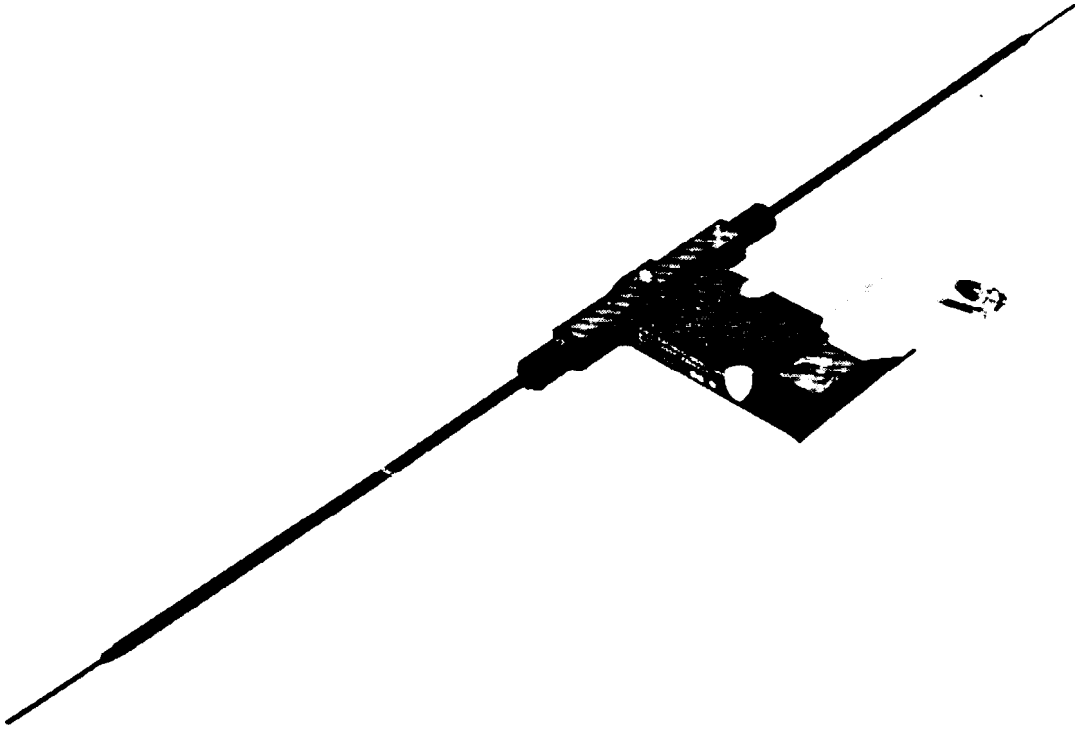
A. AT DCS FREQUENCY



B. AT SARP FREQUENCY

6-0429

Figure 4.7.2-20. UDA Free-Space Minimum and Maximum Gain



81-1-167C

Figure 4.7.2-21. VHF Beacon Antenna

TABLE 4.7.2-10. VHF BEACON ANTENNA CHARACTERISTICS

Parameter	Value
Frequency	137.35, 137.77 (MHZ)
Polarization	Linear
Coverage, Gain	Meaningful only at satellite level since satellite contributes significantly to the pattern
Nominal Impedance	50 ohms
VSWR	1.5:1
Power Handling	1 watt
Dipole Length	42 inches
Weight	1.6 lb, excluding mounting hardware
Temperature	-68" to +67°C

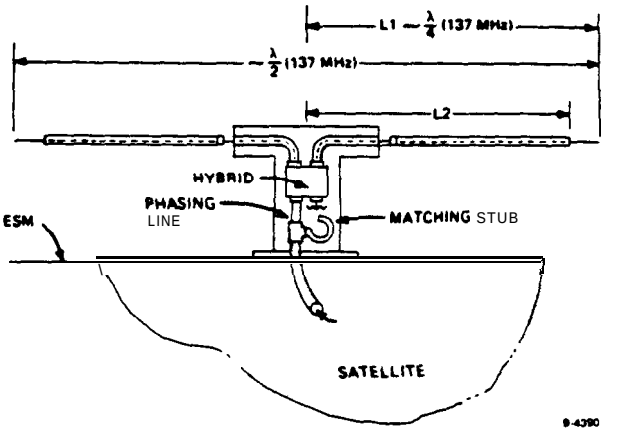


Figure 4.7.2-22. BA Tuning Details

of these three dimensions place the desired resonances at the same impedance which can then be matched with a simple stub.

The antenna is fixed-mounted on the Earth-facing panel of the spacecraft parallel to the long (z) axis of the spacecraft (normal to the orbit plane). This antenna is predominantly linearly polarized within the 63" half-angle cone that covers the Earth. This antenna provides a gain greater then -5dBi when observed with the polarization diversity CDA Beacon Receiver. At the beacon frequencies, this antenna has a gain greater than -14 dBi over 97 percent of 4π steradians.

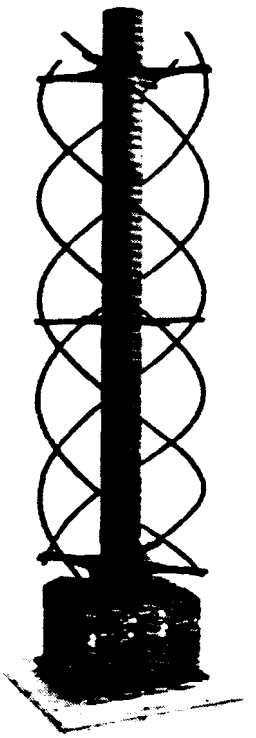
4.7.2.11 Search and Rescue Receiving Antenna (SRA)

The SRA, designed and built by ASD, is a single unit operating with separate outputs at 121.5, 243, and 406.05 MHz. A photograph of the SRA is shown in Figure 4.7.2-23; the SRA characteristics are summarized in Table 4.7.2-11.

The assembly is three antennas in one, each with a pattern of its own. The elements are of the quadrifilar type, wound in a left-hand screw-sense to provide the required right-hand circular polarization sense. The patterns are unidirectional, earth-facing, and shaped to minimize pattern interference due to multipath radiation from other parts of the satellite. The outer element comprises four 1-1/4 turn helices and is top fed and operates at 121.5 and 243 MHz; its construction is of thin-walled brass to provide a rigid, light-weight structure. The inner element comprises four 1-1/2 turn helices and is bottom fed and operates at 406.05 MHz; it consists of gold-plated brass strips bonded to an Astroquartz tube. The box at the base provides a structural attachment and support for the elements and also serves as the housing for the antenna feed components. A schematic of the SRA is presented in Figure 4.7.2-24.

TABLE 4.7.2-11. SEARCH AND RESCUE RECEIVING ANTENNA CHARACTERISTICS

Parameter	Value		
Frequency	121.5 MHz	243 MHz	406.05 MHz
	121.5 ±0.5 MHz	243 ±0.5 MHz	406.05 ±0.5 MHz
Polarization	RCP	RCP	RCP
Coverage	60' half-angle cone	60" half-angle cone	60" half-angle cone
Ellipticity, Free Space Measurement	Implicit in gain characteristics	Implicit in gain characteristics	Implicit in gain characteristics
Gain, Free-Space Measurement	Figure 4.7.2-256	Figure 4.7.2-25B	Figure 4.7.2-25C
Nominal Impedance	50 ohms	50 ohms	50 ohms
VSWR	1.6:1	1.6:1	1.6:1
Weight	14.0 pounds, excluding boom and mounting hardware		
Temperature	-95" to + 67°C except for hybrid box -80 to + 80°C hybrid box		



81-4-79C

Figure 4.7.2-23. Search and Rescue Receiving Antenna

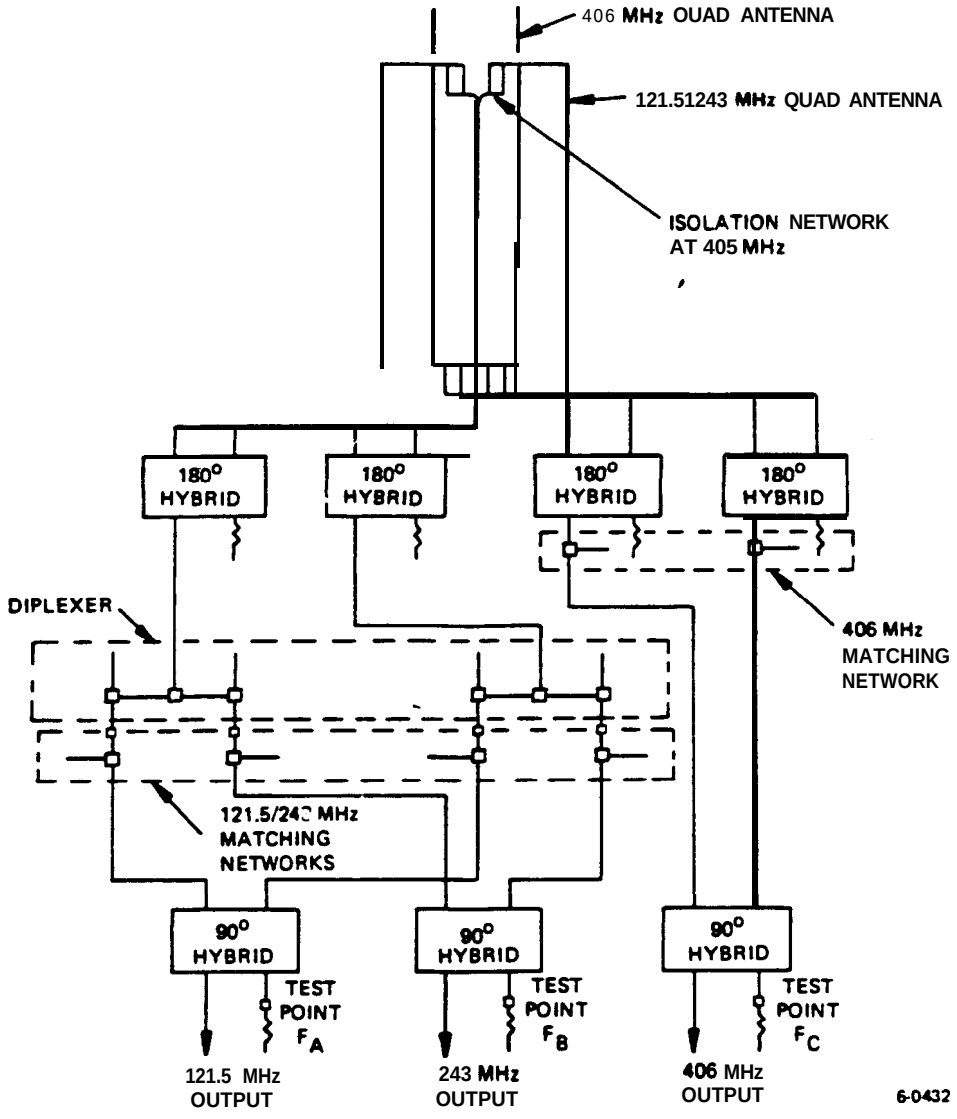


Figure 4.7.2-24. SRA Block Diagram

A quadtifilat antenna consists of a pair of bifilar antennas orthogonally displaced on a common axis and fed 90' with respect to each other. The components required to feed the bifilars are 180° hybrids. Quadrature (90°) hybrids are used to feed the pairs of bifilars. The two-frequency operation of the outer element is made possible by use of a diplexer. Matching networks where needed are provided at the inputs of the diplexer and the 406-MHz, 180' hybrids.

Because of its size, the SRA is stowed at launch and deployed after arrival in operational orbit.

4.7.2.12 Search and Rescue L-Band Antenna (SLA)

The SLA, designed and built by ASD, is a resonant, 1-1/2 turn quadrifilar helix fed by an infinite balun. A photograph of the SLA is shown in Figure 4.7.2-26; the SLA characteristics are summarized in Table 4.7.2-12. The

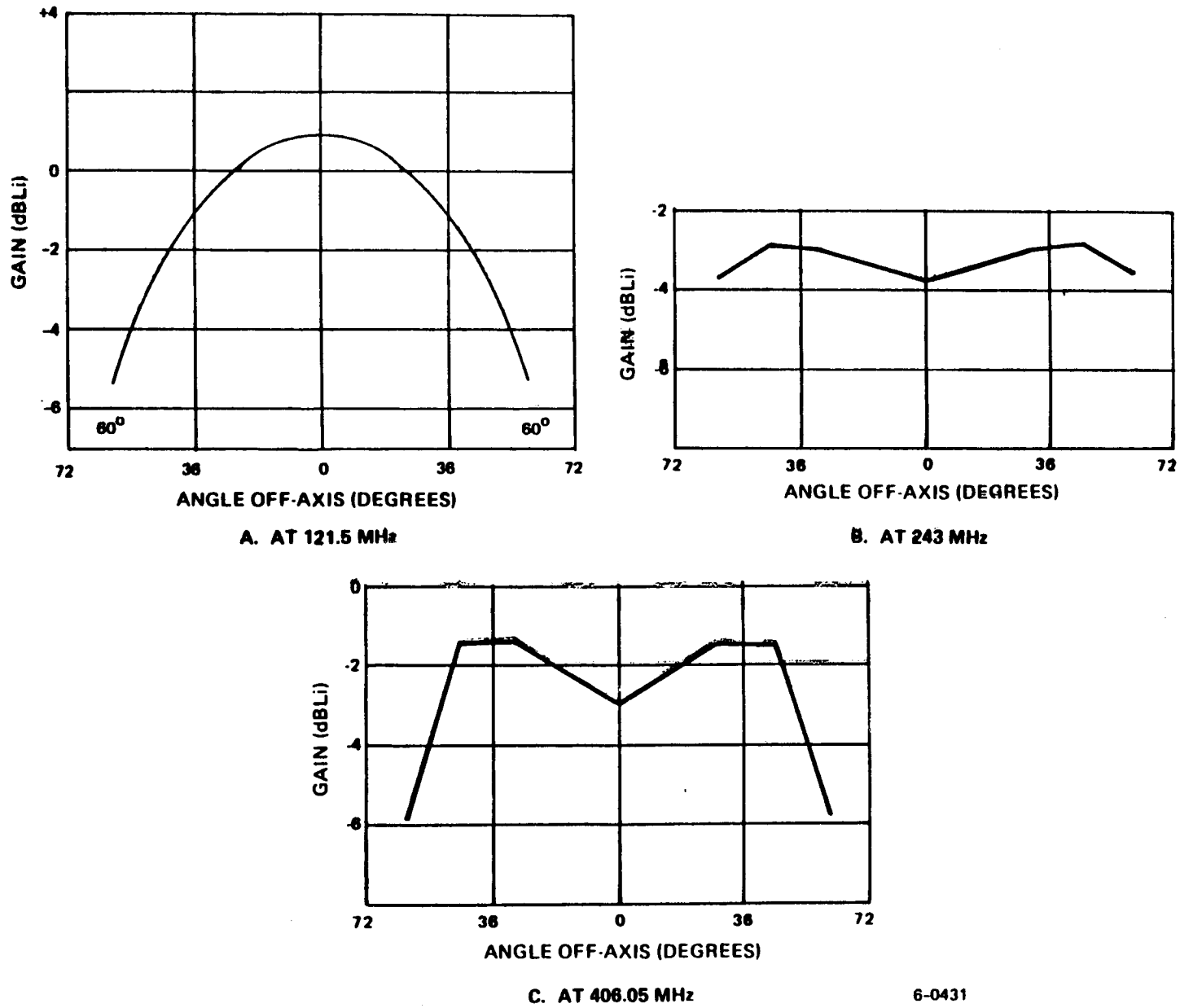
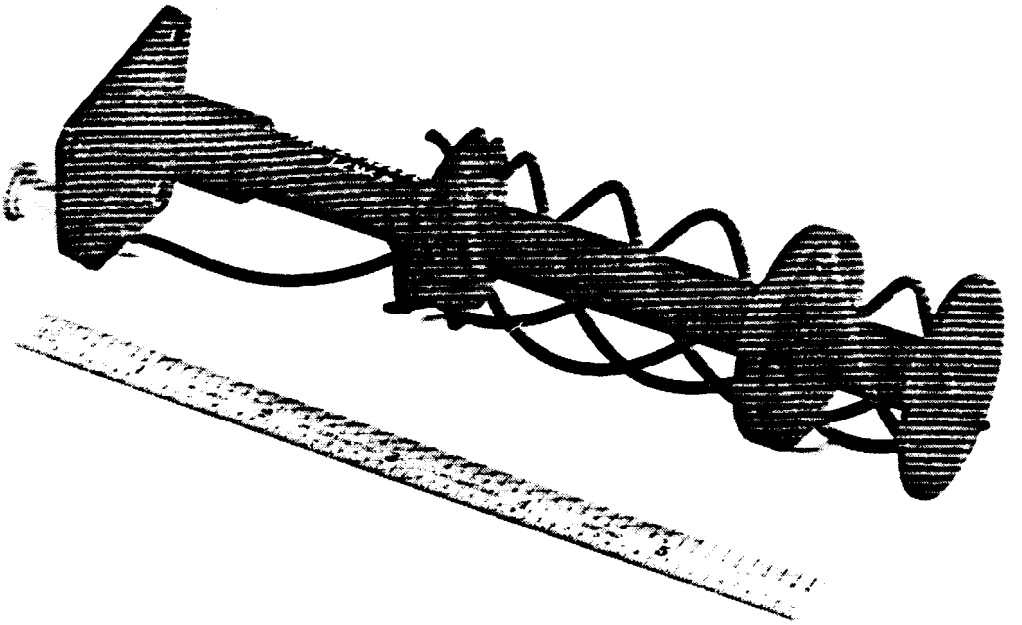


Figure 4.7.2-25. SRA Free-Space Minimum Gain



82-12-50C

Figure 4.7.2-26. Search and Rescue L-Band Antenna

TABLE 4.7.2-12. SEARCH AND RESCUE L-BAND ANTENNA CHARACTERISTICS

Parameter	Value
Frequency	1544.5 ±1 MHZ
Polarization	LCP
Coverage	60" half-angle cone
Ellipticity, Free-Space Measurement	4.5 dB in coverage region
Gain, Free-Space Measurement	Figure 4.7.2-27
Nominal Impedance	50 ohms
VSWR	1.5:1
Weight	0.7 lb, excluding mounting hardware
Temperature	-104" to +64°C

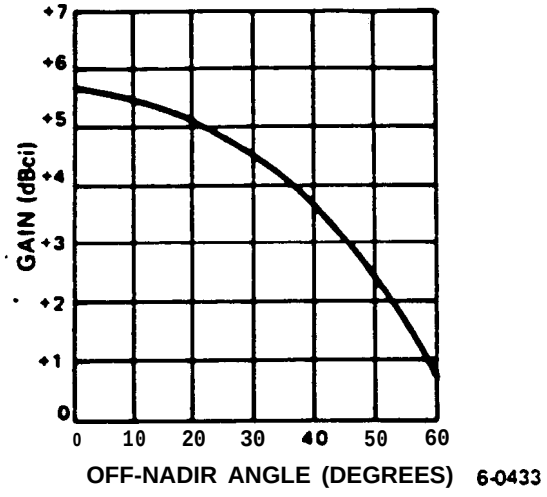


Figure 4.7.2-27. SLA Free-Space Minimum Gain

antenna comprises four helically wound wires which form a cylinder 0.14 wavelength in diameter and 0.56 wavelength long. As in the other quadrifilar antennas in ATN-K,L,M, it is two bifilar helices fed in phase quadrature. In this case as in the SOA, one of the four windings constitutes an infinite balun by making that winding a helical extension of the semi-rigid coax feedline. The feedpoint for all the helices is at the "top" or free end of the SLA. The-center conductor of the feedline feeds two of the other windings connected together at the feed point. Transmission-line current flowing on the inner surface of the feedline outer conductor flows around the end of the conductor.

This current becomes the radiating antenna current as it continues its flow on the outside of the feedline winding as well as along the fourth winding connected to the outer conductor at the feed-point. The four helices are self-phased like those of the SBA.

4.7.2.13 RF Components

4.7.2.13.1 RF Filters

The satellite requires nine RF filters. The characteristics of the filters are summarized in Table 4.7.2-13.

TABLE 4.7.2-13. RF FILTERS - CHARACTERISTICS

Filter	Purpose	Baseline Supplier	Baseline Design	Outline Drawing	Attenuation Requirements
RFF-1	Control spectrum of BTX-1, -2; VTX-1, -2	Wavecom	Tuned to 136-139 MHz and incorporates a notch at 120-123 MHz. Additional rejection at 240-246 MHz and 396-411 MHz and 1655-1725 MHz for SARR and Radio Astronomy Protection.	Figure 4.7.2-28	Figure 4.7.2-29
RFF-2	Protect DCS	Wavecom	S-resonator combline (0.01-dB Chebishev) bandpass, plus an ll-section coaxial transmission line low-pass with l-GHz cutoff	Figure 4.7.2-30	Figure 4.7.2-31
RFF-3	Protect SARP-M and SARR 406.05 MHz	Wavecom	Same design as RFF-2; bandpass tuned to center on SARP-M/SARR-406.05 MHz	Figure 4.7.2-30	Figure 4.7.2-32
RFF-4	Protect SARR 243 MHz	Wavecom	3-resonator combline	Figure 4.7.2-33	Figure 4.7.2-34
RFF-5	Protect SARR 121.5 MHz	Wavecom	Frequency-selective low-pass with g-element elliptic-like design with the poles in the 136-138 MHz stopband notch	Figure 4.7.2-35	Figure 4.7.2-36

TABLE 4.7.2-13. RF FILTERS - CHARACTERISTICS (Continued)

Filter	Purpose	Baseline Supplier	Baseline Design	Outline Drawing	Attenuation Requirements
DPD	Split the composite output from the UDA into 401.65 output to DCS and 406.025 output to SARP-M	Wavecom	Two resonators in each receiver channel; lightly loaded combline configuration; coupling between resonators by printed circuit	Figure 4.7.2-37	Table 4.7.2-14
GFN	Protect GRD	K & L Microwave	Two bandpass filters connected to the antenna port.	Figure 4.7.2-38	Figure 4.7.2-39

4.7.2.13.2 RF Switch

A photograph of the RF switch is shown in Figure 4.7.2-40; the RF Switch characteristics are summarized in Table 4.7.2-15.

The RF Switch, designed and manufactured by Transco Products, Inc., is a standard mechanical design with the addition of a telemetry switch-position-indicating resistor network. The switch is SPDT and is a "fail safe" design; that is, it requires holding power in only one direction and when this power is removed, the switch is pulled back into the other position. In the S-Band application, this switch receives holding power from the SCU; in the BTX and VTX applications, it receives power from the number 1 transmitter of the pair. Thus, an ON command to BTX-1 activates the associated RF Switch and an OFF command to BTX-1 deactivates it. The RF Switch associated with the VTX works in a similar fashion.

4.7.2.13.3 Antenna Hybrid

The STX-4s SOA-3, -4 are fed via the antenna hybrid which is a four port power splitter. The input power is split into two half power output ports which have 90' phase difference and the fourth port is terminated in a 50 ohm load. Table 4.7.2-16 summarizes the hybrid characteristics.

4.7.2.13.4 RF Cabling

Signal interconnections between RF components are achieved by using low-loss coaxial cable. Flexco F242 and F342 cables are used which are flexible and have teflon spline dielectric construction.

Thirty-seven cables are required to interconnect the RF components. The cable baseline for this proposal is manufactured by Flexco Microwave, Inc. Additional cabling required within antenna assemblies or around the antenna deployment hinges for VRA, UDA, and SRA is assembled by ASD. All cables and RF components use SMA connectors. The characteristics of the cables are given in Table 4.7.2-17.

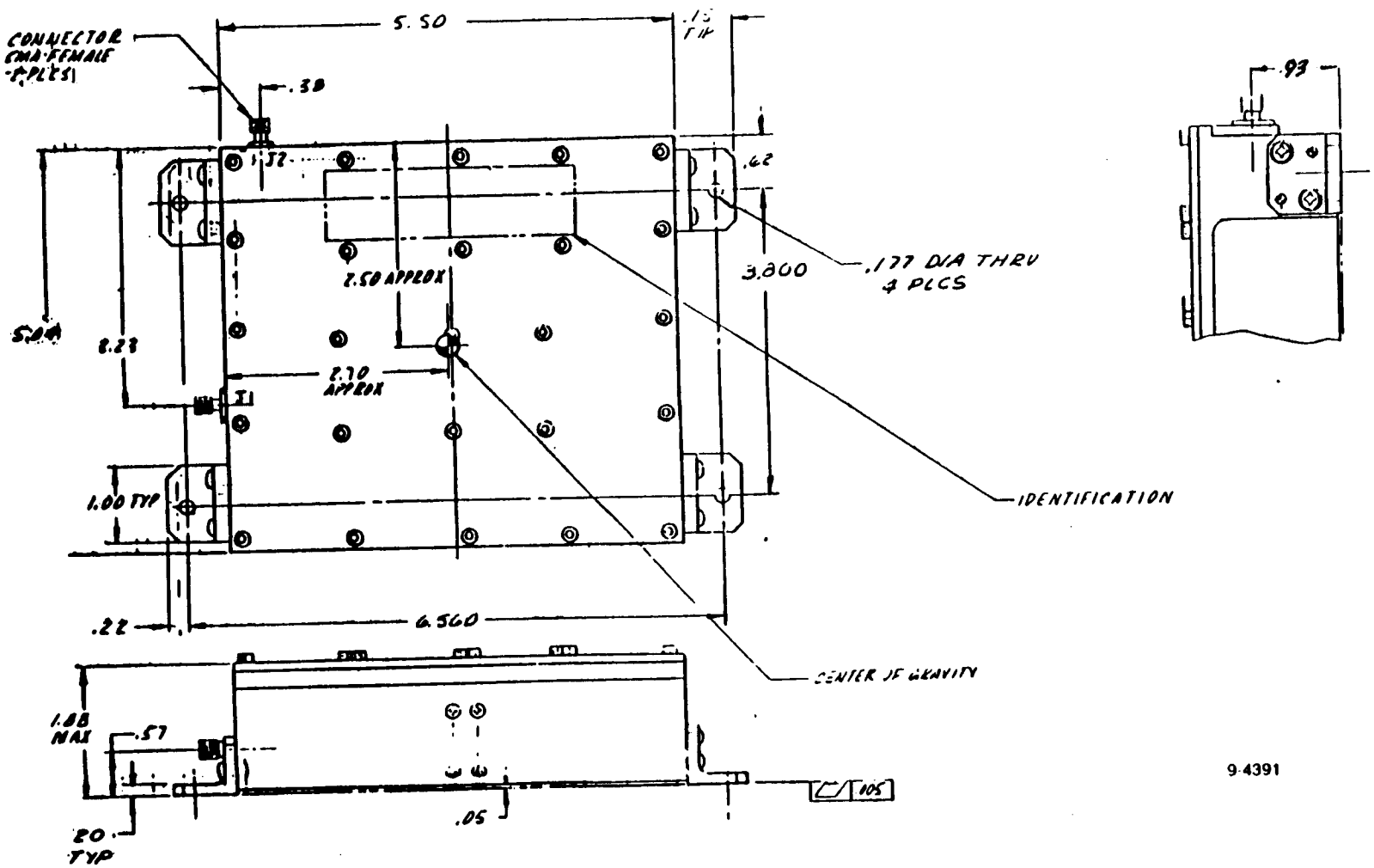


Figure 4.7.2-28. RF Filter RFF-1 Outline Drawing

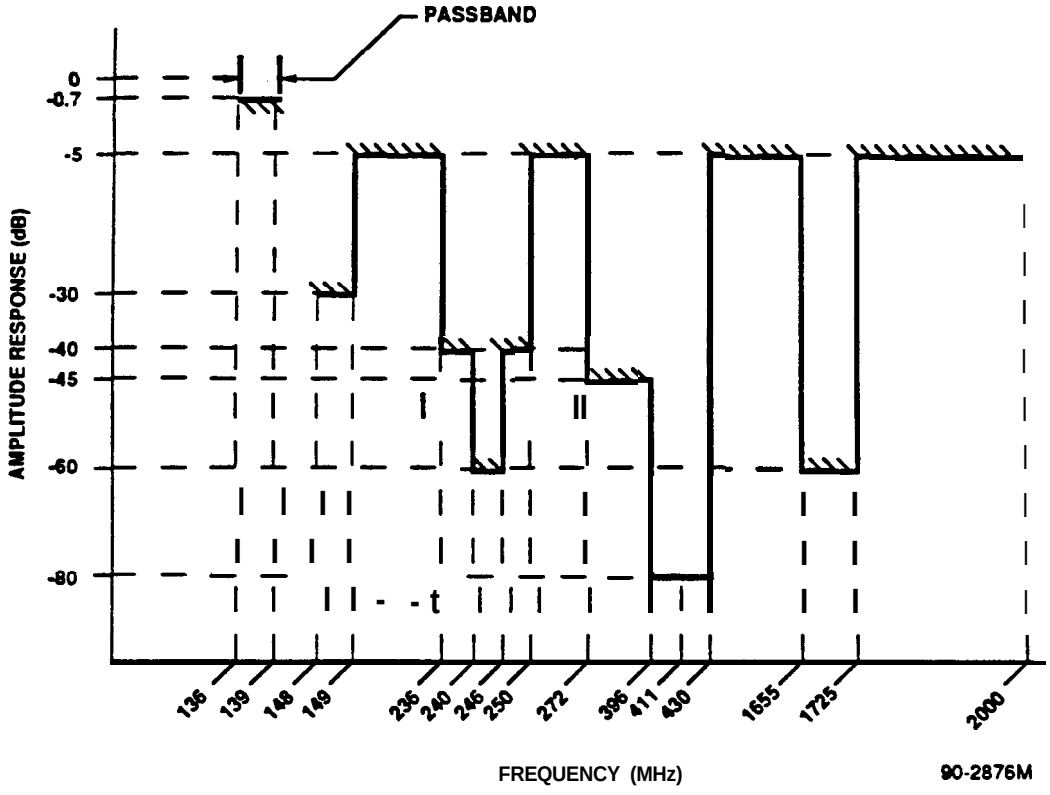


Figure 4.7.2-29. RF Filter RFF-1 Attenuation Characteristics

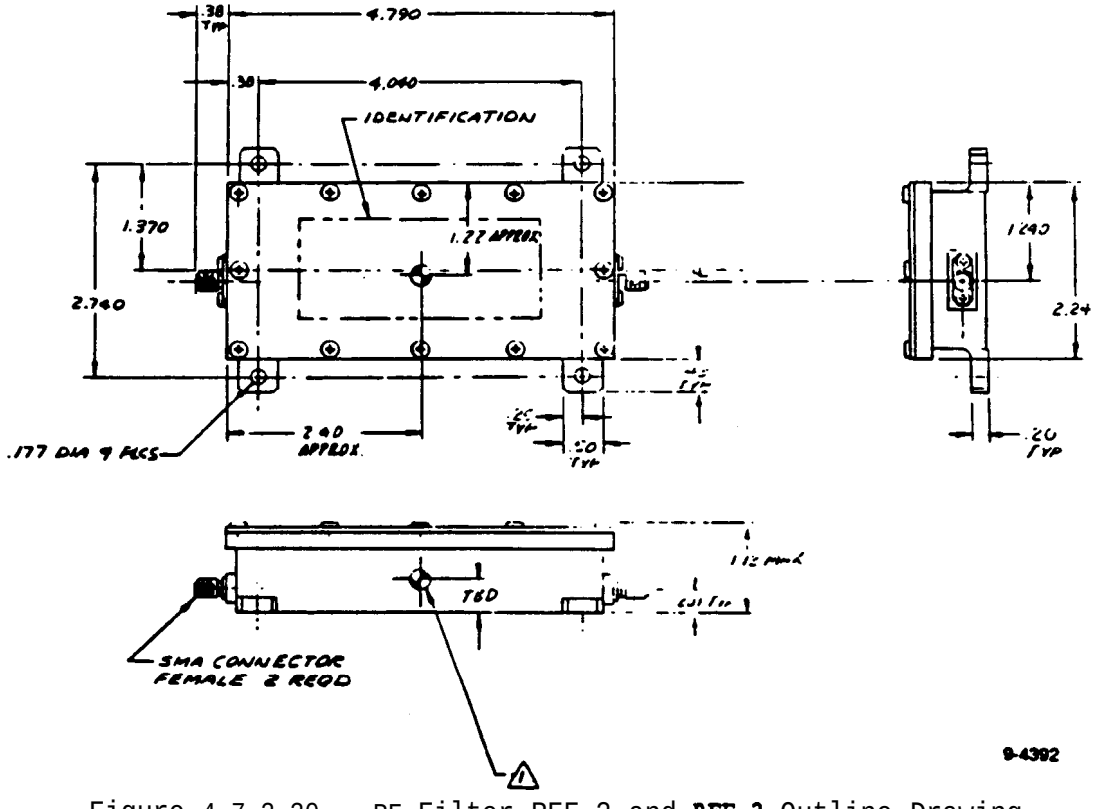


Figure 4.7.2-30. RF Filter RFF-2 and **RFF-3** Outline Drawing

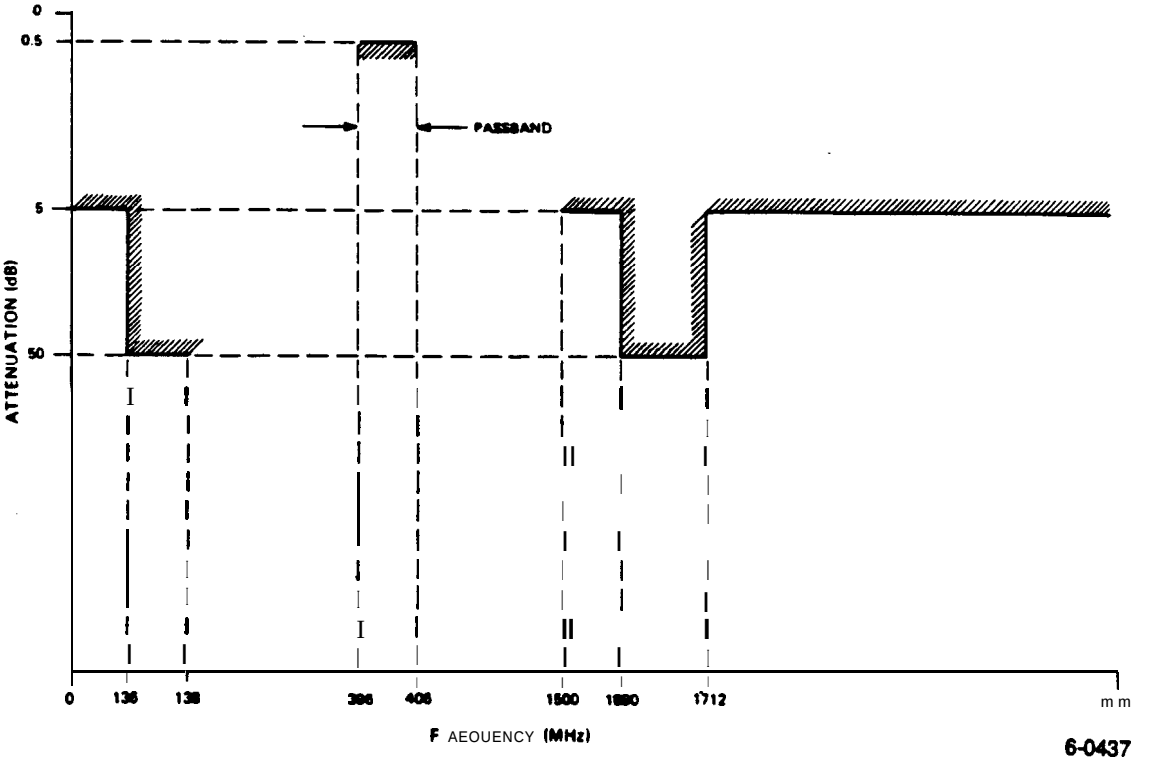


Figure 4.7.2-31. RF Filter RFF-2 Attenuation Characteristics

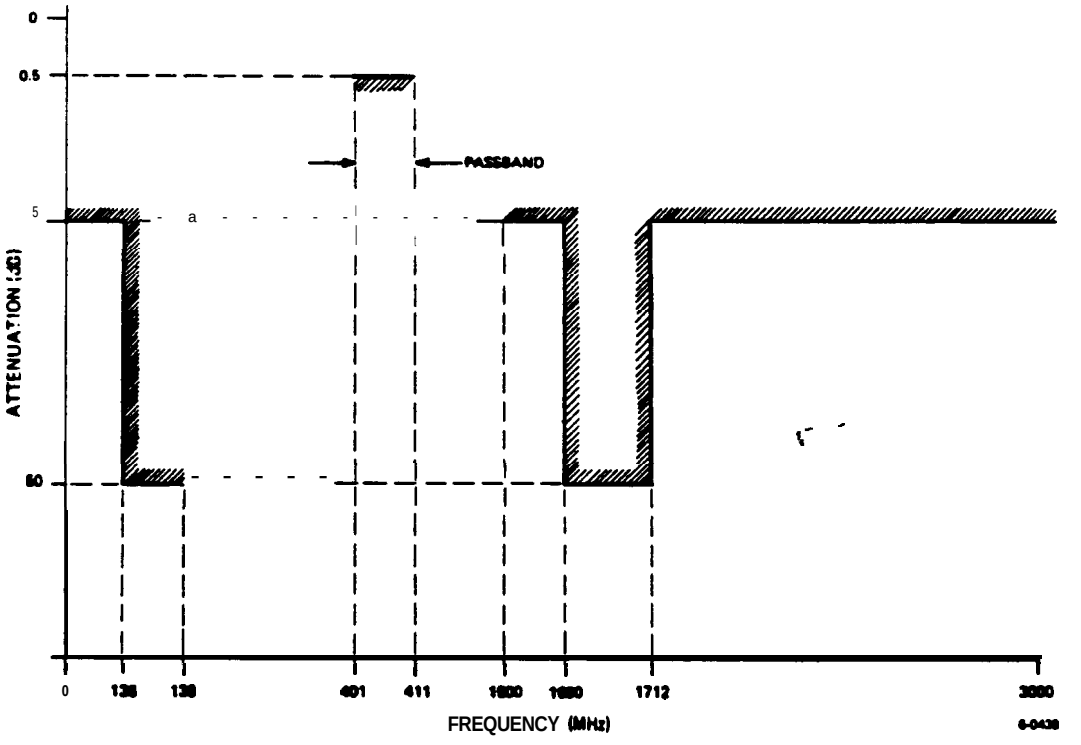


Figure 4.7.2-32. RF Filter RFF-3 Attenuation Characteristics

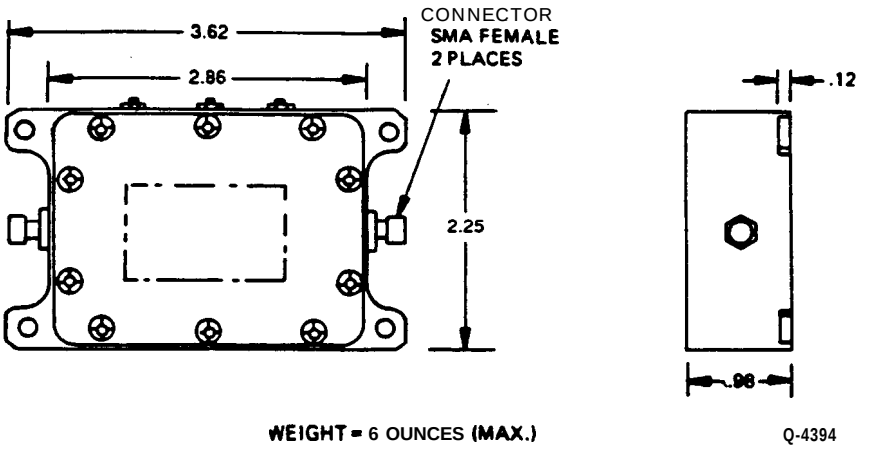


Figure 4.7.2-33. RF Filter RFF-4 Outline Drawing

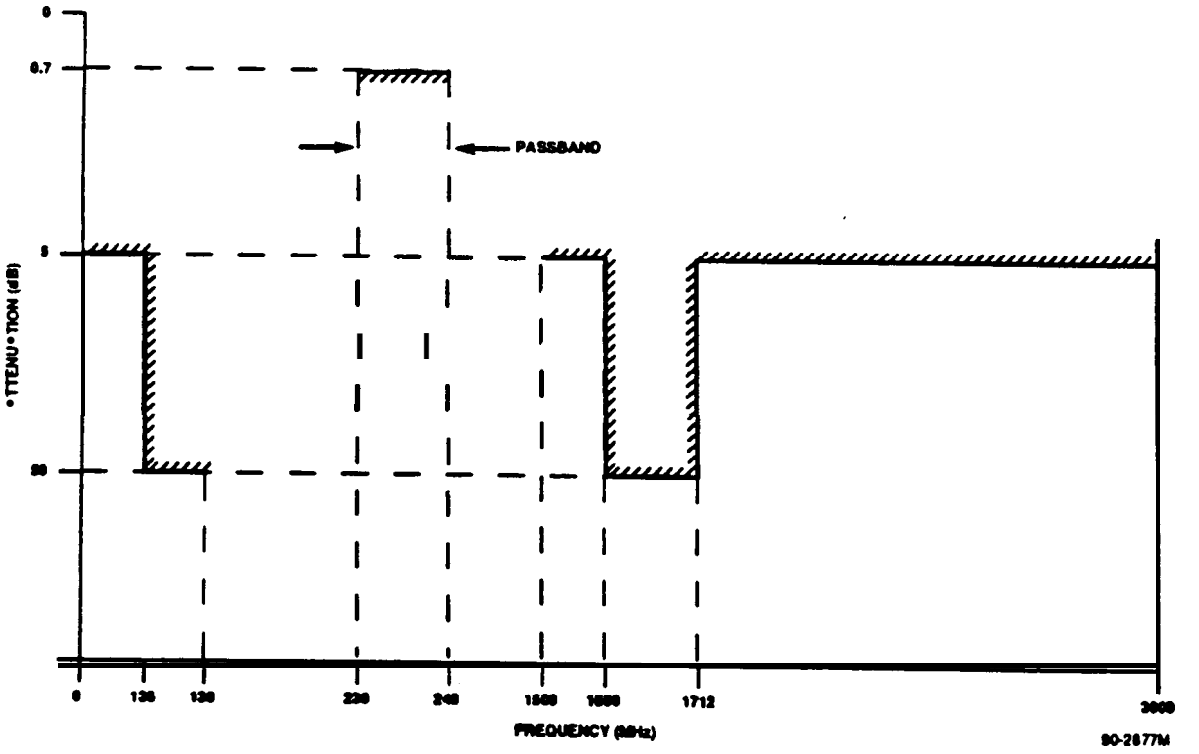


Figure 4.7.2-34. RF Filter RFF-4 Attenuation Characteristics

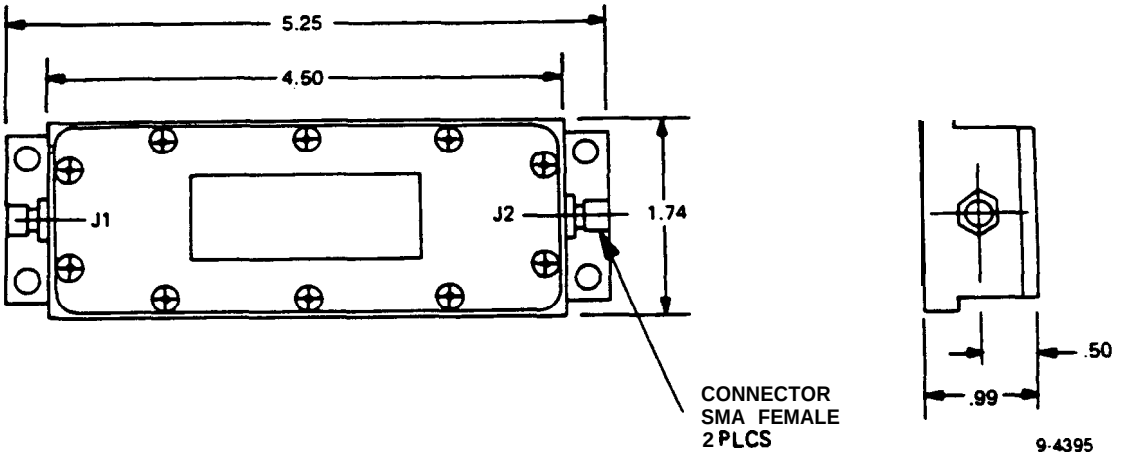


Figure 4.7.2-35. RF Filter RFF-5 Outline Drawing

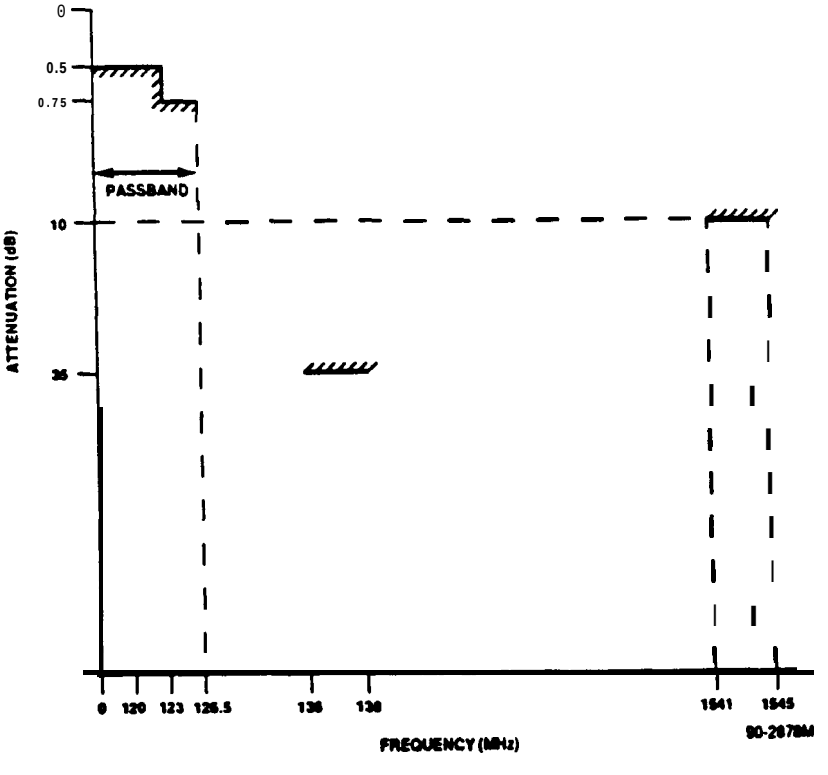


Figure 4.7.2-36. RF Filter RFF-5 Attenuation Characteristics

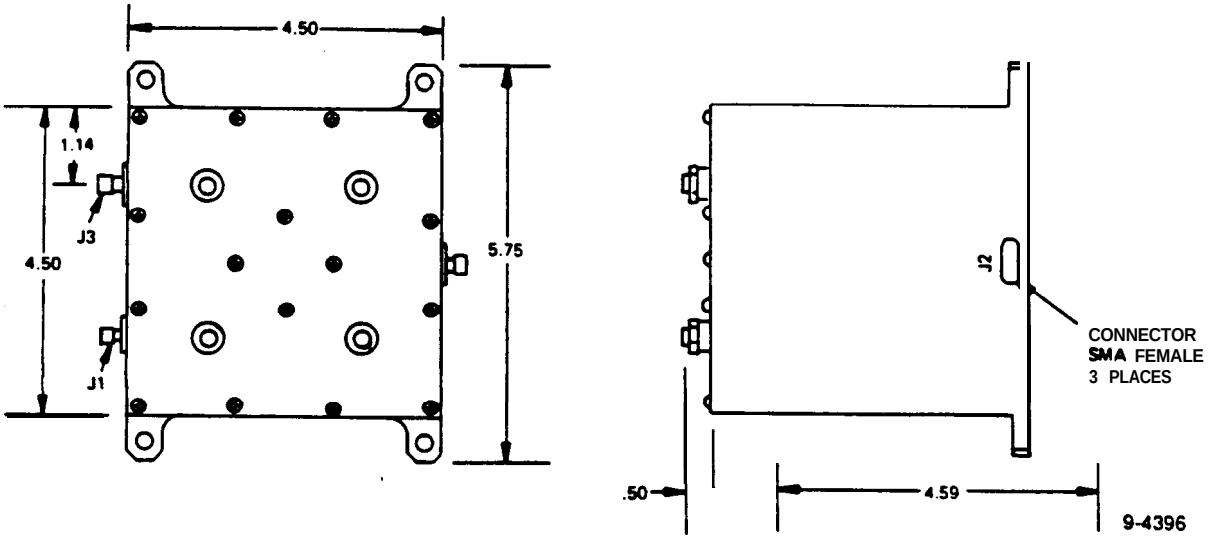


Figure 4.7.2-37. DCS/SARP-M Diplexer Outline Drawing

TABLE 4.7.2-14. DCS/SARP-M DIPLEXER ATTENUATION CHARACTERISTICS

Port 1	Port 2	Frequency	Loss
DCS	UDA	401.15 to 402.15 MHz	0.5 dB (max)
SARP-M	UDA	405.55 to 406.55 MHz	0.5 dB (max)
DCS	SARP-M	Both above bands	25 dB (min)

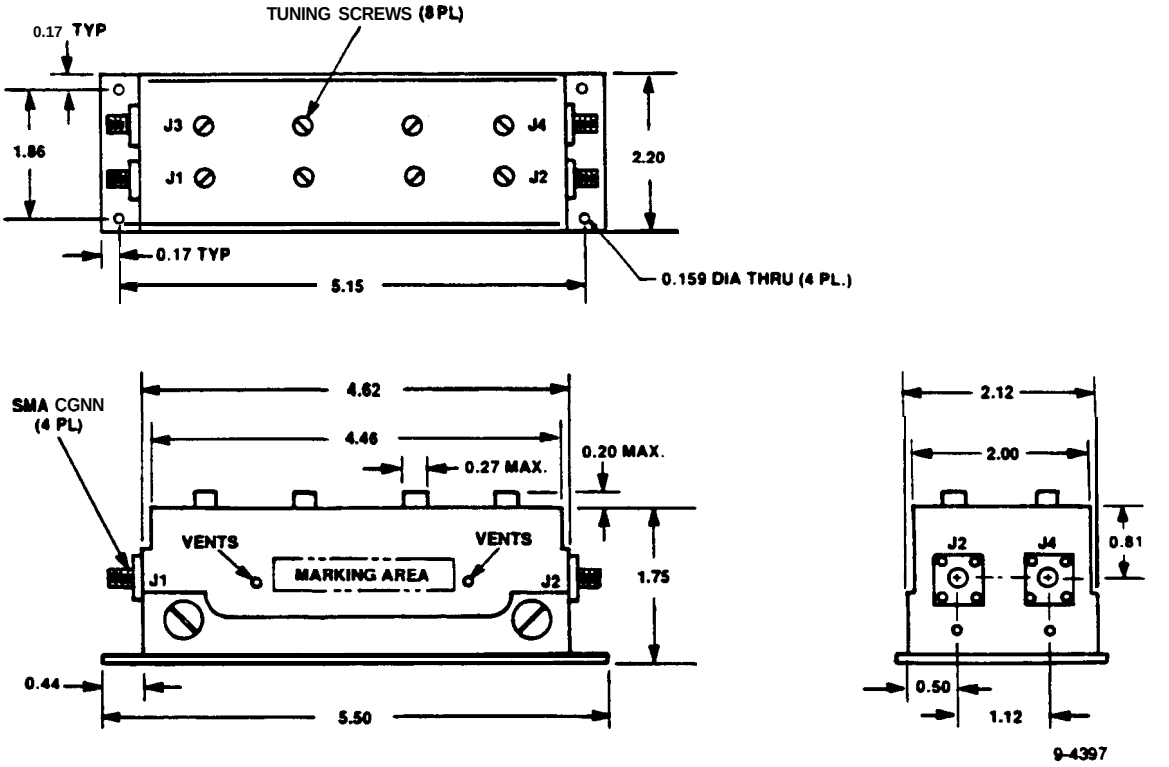


Figure 4.7.2-38. GFN Outline Drawing

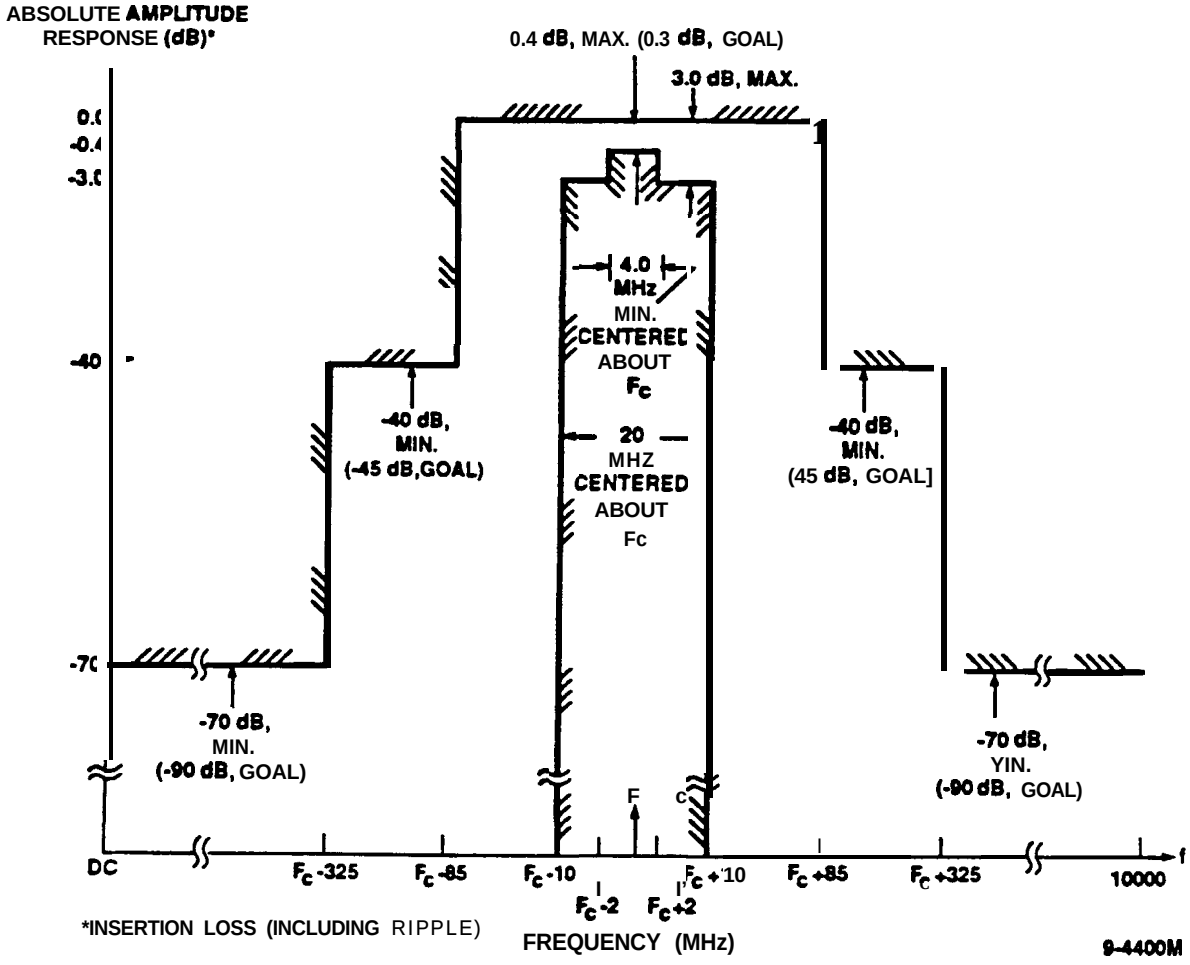


Figure 4.7.2-39. GFN Absolute Response vs. Frequency

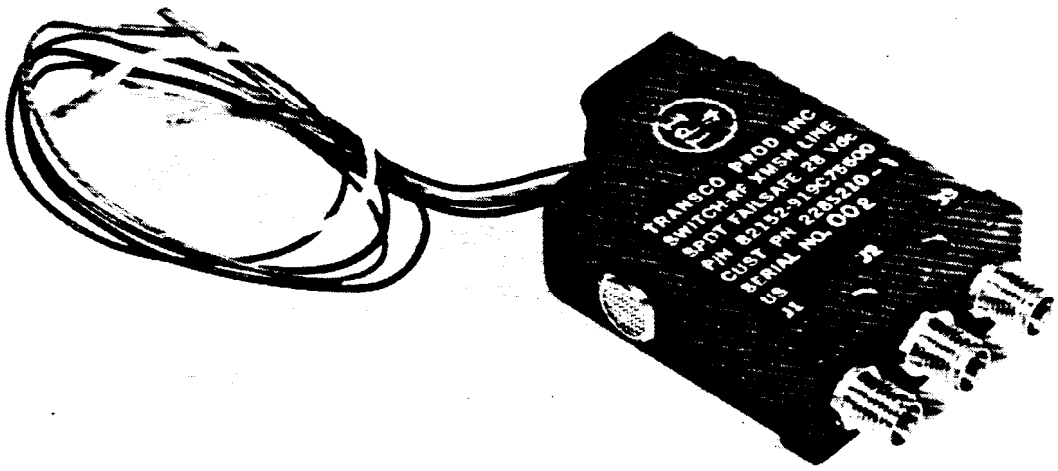


Figure 4.7.2-40. RF Switch

77-4-83C

TABLE 4.7.2-15. RF SWITCH CHARACTERISTICS

Parameter	Required Value
Frequency	100 to 2500 MHz
Impedance, VSWR any port	50 ohms nominal, Maximum VSWR = 1.2:1 with other ports terminated in 50 ohms
Insertion Loss	0.2 dB, Maximum, between J2 and J1/J3
Isolation	80 dB , Minimum, between J1 and J3
Power Handling	16 watts, CW
Size	1.34 x 1.15 x 0.5 inches
Weight, Maximum	3 ounces
Type of RF Contacts	Break before make
Type of Relay	Failsafe
Coil Control Voltage	20 to 30 Vdc
Pull-in Current (@28 Vdc)	0.12 A Maximum
Hold-in Current (@28 Vdc)	0.036 A Maximum
Switching Time	20 milliseconds, Maximum

TABLE 4.7.2-16. ANTENNA HYBRID CHARACTERISTICS

Parameter	Value
Frequency	2000 to 2300 MHz
Impedance, VSWR by port	50 ohms nominal, Maximum VSWR 1.2:1 with other ports terminated in 50 ohms
Insertion Loss	0.3 dB maximum from port 1 to ports 2 and 3 and from port 4 to ports 2 and 3, 20 dB minimum between ports 2 and 3 and between ports 1 and 4
Phase	90' ±2.0° between ports 2 and 3
Amplitude Imbalance	0.6 dB maximum between ports 2 and 3
Power	10 watts CW maximum
Weight	Less than 1 oz

TABLE 4.7.2-17. RF CABLE CHARACTERISTICS

Parameter	F242 Cable	F342 Cable
Calculated Loss at		
S-Band	0.13 dB/ft	0.13 dB/ft
VHF	0.035 dB/ft	0.027 dB/ft
UHF	0.057 dB/ft	0.048 dB/ft
Weight	0.064 lb/ft	0.080 lb/ft
Outer Conductor, Soldered Strip Wound	0.330 inch O.D.	0.395 inch O.D.
Minimum Bend Radius	1.00 inch	1.50 inches
Nominal Impedance	50 ohms	50 ohms
Temperature Range	-55°C to +200°C	-55°C to +200°C

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4.8 DATA HANDLING SUBSYSTEM

4.8.1 DATA HANDLING SUBSYSTEM DESCRIPTION

4.8.1.1 Subsystem Functions

The Data Handling Subsystem (DHS) collects and processes data from all on-board meteorological sensors, as well as collecting all housekeeping telemetry for transmission to the ground. Data processing includes formatting, resolution reduction, and geometric correction. The subsystem provides data outputs in real time, as well as playback of recorded data.

4.8.1.2 Component Functions

The DHS consists of the following components:

(a) One Dual TIROS Information Processor (TIP). The TIP formats all downlink data except that from AVHRR, the SARP, and the SARR. The TIP provides synchronization signals to the HIRS, SEM, and the SBW.

(b) One dual AMSU Information Processor (AIP). The AIP accepts data from, and provides synchronization signals to, the three AMSU instrument units. The AIP also accepts TIP data and outputs either AIP (AMSU and TIP) data or just TIP data to the XSU. The AMSU data is also output to the MIRP.

(c) One Manipulated Information Rate Processor (MIRP). The MIRP process and formats all data from the AVHRR. It produces four output formats simultaneously, a11 of which include AVHRR data. Three of the formats include TIP and AIP data.

(d) Five Dual Transport Digital Tape Recorders (DTRs). The DTRs record and play back TIP and MIRP output data.

(e) One Cross Strap Unit (XSU). The XSU switches data streams between other DHS components and four S-Band Transmitters (STXs). It provides clocks to DHS components and to the HIRS, AMSU, SEM, and SBW.

The functional flow of the DHS is depicted in Figure 4.8.1-1.

4.8.1.2.1 TIP

The TIP formats all downlink data except for that from the AVHRR, the SARP, the AMSU, and the SARR. It provides synchronization signals to the HIRS, SBW, and SEM, controls their data outputs, and accepts command verification data and housekeeping telemetry. It adds synchronization identification and time code, and outputs the data to the MIRP and the AIP. The TIP multiplexes instrument data signals and status telemetry into one 8320 bps signal (orbit mode) or 16,640 bps signal (boost mode). Low rate instrument data, housekeeping telemetry, and CPU data are inputs to the TIP. This data is time division multiplexed into a format determined by a stored program in a ROM within the TIP. The TIP can operate in any of four modes: orbit mode, boost mode, dwell mode, and dump mode.

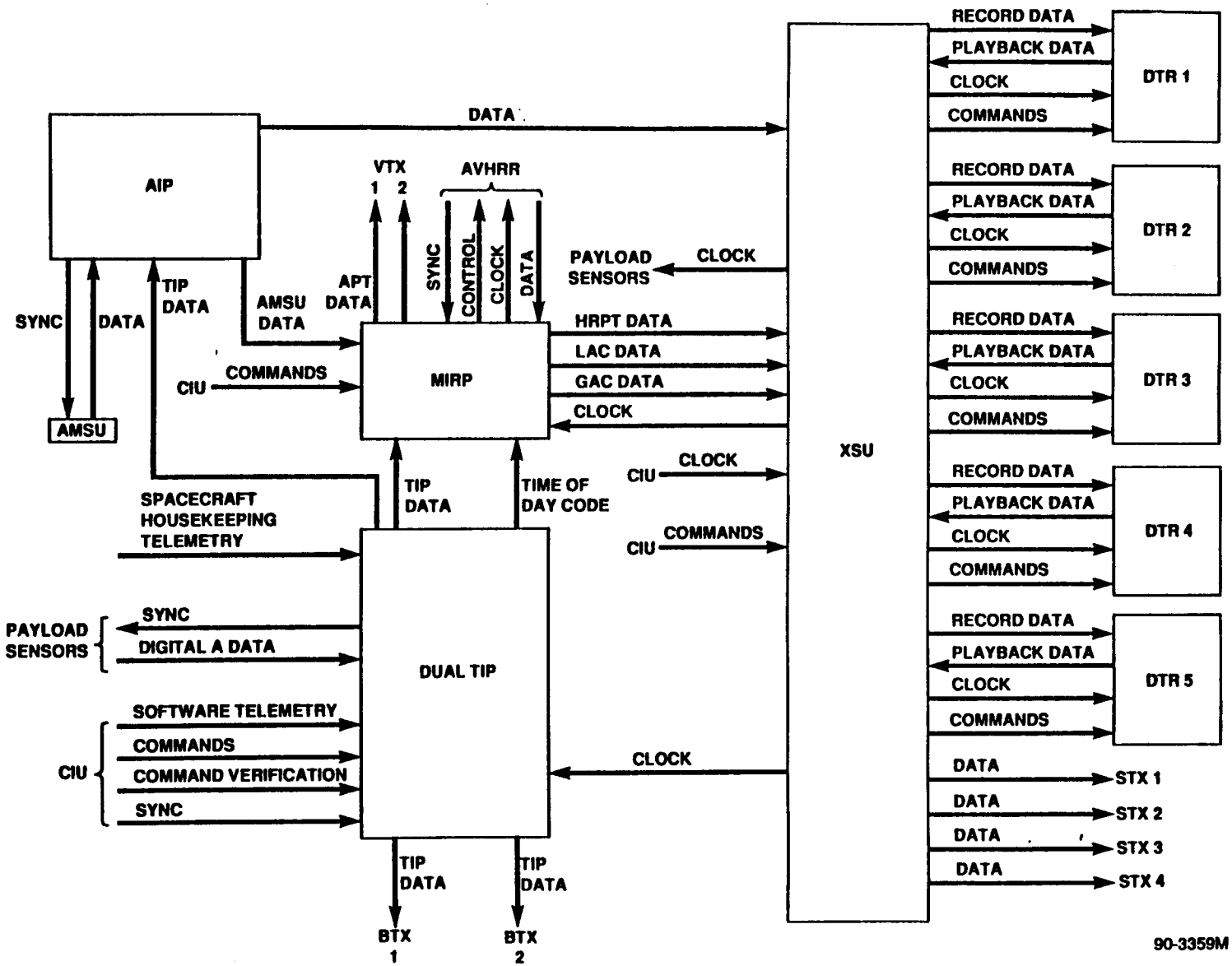


Figure 4.8.1-1. Data Handling Subsystem, Functional View

In orbit mode the TIP provides header information, command verification, CPU A & B software telemetry, payload sensor data, and housekeeping telemetry data. In boost mode the TIP provides header information, CPU A & B software telemetry, and other housekeeping telemetry data (at high rate) to the XSU via the AIP. In dwell mode the TIP provides header information, command verification, and a single channel of digitized analog housekeeping telemetry which is selected by command. In dump mode the TIP provides a modified mission mode format: all CPU A & B word locations are dedicated to either CPU A dump data or CPU B dump data.

The TIP output data stream is directed to: the beacon link, for continuous real time transmission; the digital recorders during multiple blind orbits, for playback to a ground station in Europe; and the MIRP, for multiplexing with the AVHRR data. The TIP outputs serial digital words, most significant bits first. The rates and lengths are as follows:

Bit Rate	16,640 bps	8320 bps
Word Length	8 Bits	8 Bits
Minor Frame Length	104 words (0.05 sec)	104 words (0.1 sec)
Major Frame Length	320 minor frames (16 seconds)	320 minor frames (32 seconds)

The first minor frame in each major frame contains time code instead of housekeeping telemetry, The housekeeping telemetry words are distributed in a major frame as follows: '

Data Type	3.2-Sec Digital B Subcom-l Word	32-Sec Analog Subcom Word	16-Sec Analog Subcom-l Word	1-See Analog Subcom Word	3.2-Sec Digital B Subcom-2 Word	16-Sec Analog Subcom-2 Word
Type of Data in each Word in one Minor Frame	Eight Bilevel Status Channels	One Digitized Analog Channel	One Digitized Analog Channel	One Digitized Analog Channel	Four Bilevel Status Channels	One Digitized Analog Channel
Repetition Period of Subcom, minor frames	32	320	160	10	32	160

There are 352 discrete (bilevel) telemetry points. This subcom repeats at a 3.2 second rate in Orbit Mode, and 1.6-second rate in Boost Mode. The TIP multiplexes these inputs into 8-bit words.

The 32-Second Analog Subcom format contains 320 word locations. It repeats every 16 seconds in the TIP Boost Mode and every 32 seconds in all other TIP Modes. There are 256 analog telemetry inputs available to the 32-Second Analog Subcom; each is assigned a unique analog telemetry channel number (0-255). 191 channels are sampled once each per repetition of the 32-Second Analog Subcom (i.e., once per major frame); 64 channels are sampled twice each subcom; channel zero is displayed only if addressed by TIP Mode command data word for display in the l-Second Analog Subcom or for monitoring in Dwell Mode. The TIP multiplexes these analog inputs together.

There are two TIP words for 16-second subcom data. In the first subcom there are 112 analog telemetry channels. Since there are 160 word locations, some of the channels are assigned to more than one location. The second subcom contains 128 channels. The remaining 32 words are SATCU telemetry. These subcoms repeat every 8 seconds in TIP boost mode and every 16 seconds in all other TIP modes. The TIP multiplexes analog inputs together, and is configured such that a single multiplexer gate failure will not affect more than 8 channels.

There are 10 word locations in the 1 second analog subcom. It repeats twice a second in TIP Boost Mode and once a second in all other TIP modes. The TIP multiplexes these inputs together. The analog channel appearing in word zero is selectable. The selected channel is identified in bits 7 and 8 of word 3, and bits 1 to 7 of word 4. Any one of the 512 analog inputs can be designated to appear in this word. This is done by selecting the given input channel as the dwell address in a TIP mode command data word. If the TIP also happens to be in the dwell mode, this analog telemetry point will also appear in minor frame words 14 through 103.

The TIP provides a 36 bit time-of-day counter with a count granularity of one millisecond. This counter is capable of being reset by command. The TIP inserts the time code into the TIP format as well as outputting it to the MIRP at a rate of once per millisecond.

The TIP receives its master timing from the XSU and provides 32 second, 128 second, and 256 second synchronization pulses to the payload instruments.

4.8.1.2.2 MIRP

The function of the Manipulated Information Rate Processor (MIRP) is to buffer, process, and format digital data from the selected five of six AVHRR channels into the required four output formats. The five AVHRR channels produce 10240 words of earth data per scan. The scan rate is 6 revolutions per second and each word has 10 bits. The unit configuration, processing algorithms, and output data rates are consistent with a 5 channel AVHRR. The MIRP contains large memories to: (1) permit a continuous output of earth scan data during the time the AVHRR is viewing space, and (2) manipulate the earth scan data into the desired digital signals. The MIRP output formats are:

(1) High Resolution Video (LAC and HRPT)
(2) Real Time Medium Resolution Video, (APT) and
(3) Global Stored Data (GAC).

The TIP output and AMSU data from the AIP are multiplexed into the high resolution and global stored output formats.

The MIRP output formats are summarized as follows:

	HRPT/LAC	GAC	APT
Form of Data	Serial Digital Bit Stream 10-bit words, most significant bit first		Analog A-M on 2.4 kHz Subcarrier
Line Rate	6/sec	2/sec	2/sec
Word Rate	66.54K words/sec	6654 wordslsec	4160 words/sec prior to D/A Conversion
Number of AVHRR Channels Included	5	5	2
Words of earth scan per line per channel	2048	409	909 prior to D/A Conversion
Processing of AVHRR Data	Formatting Only	Resolution Reduction & Formatting	Resolution Reduction & correction for geometric distortion formatting
Other Data than AVHRR	TIP; time of day; AMSU	TIP; time of day; AMSU	Minute Marks; calibration wedge

The MIRP can operate in any of several different modes, but all except the Normal mode are for use in case of failure or for diagnostic evaluation. In Normal Mode, the MIRP issues sampling commands to the AVHRR in phase with the line-synchronization pulses from AVHRR, the MIRP generates frame synchronization from internal timing and re-phases frame synchronization automatically to the line synchronization pulse if the phase displacement exceeds a preset value. In the Override Rephase Logic Mode, the automatic rephasing function is deleted. In the Internal Sync Mode the MIRP issues sampling commands to the AVHRR and generates frame synchronization in phase with its internal timing.

The AVHRR/MIRP interface provides data sampling commands by the MIRP, digitized AVHRR data from the AVHRR and line synchronization pulses from the AVHRR. In the Normal and Override Rephase Logic Modes, the MIRP issues sampling commands in phase with the line synchronization pulses from the AVHRR. In the Internal Sync Mode, the MIRP issues sampling commands in phase with the MIRP's internal timing.

In all modes the MIRP generates frame synchronization in phase with MIRP internal timing. The MIRP measures the time difference between the frame synchronization and the line synchronization pulse from AVHRR and formats this time difference into a data word which it inserts in the frame header of the HRPT, LAC, and GAC formats. In Normal Mode only, the MIRP rephases the frame synchronization automatically to the line synchronization pulse if the above time difference exceeds a preset value.

The MIRP provides one minute elapsed-time marks in the APT format. The MIRP accepts master timing from the XSU and outputs HRPT, GAC and LAC formats to the XSU. The MIRP randomizes GAC and LAC outputs to improve transition density and outputs the APT format as a modulated subcarrier to each Real Time VHF transmitter.

4.8.1.2.3 XSU

The XSU provides switched data interfaces with the AIP, the MIRP, the DTRs and the STXs in response to CIU commands. It distributes timing to the Data Handling Subsystem and to the payload instruments. It is designed to prevent single-point failures from degrading performance of redundant interfacing units. The only exception is the split-phase TIP data interface which is used for real-time transmission via S-Band transmitter during boost mode and the first orbit only. A single-point failure can degrade performance associated with a non-redundant interfacing unit, but not with two or more.

The XSU is capable of operating in Recorder Input Modes, STX Input Modes, or Power Switching Modes. In the Recorder Input Modes, the XSU can transfer any of the following data to the input interface of any DTR; TIP NRZ Interface, AIP NRZ Interface, MIRP LAC data, and MIRP GAC data. Any of these data streams can be connected to more than one DTR and all data inputs to the DTRs are NRZ-L. In the STX Input Modes, the XSU can transfer the playback data from any DTR to the input interface of any STX, can convert the HRPT data input from the MIRP to a split-phase format and transfer the data to any STX, or can transfer split-phase TIP or AIP data. In the Power Switching Modes, the XSU operates with either side A on/side B off or side B on/side A off.

The XSU accepts master timing from the CIU. It provides timing signals to the data handling subsystem and to the payload instruments as follows:

1.248 MHz to the AMSU, SEM, SBUV, AIP, HIRS
0.9984 MHz to the TIP and MIRP
1.3308 MHz to the MIRP

The XSU provides the following timing signals to the DTR playback clocks as required:

332.7 kHz for TIP playback
1.3308 MHz and 2.6616 MHz for LAC and GAC playback

The DTR record clocks are received with the associated AIP, TIP or MIRP data. These are divided down within the AIP, TIP and MIRP from clocks supplied by the XSU. All timing is coherently derived from the 1.024 MHz clock from the CIU.

4.8.1.2.4 DTRs

Five government-furnished digital tape recorders serve to store the mission data. Four recorders are required to support the mission: two recorders are required for the global area coverage (GAC) data during the multiple blind orbit condition (they are also used for recording the TIP output for playback to the European station during these orbits); two more are required for selectively recording high-resolution local area coverage (LAC) data during these

orbits. One DTR will record TIP.Boost Mode data during the spacecraft boost phase. A fifth recorder is carried for redundancy. GAC data is recorded continuously; LAC data is recorded for 10 minutes per orbit. All recorders are identical. Each contains two identical transport units and a common electronics unit.

4.8.1.2.5 AIP

The AIP is a redundant unit which inputs data from the three AMSU instruments and from the TIP and combines the data into a 16.64 Kbps format for output to the XSU and MIRP. Both NRZ-L and split phase data are output to the XSU, enabling both recording and real-time transmission of the data. The AIP is commandable such that the bi-phase output can be AIP data (AMSU and TIP combined) or just TIP data.

The AIP also generates the necessary data-transfer handshaking signals and the El-second synchronization signal for the AMSU instrument.

4.8.2 TIROS INFORMATION PROCESSOR (TIP)

4.8.2.1 TIP Description

The TIP performs the telemetry and low-rate instrument data processing function.

Analog telemetry signals are digitized and combined with one-bit telemetry digital status telemetry (Digital B), time code, command verification, sync, spacecraft address, format identification, and digitized instrument data (Digital A) to form a single, digital, TDM/PCM serial-output bit stream. The TIP supplies several data-output signals: one is sent to the Manipulated Information Rate Processor (MIRP); a second to the beacon transmitters; a third to the recorders; and a fourth to an S-Band transmitter.

The MIRP incorporates the TIP NRZ-L output into the Real-Time High-Resolution output, the Local Area High Resolution output , and the Global-Stored Medium-Resolution output. The Beacon transmitter phase-modulates its carrier frequency with TIP biphase - L digital data for real-time transmission to earth stations.

Digital recorders store TIP digital data for future transmission to ground stations via the S-Band via the S-Band link, The XSU will route TIP biphase L data to an S-Band transmitter for monitoring spacecraft status during the ascent phase of the mission.

One-half of the Dual TIP is always on whenever 28-volt power is applied. The TIP is used during spacecraft integration to aid in verifying the operational status of the spacecraft, for pre-launch tests at the launch pad, and during launch, orbit injection, spacecraft acquisition and normal orbital mode.

The TIP generates a data format as specified by one of two fixed programs established prior to integration. The programs define the format during launch and normal orbital mode. For diagnostic purposes during orbital mode, a CPU dump-and single-point analog-dwell submode formats are provided. Both submode formats pre-empt normal orbital mode programming.

The TIP interface diagram is shows. in Figure 4.8.2-l. A summary of TIP salient characteristics is given in Table 4.8.2-1.

4.8.2.2 Data Handling Requirements

The TIP is designed to accommodate the input signals given in Tables 4.8.2-2 and 4.8.2-3. The tabulated telemetry values include estimates for all spacecraft housekeeping functions, as well as the instruments. The signals are divided into three classes: Digital A, Digital B, and Analog.

The Digital A signals include the low-rate instrument data, command verification data, time code data, CPU telemetry data, and CPU dump data. These signals are characterized by the method in which they are sampled by the TIP. One or more synchronization signals is sent to each of the Digital A signal sources to synchronize their timing with TIP timing. In addition, an enable pulse is sent to the signal source selected for sampling. The data contained in a buffer at the Digital A signal source is asynchronously loaded by the Digital A signal source and is then clocked in the TIP by a TIP-supplied clock signal. Details on the Digital A interface can be found in Paragraph 4.8.2.4.4.

The Digital B signals (one-bit digital status telemetry) are assembled in the TIP as 8-bit digital words. These words are sampled as required by the particular format being generated.

The Analog inputs are commutated, sampled, and quantized into 8-bit digital words by the TIP. These inputs are sampled as.required by the format being generated.

4.8.2.3 Telemetry Formats

The TIP generates four telemetry formats, one in each of its four operating modes. The TIP operating modes are: Orbital Mode, Boost Mode, and High-rate Analog Dwell Mode (Single-Point). The formats generated in the Orbital Mode and Boost Mode are shown in Figures 4.8.2-2 and 4.8.2-3, respectively. The CPU Dump Mode format and High-Rate Dwell Mode format are made available for diagnostic purposes. These formats are subformats of the Orbital Mode format.

4.8.2.3.1 Orbital Mode Formats

The orbit mode minor frame contains 832 bits organized in 104 8-bit words. The minor frame period is 0.1 sec. During the orbital mode the TIP output data rate is 8.320 Kbps. Six subcommutated words are made available for sampling low data rate information. One 1 sample/32 sec, two sample/16 sec, two 1 sample/3.2 sec, and one 1 sample/sec subcoms are provided. The first 3.2 sec subcom is dedicated to Digital B (bi-level) data, the second 3.2 sec subcom is divided between Digital B data and XSU data, and the remaining subcoms are dedicated to analog data. The Subcom Frame Formats for all TIP operating modes are shown in Figure 4.8.2-4.

There are 56 bits of overhead which contain sync, spacecraft address, frame status, and parity information. The first 20 bits of each minor frame consists of an optimum frame sync code selected from the GSFC PCM Telemetry Standards. The next four bit6 are used for spacecraft identification. The address is selected by external connection to the unit, prior to flight.

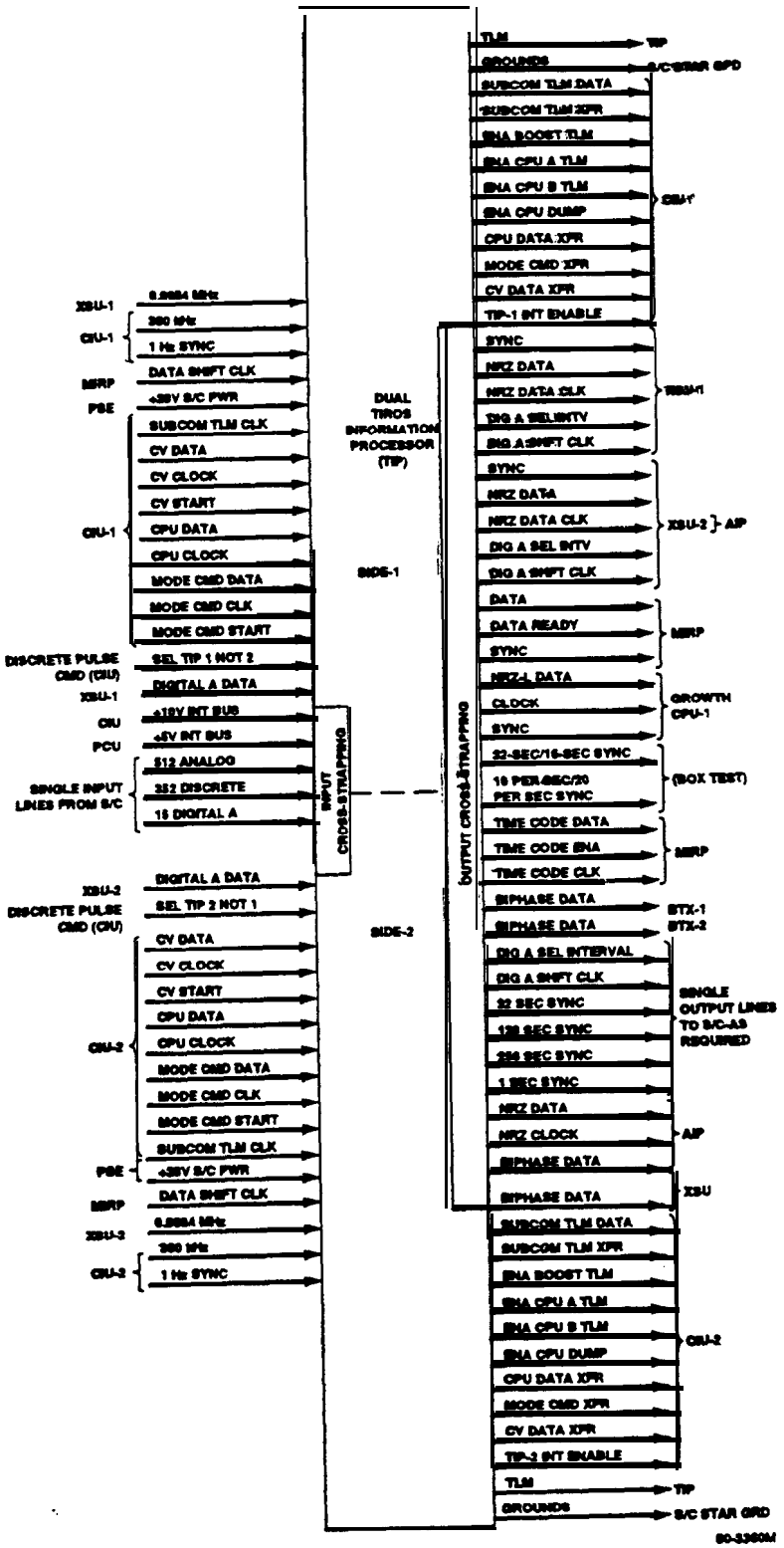


Figure 4.8.2-l. TIP Interface Diagram

TABLE 4.8.2-1. TIP SALIENT CHARACTERISTICS

Parameters	Characteristics
Size (1 x W x H)	13.274 x 6.875 x 8.750
Weight	17 lbs
Power	5.2 Watts Max EOL
Number of Inputs 352 Digital "B" 16 Digital "A"	512 Analog
Redundancy	Dual unit except for common telemetry input gates. A gate failure is confined to a maximum of 8 input channels.
Digital "A" inputs are individually buffered and cross-strapped internal to TIP	
Orbital Mode Format	
Output Data Rate	8320 bps
Minor Frame Length (Fixed minor frame length-alterable frame word assignments)	832 bits
Minor Frame Period	0.1 sec.
Major Frame Period	32 sec.
Word Organization	8-bit
Minor Frame Capacity	12.5% Spare
Subcommutated Frames	6
• 32-sec Analog Subcom (Eardwire Program)	192 channels @ 1 sample/32 sec. 64 channels @ 1 sample/l6 sec.
• 16-sec Analog Subcom (Program in PROM)	128 channels allocated
• 16-sec Analog Subcom (Rardwire Program)	128 channels allocated
• I-set Analog Subcom (Program in PROM)	128 channels allocated
• 3.2-sec Dig "Bl" Subcom (Rardwire Program)	256 channels @ 1 sample/3.2 sec.
3.2-sec Dig "B2" Subcom	96 channels @ 1 sample/3.2 sec.
Diagnostic Mode Formats	
CPU Memory Dump	Dumps at 60 16-bit words/second.
Single-Point Analog Dwell	Dwell channel selected by command, 1 sample/sec or 1040 samples/sec. analog dwell capability
Boost Mode Format	
Output Data Rate	16.64 kpbs
Minor Frame Length (Fixed minor frame length-alterable f rame word assignments)	832 bits
Minor Frame Period	0.05 sec.
Major Frame Period	16 sec.
Word Organization	8-bit
Minor Frame Capacity	2.9% Spare
Subcowutated Frames	Orbital Mode subcommutated formats with sampling at 2 times the orbital rate
Analog Channel Uniform Sampling Rate (16 Channels)	20 samples/sec/channel
Single-Point Analog Dwell	2 samples/sec
Parity	Even parity check bit generated for every 17 word6 formatted in all operating modes except for High-rate Dwell Mode

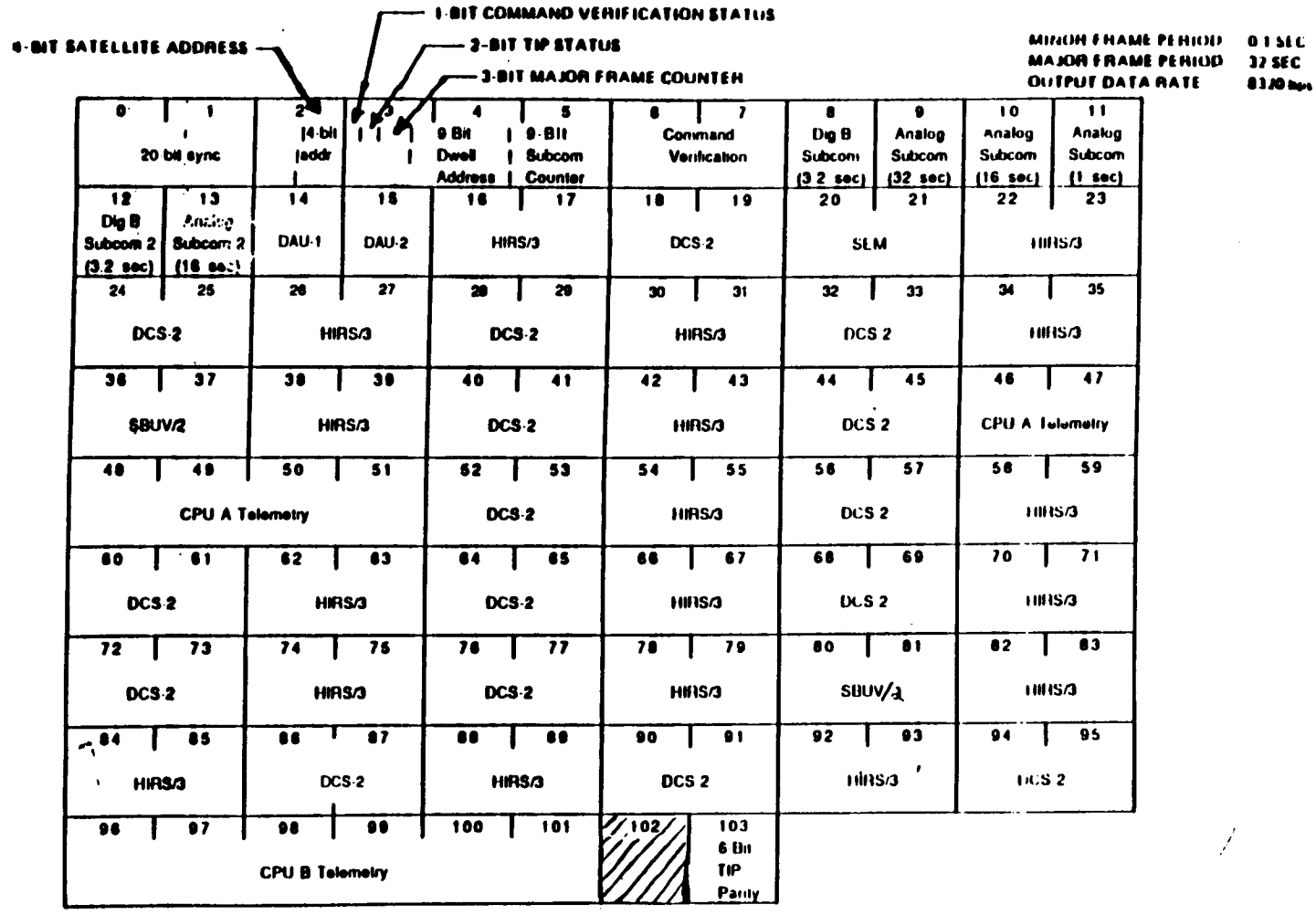
TABLE 4.8.2-2. TIP ORBITAL MODE DATA HANDLING REQUIREMENTS

Input Signal	Data Rate (bps)	Source Sampling Requirements	8-Bit Words/0.1 sec Minor Frame
AIRS/3	2880	16-Bit Word/Sample No Interrogation during first 4 msec of Minor Frame	36
DCS	960	16-Bit Word/Sample	32
SEM	160	16-Bit Word/Sample	2
SBUV/2	320	16-Bit Word/Sample	4
Command Verif.	160	16-Bit Word/Sample	2
CPU A TLM	480	Interrogation at the Beginning of a Minor Frame-Burst of Three 16-Bit Words/Sample	6
CPU B TLM	480	Interrogation at the Beginning of a Minor Frame-Burst of Three 16-Bit Words/Sample	6
Time Code		40-Bit Word - 1 Sample/32 sec	(Subcoms Pre-empted)
SYNC and S/C Adr.	240		3
Frame Status	320		4
Digital B TLM-1	80	1 Sample/3.2 sec	1
Digital B TLM-2	80	1 Sample/3.2 sec	1
Analog TLM	80 80 80 80	1 Sample/sec 1 Sample/l6 sec 1 Sample/16 sec I Sample/32 sec	1 1 1 1
CPU Memory Dump	960	Burst of 3 16-Bit Words/Sample	(CPU A&B TLM Pre-empted)
xsu	20	8-Bit Word/Sample	Digital B TLM-2 Pre-empted
DAU	160	8-Bit Words	2
SATCU	16	8-Bit Words	Preempts 16AN-2 Subcom
Subtotals	8240		103
Spares	80 1%		1
Total	8320		104

TABLE 4.8.2-3. TIP BOOST MODE DATA HANDLING REQUIREMENTS

Input Signal	Data Rate (bps)	Source Sampling Requirements	8-Bit Words/0.05 sec Minor Frame
CPU	11200*	Burst of 7 16-bit words/sample-interrogation 5 times per Minor Frame (Every 10 msec)*	70*
sync & S/C	480	24-bit word/sample	3
Frame Status	800	16-bit word/sample	5
Command Verification	320	16-bit word/sample	2
Digital B Telemetry-l	160	1 sample/l.60 sec	
Digital B Telemetry-2	160	1 sample/l.60 sec	1
XSU (Digital A) Status		8-bit word/sample	(Part of Digital Telemetry-21
Analog Telemetry	160 160 160 160	1 sample/0.5 sec 1 sample/8.0 sec 1 sample/16.0 sec 1 sample/8.0 sec.	1 1 1 1
	2560	1 sample/0.05 sec	16
DAU	320	8-bit Words	2
Subtotals	16640		104
Spares	0		0
Total	16640		104

*Each burst will contain 5 16-bit words rather than the capacity 7 16-bit words. The data rate will be 8000 bits/sec. There will be 50 8-bit words per 0.05-sec minor frame. The excess capacity will be filled with an alternating one-zero pattern.



NOTES
- NUMBER IN UPPER LEFT HAND CORNER INDICATES MINOR FRAME WORD NUMBER
- TIME CODE DATA APPEARS DURING MINOR FRAME "0" WORD LOCATIONS 8 THROUGH 12
- ///// WORD LOCATIONS ARE SPARE AND CONTAIN CODE 01010101.

90-3361

Figure 4.8.2-2. TIP Orbital Mode Format - NOAA-KLM

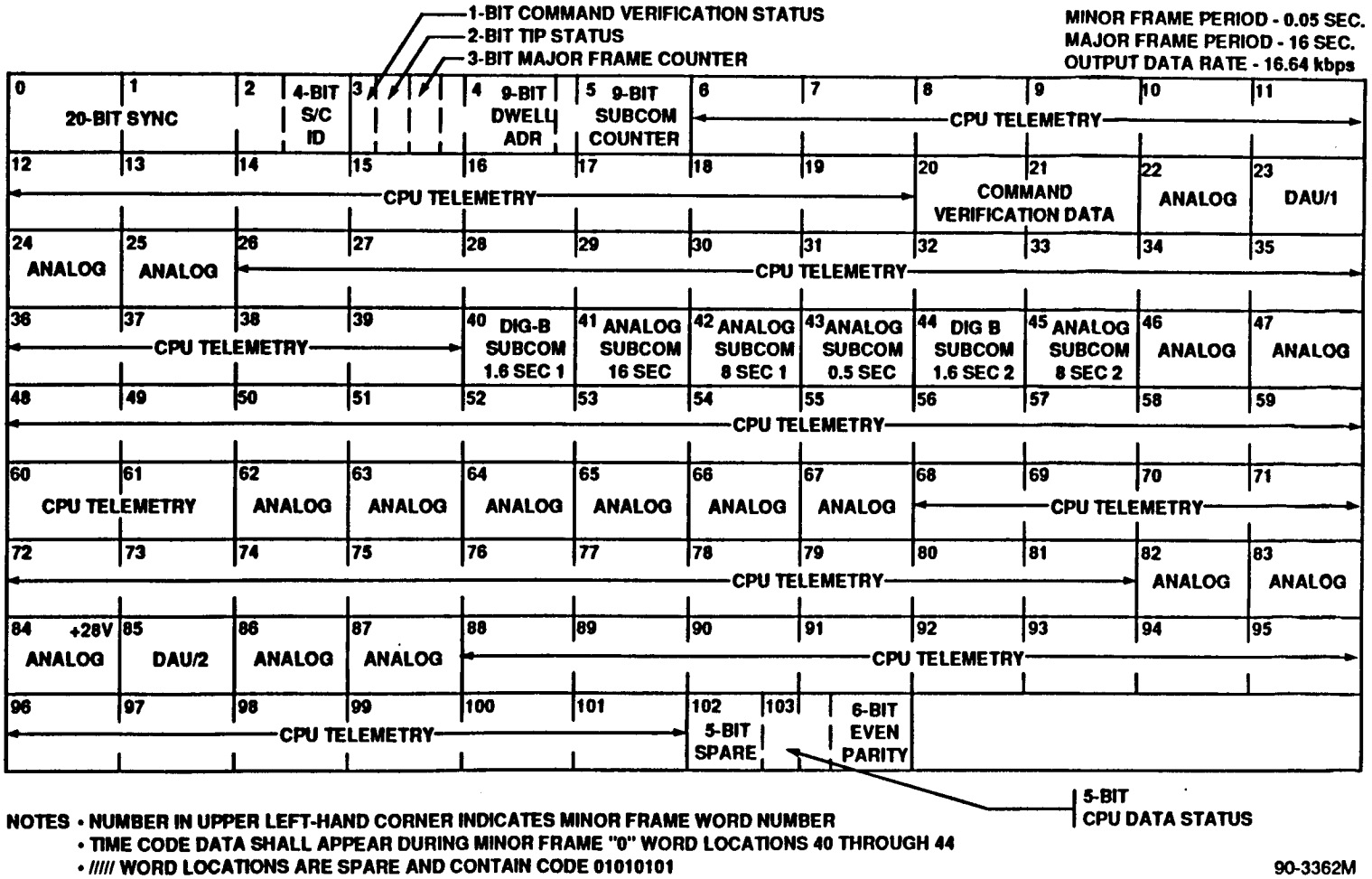


Figure 4.8.2-3. TIP Boost Mode Format for NOAA-KLM

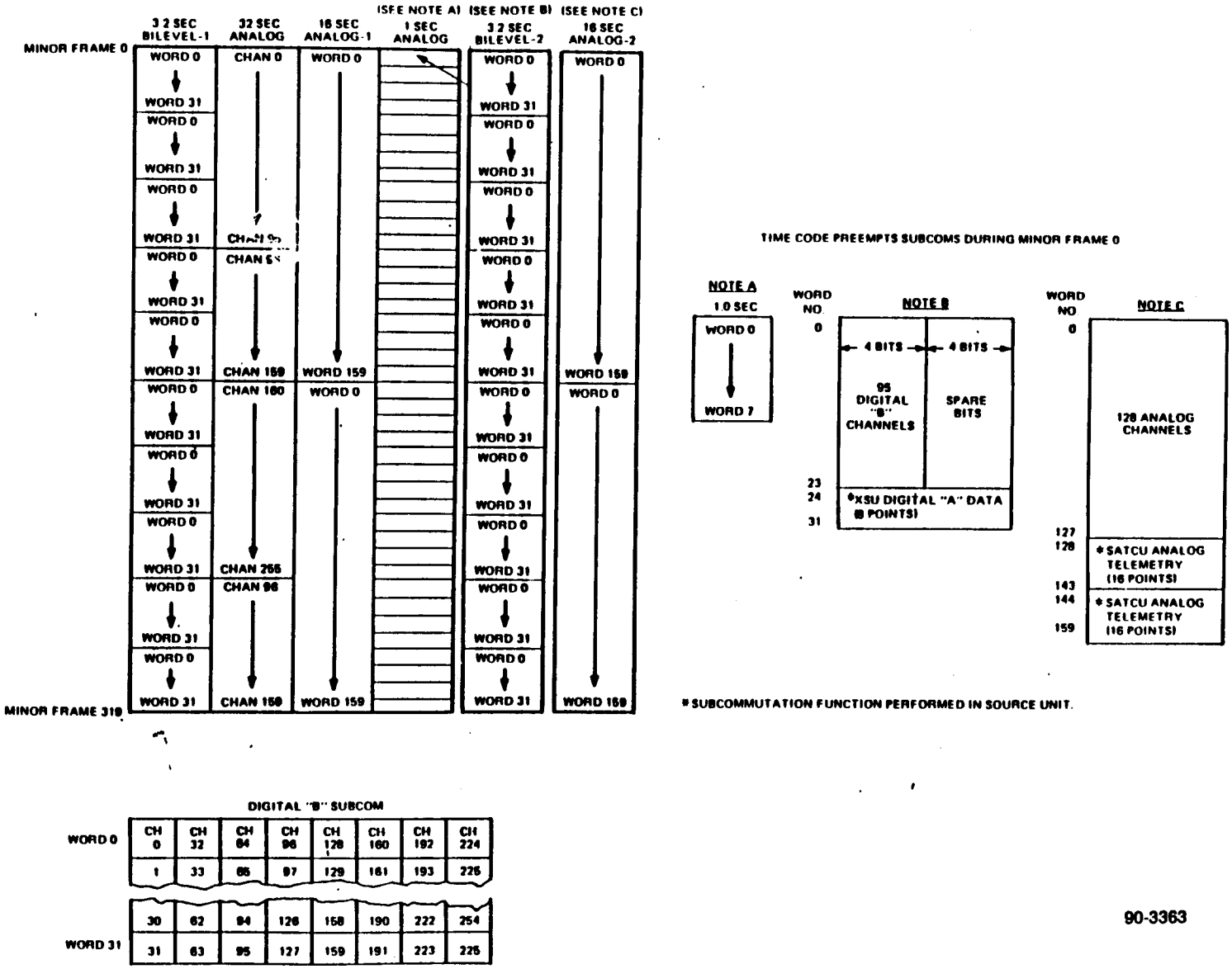


Figure 4.8.2-4. TIP Subcom Frame Format

Bit 1 of minor frame word 3 is used to inform the ground that a command verification word update has been received. The bit representation is as follows:

1 - CV word updated during this minor frame

0 - CV word not updated during this minor frame

The CV word received last is repeated every minor frame. Bits 2 and 3 of minor frame word 3 are used to identify the various TIP operating modes. The next three bits are used to identify the instrument calibration data frames which occur once every 128 sec or 256 sec. The major frame counter is binary coded: count 000 represents major frame 0 and count 111 represents major frame 7.

Bits 7 and 8 of minor frame word 3 and bits 1 through 7 of minor frame word 4 contain the 9 bit address which is used to identify the channel being sampled in all dwell modes. Address 000000000 represents analog channel "0" and address 111111111 represents channel 511.

The next 9 bits are used to identify the subcom frame word. The subcom counter is binary coded and advances once per minor frame and resets every 320 minor frames. Count 000000000 represents subcom word 0 and count 100111111 represents subcom word 319.

Bits 1 and 2 of Minor Frame Word 102, are used to inform the ground of the status of CPU data transferred to the TIP during normal interrogation. The bit representation is a follows:

Word 103		
Bit 1	bit 2	Designation
0	0	All CPU data received.
1	0	CPU A telemetry or the first three 16-bit words of CPU dump data output during the minor frame not received in entirety.
0	1	CPU B telemetry or the last three 16-bit words of CPU dump data output during the minor frame not received in entirety.
1	1	CPU A telemetry and CPU B telemetry or the first and last three 16-bit words of dump data was not received in entirety.

Since CPU data is not transferred to the TIP in the high-rate dwell mode, no CPU status bits are output.

Bits 3 through 8 of Minor Frame Word 103 is used to check for even parity on TIP data. The bits have the following interpretation:

Bit	Interpretation
3	Even parity check on data contained in Minor Frame Words 2 through 18.
4	Even parity check on data contained in Minor Frame Words 19 through 35.
5	Even parity check on data contained in Minor Frame Words 36 through 52.
6	Even parity check on data contained in Minor Frame Words 53 through 69.
7	Even parity check on data contained in Minor Frame Words 70 through 86.
8	Even parity check on data contained in Minor Frame Words 87 through 102 including Bits 1 through 7 of Minor Frame Word 103.

The remaining words in the minor frame can be assigned to Digital A or analog sources.

4.8.2.3.2 Boost Mode Format

The Boost mode minor frame format is shown in Figure 4.8.2-3. The frame structure, including the subcom frames, is identical to the orbit mode format except that output data rate is 16.64 K bps. Like the orbit mode format, minor frame word allocations are alterable by changing the contents of the TIP program memory (see Paragraph 4.8.2.4.1).

In Boost mode there are 58 bits of assigned overhead. These data are identical to orbit mode overhead with the addition of 2 extra bits for CPU status. Since the CPU data transferred to the TIP in Boost Mode consists of 5 interrogations instead of 3 per minor frame two additional CPU status bits are output. Bits 6-8 of minor frame word 102 and bits l-2 of minor frame word 103 are used to inform the ground of the status of CPU data transferred to the TIP during normal interrogation. The bit representation is as follows:

Word 102 Bit 6	Designation
0	CPU data contained in word locations 6-19 received in entirety.
1	CPU data contained in word locations 6-19 not received in entirety.

Word 102 Bit 7	
0	CPU data contained in word locations 26-39 received in entirety.
1	CPU data contained in word locations 26-39 not received in entirety.

Word 102 Bit 8	
0	CPU data contained in word locations 48-61 received in entirety.
1	CPU data contained in word locations 48-61 not received in entirety.

Word 103 Bit 1

0	CPU data contained in word locations 68-81 received in entirety.
1	CPU data contained in word locations 68-81 not received in entirety.

Word 103 Bit 2

0	CPU data contained in word locations 88-101 received in entirety.
1	CPU data contained in word locations 88-101 not received in entirety.

The remaining words in the minor frame can be assigned to Digital "A" or analog sources.

4.8.2.3.3 CPU Dump Format

A CPU dump format is available for verifying CPU memory loads and for diagnostics of the CPU and its software. It is a variation of the Orbit Mode Format shown in Figure 4.8.2-2, wherein all of the CPU-A and CPU-B words are dedicated to dump from a single CPU. All other data remain undisturbed.

4.8.2.3.4 Single-Point Analog Dwell Mode

A single-point analog dwell mode is available for hardware diagnostics. It is a major variation of the orbit mode format. Selecting this format effectively takes the spacecraft out of service, since all payload sensor data normally formatted by the TIP are lost.

In the high-rate dwell mode, all of the words in the minor frame are pre-empted with digitized analog samples from any one analog data source except for overhead, command verification, and the subcoms. Fourteen adjacent samples out of 104 are lost due to overhead, command verification, and subcoms. The sampling rate is 1040 eight-bit samples/second, with gaps as noted above.

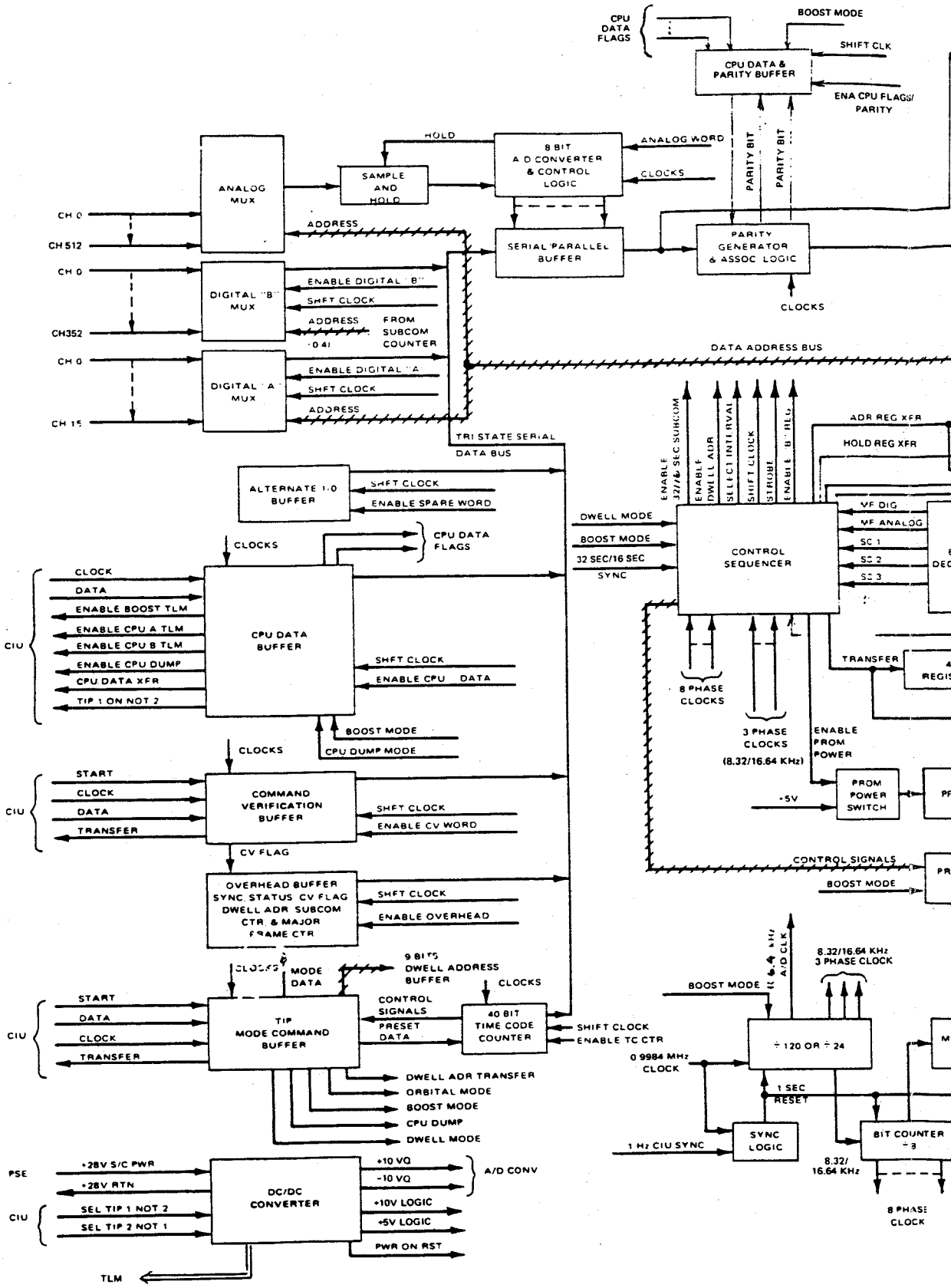
In addition to the high-rate dwell format. a low-rate dwell capability is provided in the orbit mode and boost mode formats. Word 0 in the- orbit mode 1 sec subcom and the Boost mode 0.5 sec subcom is reserved to sample any analog channel upon command. The address of the channel being sampled will appear in each minor frame. Payload data is not lost in this mode.

4.8.2.4 Function Description

4.8.2.4.1 Programming and Timing

A functional block diagram of the TIP is shown in Figure 4.8.2-5. For simplicity, the redundant portion, including cross-strapping, has been omitted.

Upon application of spacecraft power, one side of the TIP will become activated; the TIP will begin to cycle through the selected program stored in the TIP program memory and automatically select the program for Orbital Mode.


CPU DATA FLAGS
BOOST MODE
SHIFT CLK
CPU DATA & PARITY BUFFER
ENA CPU FLAGS/ PARITY
HOLD
8 BIT A D CONVERTER & CONTROL LOGIC
ANALOG WORD
CLOCKS
PARITY BIT
PARITY BIT
ANALOG MUX
SAMPLE AND HOLD
CH 0
CH 512
ADDRESS
SERIAL PARALLEL BUFFER
PARITY GENERATOR & ASSOC LOGIC
CLOCKS
CH 0
DIGITAL "B" MUX
ENABLE DIGITAL "B"
SHFT CLOCK
ADDRESS
FROM SUBCOM COUNTER
CH352
CH 0
DIGITAL "A" MUX
ENABLE DIGITAL "A"
SHFT CLOCK
ADDRESS
CH 15
DATA ADDRESS BUS
TRI STATE SERIAL DATA BUS
ALTERNATE I-O BUFFER
SHFT CLOCK
ENABLE SPARE WORD
CLOCKS
CPU DATA FLAGS
CLOCK
DATA
ENABLE BOOST TLM
ENABLE CPU A TLM
ENABLE CPU B TLM
ENABLE CPU DUMP
CPU DATA XFR
TIP 1 ON NOT 2
CIU
CPU DATA BUFFER
SHFT CLOCK
ENABLE CPU DATA
BOOST MODE
CPU DUMP MODE
CLOCKS
START
CLOCK
DATA
TRANSFER
CIU
COMMAND VERIFICATION BUFFER
SHFT CLOCK
ENABLE CV WORD
CV FLAG
OVERHEAD BUFFER SYNC STATUS CV FLAG DWELL ADR SUBCOM CTR & MAJOR FRAME CTR
SHFT CLOCK
ENABLE OVERHEAD
CLOCKS
MODE DATA
9 BITS DWELL ADDRESS BUFFER
CLOCKS
START
DATA
CLOCK
TRANSFER
CIU
TIP MODE COMMAND BUFFER
CONTROL SIGNALS
PRESET DATA
40 BIT TIME CODE COUNTER
SHIFT CLOCK
ENABLE TC CTR
DWELL ADR TRANSFER
ORBITAL MODE
BOOST MODE
CPU DUMP
DWELL MODE
PSE
+28V S/C PWR
+28V RTN
CIU
SEL TIP 1 NOT 2
SEL TIP 2 NOT 1
DC/DC CONVERTER
+10 VQ
-10 VQ
A/D CONV
+10V LOGIC
+5V LOGIC
PWR ON RST
TLM
ENABLE 32/16 SEC SUBCOM
ENABLE DWELL ADR
SELECT INTERVAL
SHIFT CLOCK
STROBE
ENABLE "B" FIELD
ADR REG XFR
HOLD REG XFR
DWELL MODE
BOOST MODE
32 SEC/16 SEC SYNC
CONTROL SEQUENCER
VF DIG
VF ANALOG
SC 1
SC 2
SC 3
TRANSFER
8 PHASE CLOCKS
3 PHASE CLOCKS (8.32/16.64 KHz)
ENABLE PROM POWER
+5V
PROM POWER SWITCH
CONTROL SIGNALS
BOOST MODE
A/D CLK
8.32/16.64 KHz 3 PHASE CLOCK
BOOST MODE
÷ 120 OR ÷ 24
0.9984 MHz CLOCK
1 SEC RESET
1 Hz CIU SYNC
SYNC LOGIC
BIT COUNTER ÷ 8
8.32/ 16.64 KHz
8 PHASE CLOCK

During the commutation process, the TIP will generate all necessary control signals for read-in of the data sources.

The TIP program memory consists of one SIGNETICS 2KX8 bit Bipolar programmable read-only memories. Use of these memories allows format changes to be made up to one month prior to integration. The program memory is organized in 512 x 8-bit bytes and is partitioned as follows:

Memory Partitioning	No. of Words	Address Location
Orbital Mode Minor Frame Program	128 words	0 thru 127
Boost Mode Minor Frame Program	128 words	128 thru 255
16 sec/8 sec Subcom Program	192 words	256 thru 447
1 sec/0.5 sec Subcom Program	16 words	448 thru 463
Minor Frame Analog Channel Addresses	16 words	464 thru 479
Spare	32 words	480 thru 511
Inactive	1536 words	512 thru 2047

The TIP Control Sequencer takes an instruction from the control PROM's and, from that data, determines the next word in the TIP output format. It executes the necessary steps to form the address of the data source. The instruction format is shown below:

Op-Code			Data				
B7	B6	B5	B4	B3	B2	B1	B0

Op-Code	Op-Code Representation	Data (Bits 0 to 4)
000	Digital Minor Frame Word*	Data Source Address
001	32/16 sec Analog Subcom	Not Used
010	16/8 sec Analog Subcom	Not Used
011	16/.5 sec Analog Subcom	Not Used
100	16/8 sec Analog /SATCU Subcom	Not Used
101	Spare Subcom	Spare
110	Spare Subcom	Spare
111	Analog Minor Frame Word	Analog Source Address

*Digital "B" Subcom is be treated as a digital word.

The three most significant bits represent an op code for digital, analog, or subcom words. In the case of digital words, the five least significant bits represent the source address. For analog words, the four least significant bits, when added to the binary equivalent of 464, gives the PROM address where the analog address is located. For subcom words, the bits are not used. The addresses of the data is contained in the subcom counters. Power on reset sets all counters and registers to zero. This automatically selects the overhead buffer, which causes the first word to be output. In the meantime, the second word is being readied by the control sequencer; therefore, the control sequencer is working one word ahead of the output word. First, the sequencer turns on the PROM's and loads the data into the A and B registers. The address for

the PROM is the word counter. At this point, the type of word can be determined. Second, based on the word type and the subcom counters, either the PROM is readdressed and the data is loaded into the holding register or B register, or subcom data is loaded into the holding register. If the word is digital, then register B data is loaded into the address register, unless the 32 sec counter is zero and it is any subcom word, then the data is loaded into the address register which enables time code readout. If it is an analog word or a subcom word, then the PROM must be enabled again to get the address data out. An analog word and the 32 second subcom counter not equal zero loads the address holding register with the B register data plus CT 464. If a 32 second subcom is called for and the counter is less than 256, then the holding register data is the subcom count. If the counter is greater than or equal to 256, then the holding register data is the subcom count minus 160. This is a repeat of channels 96 through 159. These channels are uniformly sampled once every 16 seconds except when the 1 sec count is zero, in which case the analog dwell address is sampled, the 1 sec and 16 sec subcoms involve addressing the PROM again. For 16 sec subcom, the PROM address is 256 plus the 16 sec subcom counter. The data at that address is loaded into the holding register. If it is a 1 second subcom, the PROM address is 448 plus the 1 second subcom count. As with the 16 second subcom, the data at the address is loaded into the holding register.

When the new source address has been set up, the word counter is advanced one count. If the count is 104, the counter is reset and a new minor frame is started. The subcom counters are advanced one count or reset if they have reached their maximum count.

When in boost mode, the initial PROM data is located at 128 plus the word counter. In dwell mode, after word 13, the dwell address is loaded into the holding register.

Each word is broken up into eight bit times numbered 0-7. During BC DEC 1, the PROM is enabled and the data is transferred into the A and B registers. If the PROM is to be addressed again, this is done in BC DEC 2. If the PROM is not to be readdressed, the data is transferred to the holding register in BC DEC 3. This allows time for the PROM to release the data bus, yet if data is to come from the PROM it does not waste the energy that went into turning on the PROM in the first place.

The basic clock input is 0.9984 MHz which is the input to the chain. The sync logic synchronizes the timing chain to the CIU 1 Hertz clock. The 0.9984 MHz is divided by three. This is then divided by five to get 66.56 kHz which is used by the CIU/CPU board for operating its sequencers and transferring time code data to the MIRP. The divide by three output also feeds a divide by two whose output is the basic boost rate clock. Another divide by two is the basic orbit mode clock. An AOS gate selects between the boost and orbit clock. The boost clock of 166.4 kHz is used as the logic clock in the successive approximation A/D converter.

The output of the AOS (166.4/83.2) is divided by five to produce the Biphase Data generator clock. The AOS clock is also divided by two to get the parity logic clock.

The parity logic clock is divided by five to generate a three phase bit rate clock. The bit rate clock is divided by eight into an eight phase clock, each phase active for one bit time. The carryout is the word rate clock.

At this point, the chain splits into two directions. One chain, the binary chain, has a divide by 104. This is the Minor Frame Counter. The outputs are used as the initial address to the PROM. The output of this counter clocks the 1 second subcom counter. The other half of the chain is the decade divider. This facilitates decoding particular word counts. The output of this chain drives the 16 and 32 second subcom counters. The 32 second subcom counter clocks the divide by eight Major Frame counter.

Finally, there is reset logic for the decode and binary chains. The counter are reset every 104 words. The 16 and 32 second subcom counters also have individual reset logic.

4.8.2.4.2 Analog Multiplexer

The TIP Analog multiplexer design includes failure isolation as specified below:

1. Any multiplexer failure will not damage any analog sources;

2. Any failure will not damage the TIP control logic circuitry;

3. Analog source point failures will not damage the multiplexer nor will it compromise any other channels of data; and

4. Any multiplexer failure mechanism will not compromise more than eight channels of data.

The redundant analog multiplexer is comprised of four identical boards (A2, A3, and A4, and A17), each commutating 128 input channels into two redundant outputs. Additional multiplexing is done on the Dual A/D converter board A5, where a total of six outputs from each side of the multiplexer will be further commutated into an LH0052 voltage follower. The multiplexer operation is performed exclusively by HARRIS HI-508A 8-channel multiplexer devices. These devices are constructed using COS/MOS technology to provide low power operation in addition to the following features:

1. Analog overvoltage protection;
2. Break-before-make switching;
3. Fast access time;
4. Fail safe operation in the event of power loss; and
5. Low charge transfer characteristics as a result of gate switching.

Input cross-strapping is accomplished at the input to the first level of multiplexing to insure that not more than eight channels are contaminated as a result of a multiplexer gate failure. The TIP side selected for operation controls and power its respective half of the multiplexer. Therefore, with the cross-strapping at the multiplexer input, the only interaction between redundant halves is through the input cross-strapping connections.

4.8.2.4.3 Digital B Multiplexer

The TIP Digital B multiplexer design includes failure isolation as specified below:

1. Any multiplexer failure will not damage any telemetry source points;

2. Any multiplexer failure will not damage the TIP control logic circuitry;

3. Telemetry source overvoltage failures will not damage the multiplexer, nor will it affect any other telemetry; and

4. Any multiplexer failure will at most compromise eight channels of discrete telemetry.

The Digital B multiplexer is comprised of three identical circuit boards, each handling 128 channels. Each board contains four independent bit multiplexers which are organized to output 32 four bit words and which when combined provide selection of one out of 32 possible eight bit words.

All input channels are buffered and cross-strapped to redundant multiplexing logic on the same board. The TIP side selected for operation controls and powers its respective multiplexer section. The only interaction between redundant halves is through the cross-strapping connections. The multiplexer operation is performed with Harris HI-508A 8-channel multiplexer devices. The Harris HI-508A incorporates input overvoltage protection circuitry, and in the present configuration, can handle any voltage between -20 volts and +15 volts. Any input voltage exceeding either power supply voltage is shunted to that supply. Due to the multiplexer overvoltage protection network, both sides of the first level of multiplexing must be constantly powered in order to maintain a high input impedance to the off side of the multiplexer. Diodes provide power cross-strapping such that a power supplying failure on one side can be circumvented. The 510 ohm resistors isolate IC power lead shorts to ground. The enable lines are connected to V_{DD}, so that the multiplexer devices will be disabled when power to that side is off. The address lines are directly connected from the TIP CMOS control logic to the multiplexer address inputs.

The second level of multiplexing can be unpowered on one side while operating the other side. There are no power cross-strapping or isolation networks needed for the power connections.

As in the first level, the enable connections are connected to V_{DD}, and the address inputs are parallel and connected directly to the TIP control circuitry. Each bit line is buffered by a single N-channel open-drain driver with the drain connected to +10 volts through 47K ohms. The driver was chosen to convert +5V logic signals to +10 volt signals, which are compatible with TIP logic levels. In addition, unconnected multiplexer inputs will not cause excessive current to be drawn as is the case with COSMOS in general. The threshold voltage of the driver will range from 1.5 volts to 3.5 volts.

4.8.2.4.4 Digital A Data Inputs

Instrument Digital A data outputs will be received by the TIP on single output lines. These signals are cross-strapped internal to the TIP such that a single Digital A input gate failure will not contaminate other Digital A channels. The Digital A interface consists of a data line from the instrument to the TIP and a clock and data select interval from the TIP to the instrument. These signals are transferred using the standard "FAST" type TTL-to-COS/MOS or COS MOS-to-COS/MOS interface circuit developed for the TIROS-N spacecraft.

The clock signal is continuously available to all Digital A users. The select interval is enabled only when a particular Digital A data source is to be interrogated. When interrogated, 8-bits of data are shifted serially to the TIP for readout in the TIP output data stream. For contiguous sampling of the same data source, data will be accepted by the TIP in 8-bit increments. A narrow pulse will separate contiguous select intervals.

The TIP furnishes the instruments with pulses to synchronize their operations with the data collection activities of the TIP. A TIP major frame sync pulse, 128 sec sync, or 256 sec sync pulses are provided. The 128 sec and 256 sec sync pulses are used for instrument calibration purposes. These signals are transferred to users on standard interface circuits.

4.8.2.4.4.1 Digital A Multiplexer. The Digital A multiplexer is contained on the cross-strapping and interface board A10. The multiplexer commutates up to 16 Digital A inputs which are cross-strapped prior to multiplexing. Multiplexing is accomplished using the National 54C151 8-channel digital multiplexer. The multiplexers are powered from the +10V Interface Bus, which is supplied to the TIP by the spacecraft. The TIP side selected for operation controls and powers its respective control and data selection logic. The only interaction between redundant halves is through the cross-strapping connections.

The cross-strapping configuration simply consists of two isolating resistors commonly connected at the signal source with the other ends connected to the associated redundant input channel. The resistor values were chosen such that a gate short to ground or the +10V supply internal to the 54C151 will not interfere with operation of the redundant side. The input filter required at the receiving end of each Digital A signal is consistent with the specification for the "FAST" type standard interface circuit.

The 54C151 digital multiplexer devices are powered continuously from the +10V Interface Bus. To insure redundant operation and to protect the +10V Interface Bus from IC power shorts to ground, a 510 ohm isolation resistor is connected in series with the chip power line; one to each redundant 16 channels.

The output of each redundant eight channels of multiplexing is connected to CD4049 buffers which contain a special input protection network which allows input signals to be present when power is not applied to the buffer. If these special devices were not used, it would be possible for the disabled TIP side to become powered through the interface.

4.8.2.4.5 Command Verification

The TIP provides the means for telemetering command status information for uplinked real time commands. A 16-bit word is used to determine verification of receipt of an uplinked command, or execution of the command, or status information if the command was rejected.

The command verification source buffer is located in the CIU. Four signal lines between the TIP and the CIU are required for data transfer. A start signal is generated by the CIU as an indication that it is ready to send the verification word. The TIP responds by generating a transfer signal which is received by the CIU. At the time of receipt, the CIU transfers the data with a CIU generated shift clock. When the 15th bit is received by the TIP, the transfer signal which was presented to the CIU is terminated. The transfer operation is asynchronous with the TIP minor frame. The TIP will store the word until the appropriate interval for insertion into the TIP output serial bit stream. The maximum delay from receipt of the verification word to inclusion in the main frame is one minor frame (0.1 sec in orbit; 0.05 sec in boost).

CV data for the mission is inserted in the format in words 6 and 7 in orbit modes and words 8 and 9 in boost mode. The selection is controlled by the CV enable and digital A shift clock.

In order to assure complete transfer of the CV word, a cutoff time must be established prior to readout. Since transfer from the CIU takes approximately 200 sec, the cutoff must be established sufficiently prior to readout into the minor frame to take this into account. A convenient cutoff is the Minor Frame Sync which is generated in the TIP. This allows 1.5 milliseconds in boost mode and 5.7 milliseconds in orbit modes for the transfer of a CV word.

When the CIU has a word in its buffer, it sends the start signal to the TIP. When the TIP is ready to receive the word, it sends the transfer signal back to the CIU. The CIU synchronizes this signal to its own clock and transfers the 16 bit word to the TIP at a 102.4 kHz rate. If a start signal is not received before Minor Frame Sync, then transfers will not be allowed until after a readout has been completed. If a start signal is received after Minor Frame Sync, but before readout, a transfer signal will be returned after readout. Since the CIU does not have a bit counter, the TIP must keep track of the bit count. The transfer signal must be reset at the center of bit 15.

When a new word is received from the CIU, a flag is set which is inserted in word 3 of the format. This indicates that the CV data is new. Old data is recirculated in the buffer when it is read out and will be read out in all successive frames until a new word is received. The flag is reset after the data is read the first time.

4.8.2.4.6 Command Data Buffer

The Command Data Buffer (CDB) receives command data from the CIU. The data transfer from the CIU will be one or two 16 bit words depending upon the type of data. Mode data and Time Code Day Preset are one word transfers, while Time Code Millisecond of Day Preset is a two word transfer.

When the CIU has data to transfer to the TIP, it activates the start signal. If the CDB is ready, it returns the transfer signal to the CIU. The CIU then sends the data and a clock to the CDB. Since the CIU does not have a bit counter, this function must be supplied by the TIP. The CDB raises the transfer line during bit 15 to indicate to the CIU that there is only one bit remaining to be transferred.

The CDB is considered to be ready when any previously transferred data has been accepted by the appropriate buffer logic, such as the Time Code Counter, Mode Register or Dwell Address Register. This prevents loss of any command data.

In order to simplify data distribution, all data is shifted to the MSB end of the buffer. Therefore, in the case of a one word transfer, backfill will be generated to move the data to the end of the buffer. There is, obviously, no need to generate backfill in a two word transfer.

When the last word of a transfer is received, the CDB raises a flag to either the Mode Buffer or the Time Code Counter logic to indicate that new data is present in the buffer. The CDB does not respond to any new start signals until the appropriate buffer has returned a data accepted signal. If a new start signal has been received from the CIU, a transfer will be initiated as soon as the data has been accepted by the other logic.

4.8.2.4.7 Time Code Generator

In addition to data formatting, the TIP contains a ground presetable time code generator which provides a time record of data as it is sampled once every major frame. The time code generator is binary coded to count milliseconds of a day and day of year. Time code data appears in all TIP formats as a 40-bit word organized as shown below:

9-bit day count LSB	4-bit spare 0 1 0 1	27-bit millisecond of day count MSB LSB

The time code data pre-empts subcom telemetry during minor frame 0 and is the time referenced to the beginning of the minor frame to within ±1 msec. Also, Time Code Data is presented to the MIRP, for inclusion in its formatted output data stream, once every millisecond.

A time-code-error-correction capability is also included. The day count is preset in real time upon ground command. The millisecond-of-day count is preset upon receipt of command data from the CPU/CIU. Correction information on the millisecond-of-day count is loaded into the CPU by ground command. The CPU determines the correct time referenced to the trailing edge of the CIU 1-second sync signal. Command data is sent to the TIP prior to the sync transition at which time execution takes place.

The format for the Time of Day is nine bits of binary Day-of-Year (DOY). This is counted from zero to five hundred eleven days and then resets to zero again. The Milliseconds-of-Day (MOD) is twenty seven binary bits. Since there are

86,400,000 milliseconds in twenty four hours, the counter runs from zero to the binary equivalent of 86,399,999 and resets to zero. At this time, the DOY counter is incremented by one.

The DOY and MOD counters may be independently set to any predetermined number. This is accomplished from the CPU via the CIU and the Command Data Buffer (CDB) located in the TIP. Error correction is also implemented by the CPU following the same data path as preset. At a positive edge of the 1 Hz clock, the CPU computes the time at the next negative edge and transfers it to the CIU, which in turn sends it to the CDB. The CDB raises a TCC Data Flag to the TCC logic. If the flag is active when the 1 Hz goes negative, then on the next 1 kHz edge, the data is loaded into the MOD counter. The 1 kHz clock used by the MOD counter is divided down from the 360 kHz clock from the CIU. DOY data is loaded at the next 1 kHz after receipt of the command. After data has been loaded, a data accepted pulse is returned to the CDB logic, which removes the Data Flag.

The output interface to the MIRP is a 40 bit burst at 66.56 kHz occurring once every millisecond, transmitted MSB of the DOY first. The TIP time code is loaded into a register at the beginning of every minor frame. During word 0 of a major frame, which is every 320 minor frames, the time code is read out in place of the analog and digital subcom's by a Digital A type interface.

The MOD counter is a twenty-eight bit shift register that, in conjunction with the serial adder, recirculates the MOD count, incrementing it as it shifts. Only twenty-seven bits are needed for MOD count. The spare bit essentially acts as a carry reset for the serial adder. The register is characterized as parallel in, parallel out, serial shift register. Parallel load is synchronous with the clock and there is an asynchronous jam reset.

4.8.2.4.8 CPU Telemetry

The TIP accepts digital data from the CPU via the CIU during normal mission mode and launch mode. The TIP outputs data of the type selected in the order received.

During the appropriate intervals the TIP generates the data enable signals as a request for data. These signals are:

Enable CPU A Telemetry Enable CPU B Telemetry	- in Orbit Mode
Enable CPU Dump Data	- in CPU Dump Mode
Enable CPU Launch Telemetry	- in Boost Mode

In addition, the TIP generates the CPU data transfer signal which instructs the CIU to initiate the data transfer sequence. When the transfer pulse is received, the CIU data is output to the TIP by a CIU derived shift clock.

In the launch mode, CPU data is transferred to a TIP buffer in five 16-bit word bursts every 0.01 sec (8000 bps) for inclusion in the TIP output data stream. In the mission mode, CPU data from both CPU A and CPU B is transferred to the TIP in 3 word bursts at a 480 bps rate for each source.

The CPU Telemetry Buffer receives CPU telemetry from the CPU via the CIU. Readout of the buffer is controlled by a digital A type interface.

There are two modes of operation for the CPU Telemetry Buffer. In orbit mode, six 16-bit words are transferred from the CPUs - three from CPU A and three from CPU B. CPU A telemetry is read out in the first half of the minor frame, CPU B telemetry in the second half of the minor frame. CPU A telemetry is transferred from the CIU in the second half of the minor frame, CPU B telemetry is transferred in the first half. In boost mode, the PCU in control transfers five 16-bit words. The TIP design can accommodate five to seven words by means of external harness wiring.

The interface to the CIU/CPU is not a standard interface. Instead, the TIP generates a telemetry enable signal, which causes an interrupt in the CPU. Then the TIP generates a transfer signal and the CIU will transfer data and clock when it is ready. At bit 15 the TIP will terminate the transfer signal. In orbit mode, the transfer signal will be generated two more times. In boost mode, it will be generated four more times. After all words are transferred, the enable will also be terminated, Enable signals are generated twice per minor frame in orbit mode, which is once every 50 milliseconds, and five times per minor frame in boost mode, which is once every 10 milliseconds.

Adequate time is allowed to transfer all the data, however, it is possible that the CPU is occupied with a higher level interrupt. In this case a telemetry cutoff signal is provided such that there is sufficient time to backfill the registers with an alternating 1-0 pattern before readout begins. There must be sufficient time to backfill the buffer. The worst case is boost mode, when three milliseconds are allocated to backfill. A full 128 bits at 66.56 kHz will take 1.923 milliseconds which leaves 1.077 milliseconds spare time. If a complete set of words is not received by the cutoff, a flag is set to indicate that the transfer was not received in entirety. In orbit mode, there is one flag for each of the two transfers during a minor frame. In boost mode, there are five flags, one associated with each of the five sets of transfers.

The Start/Cutoff Sync Logic synchronizes the start and cutoff signals to the 66.56 kHz-N. The sequencer runs on 66.56 kHz which guarantees no timing problems. State 1 resets the start signal and State 4 resets the cutoff signal. State 2 is used to prevent the sequencer from getting locked into an unused state.

The interface logic and transfer sequencer has a telemetry enable flop, which when set by State 3 generates an enable signal. This signal is gated with boost or dump modes to enable boost or dump telemetry. When the signal is gated with orbit and the 1, 2 select signals, it enables CPU A or B telemetry. This flop is reset when all words are received or when cutoff (State 4) is reached. This box also has the transfer flop which is set by State 7 and reset upon receipt of bit 15. The transfer sequencer synchronizes receipt of bit 15 and generates the required delay. If all the words have not been received, it sets transfer again. If all words have been received, then it resets the telemetry enable flop.

The CPU data flag is the state of the last word received signal when State 4 is reached. However, this has to be delayed one bit time because the first word read out in a minor frame was actually transferred at the end of the preceding frame. Flag bits 4 and 5 become CPU A and B in orbit modes.

The bit counter is clocked by the CPU data Clock or the backfill clock. The carry out of the bit counter clocks the word counter. The word counter also has a decode gate to stop backfill when 128 bits have been loaded into the registers. There is also an And/Or Select that is controlled by boost mode to select between three words for orbit mode or five words for boost mode as the last word received signal.

The clock selector steers clocks to the two registers, the bit counter and the reclock flop in the readout selector. The CPU data clock and the backfill clock go to one register and the bit counter. The readout clock goes to the other register and the readout selector. The clocks at the registers are controlled by the 1, 2 select flop. The backfill clock generator must always be started; it is stopped when the word counter indicates that the buffer is full.

The data selector directs CPU data or backfill data to the registers. There is also a flop that is toggled by the backfill clock to generate the alternate 1-0 pattern for backfill. The readout selector, under control of the 1, 2 select flop, selects either register 1 or 2 for readout. There is also a reclock flop and the tristate serial data bus driver.

4.8.2.4.9 Subcom Telemetry Output to the CIU/CPU

TIP subcom information is available for transfer to the CIU/CPU during all TIP operating modes except for boost mode. The data sequencer generates a data load signal which lasts eight TIP word times and starts two word times prior to the output of minor frame subcom data (Word 6 in orbital modes and Word 38 in boost mode). The data load signal inhibits any attempt by the CIU to transfer data when the TIP is updating its buffer with new data. In synchronism with the start of the data load signal, an address enable signal is generated by the sequencer to permit parallel loading of subcom address and major frame address data into a 16-bit storage buffer. The address data is then serially shifted into a 64-bit serial data buffer. Addition of the 16-bit buffer allows the CIU the maximum time to asynchronously transfer data from the TIP to an internal buffer in the CIU (90 msec maximum in orbital modes and 45 msec in boost). When 16-bits of address have been stored, the address enable signal is terminated allowing the TIP minor frame serial output, containing the subcom data, to be serially shifted into the 64-bit serial buffer.

When the remaining 48 bits of data have been stored, the subcom telemetry transfer signal to the CIU is activated for one bit period at the TIP output data rate (1/8320 sec in orbital modes and 1/16640 sec in boost mode). In response, the CIU generates the subcom TLM clock signal which shifts data out of the TIP into a buffer internal to the CIU. The CIU shifts data in bursts of 16-bits until all 64-bits have been transferred.

4.8.2.4.10 Output Data to the MIRP

TIP data is transferred to the MIRP serially on a word basis during all orbital operating modes. Data is serially shifted into a serial buffer on the positive going transition of the BRC $\phi 3$ clock. When a complete 8-bit TIP word has been loaded, the data is asynchronously parallel-transferred into a storage buffer, ready for transfer to the MIRP. The MIRP word rate clock, which is generated by the TIP, provides the means for establishing word synchronization and for data transfer. At the time of transfer, the TIP supplies the MIRP with a

data ready indication. In turn, the MIRP responds to the transfer request at any time between 15 μsec and 350 μsec from the start of the data ready request. Data transfer is accomplished with the MIRP supplied clock (66.54 KBS). When the first positive transition of the MIRP clock occurs the TIP will terminate the data ready signal. In addition, the MIRP is supplied with a sync signal which allows the MIRP to synchronize the beginning of a TIP minor frame of data with its internal timing operations. The sync signal occurs periodically once ever TIP minor frame (0.1 sec).

4.8.2.4.11 A/D Converter

Analog-to-digital conversion is performed using the classical method of successive approximation. The dual A/D converter board, A5, contains two converters, one for each redundant side of the TIP. A single converter contains the appropriate successive approximation logic, a D/A converter, the third level of analog multiplexing (including voltage follower), the sample and hold network, and a comparator. In addition, a precision calibration voltage source, independent from the converter reference, supplies calibration telemetry.

The A/D converter operation is initiated by the analog word signal. This signal is used to inform the converter logic that the analog signal present at the output of the voltage follower is to be sampled and converted to digital data. The sequencer in turn generates the A/D power enable signal which enables switched power to the analog circuitry of the converter. At a time three-quarters into the word period, the A/D convert signal is generated. As a result, the analog input signal is held for conversion. The converted data is stored in an 8-bit holding register. At the appropriate time, an analog word transfer signal is generated which transfers the converted word into an 8-bit buffer for digital combining into the TIP serial output bit stream.

4.8.2.4.12 DC/DC Converter

Each TIP DC/DC converter board (A1/A16) provides ±10V quality, +10V logic, and +5.2V logic power. The quality buses are used exclusively for analog circuitry. In addition, the board contains a power on reset circuit, analog voltage telemetry circuits, and the +28V S/C power switching circuitry. Power selection to redundant TIP units is accomplished such that a single point failure will not contaminate both units. Each power supply unit contains a DC/DC converter and four voltage regulators, which serve as the interface between the spacecraft power source and the load electronics.

The DC/DC converter is a high-efficiency, two transformer square wave oscillator with the low power transformer operating in the saturating mode and the high power (output) transformer operating in the linear mode. The input to the converter contains an RFI filter and an LC filter to reduce the chopped currents that are fed back onto the spacecraft regulated bus. The oscillator is transformer-coupled to each of the four voltage regulators. The input squares waves are rectified, filtered and series regulated. The series regulators use negative feedback to control the output voltage and impedance.

4.8.2.4.13 Output C s-strapping

Cross-strapping is provided to interface the redundant TIP to redundant and non-redundant units on the spacecraft. Cross-strapping is implemented such that:

1) Any cross-strap failure will at most compromise one output interface; and

2) Any cross-strap failure will not damage the Interface Bus or the TIP control logic.

Failures are considered to be single point failures and that no failure occurs in the harness or wiring.

In the case of non-redundant interfaces, the cross-strapping consists of NOR gates driving CD 4050 buffer/drivers. Output filtering is incorporated as defined for standard type interface circuits. The NOR gates are powered from the +10V Interface Bus, so that the 10V TIP can interface directly to the cross-strapping logic. The CD 4050's also provide level translation to allow the +10V TIP to interface to a +5V or +10V unit by simply connecting the +5V or +10V interface bus to the output drivers. The CD 4050 output drivers are isolated from the interface bus through a 51 ohm resistor placed in the power supply lead of the ICs. This way the interface bus is protected against shorts and the logic is powered regardless of which side of the TIP is selected. A one microfarad capacitor is used to reduce ripple.

The NOR gates and the AND/OR select gates have 510 ohm isolation resistors in the power supply leads to protect against shorts. Note that when one side is off, the inputs of the NOR gates see 75 ohm to ground through a diode. This represents a logic level low (the output is then low) and the powered side signals will propagate through the NOR gates.

The output cross-strapping for a redundant interface is similar to the non-redundant interface except that each Side 1/Side 2 signal drives two CD 4050s which in turn drive independent sets of AND/OR select gates. This arrangement provides isolation between sides. Each redundant output interface has a 51 ohm isolation resistor to protect against short. A 1.0 μf capacitor helps reduce ripple. AND/OR select gates also have 510 ohm resistors to protect the interface bus.

4.8.2.4.14 Parity Generator

The TIP provides an even parity check on data contained in minor frame word location 2 through 103, which includes the parity check bits. The check bits are included in all TIP operating modes except for dwell mode. Parity bits P1 through P6 provide an even parity check on data contained in the following minor frame words:

P1 - 2 through 18
P2 - 19 through 35
P3 - 36 through 52
P4 - 53 through 69
P5 - 70 through 86
P6 - 87 through 102 (including Bits 1 through 7 of minor frame word 103)

The parity generator portion of the parity logic simply consists of a modulo-2 adder (exclusive "OR" gate) and a D-type flip-flop. The generator determines whether the number of data "1"s within a given period is odd or even. The parity sequencer determines the start and end of the parity generating sequence. As parity check bits P1 through P5 are determined they are stored in a buffer for commutation in minor frame word 103. The parity word is treated similar to Digital A data. Parity bit P6 is calculated and inserted in the output bit stream in real time, since P6 includes a parity check on bits P1 through P5.

The parity decode signal, which feeds the parity sequencer, determines the parity sequence period as defined by P1 through P6. When the parity decode signal becomes activated, the sequencer generates the parity load pulse and the parity reset signal, respectively. The parity load pulse allows each check bit (P1-P5) to be read into storage. The parity reset signal resets the parity generator, which defines the beginning of a parity generating sequence.

4.8.2.5 Flexibility

4.8.2.5.1 Format Changes

The TIP provides flexibility in allowing format changes from mission-to-mission. This is made possible by use of IC Programmable Read Only Memories (PROM) contained within the TIP. Format changes are restricted to word assignments in the Orbital Mode and Boost Mode minor frame and the 1 sec and 16 sec analog subcom frame data formats.

The Orbit Mode minor frame word locations 6, 7, and 13 through 102 can be assigned to Digital A, Digital B, or Analog words. However, hardware constraints limit the placement of CPU A and CPU B digital telemetry. CPU A telemetry can be assigned to any word locations between word 24 and 51 inclusive. CPU B telemetry can be assigned to any word locations between word 74 and 102 inclusive. These telemetry are not confined to contiguous word locations.

In Boost mode, minor frame word location 20-25, 45-47, 62-67, and 82-87 can be assigned to Digital A, Digital B, or Analog words. Hardware constraints limit placement of CPU boost telemetry to the locations as shown in Figure 4.8.2-3.

The 1 sec Analog subcom and the 16 sec Analog subcom-1 frame formats are defined by PROM. Analog channel selection is restricted to TIP Analog Channels 256 through 383. These channels can be sampled in any order consistent with the frame lengths specified in the TIP Performance Specification. However, word 0 of the 1 sec subcom is restricted, since this word is reserved for Dwell data.

4.8.2.5.2 Interfaces

The TIP can accommodate existing standard interface changes i.e., CMOS to TTL to CMOS, without impacting TIP design. A simple wiring change and part substituation is all that is required.

The TIP is designed to handle up to 16 Digital A inputs for growth missions. All unassigned Digital A inputs are configured for COS/MOS sources. However, TTL sources can be accommodated simply by changing the value of the TIP interface pull-up resistor from 100K to 619 ohms.

Since each instrument package h : a unique set of interface signal requirements, Digital A output control signals are provided for NOAA-HIJ instruments only. In addition, sync signal changes to an existing interface can be accommodated by a simple wiring change.

The TIP provides the on board CPU with spacecraft status telemetry for performing on-board data processing. Minor frame word 13 in Orbital Modes and word 45 in Boost Mode are included in the data which is transferred. The word location offers additional flexibility in processing capabilities since it can be assigned to a Digital A, Digital B, Analog, or Subcom word.

The TIP provides a spare biphase redundant output for growth. If for some reason redundant NRZ data and clock signals are required, a simple wiring change will make these signals available in place of biphase data.

The TIP contains sufficient buffering and formatting capabilities to accommodate 5, 6, or 7 word (16-bit/word) transfer from the CIU during boost mode. This capability is programmed by wiring which is external to the TIP.

4.8.2.5.3 PROM Instruction Format

The organization of the PROM instruction address contains the capability for adding three additional analog subcoms. These subcoms can be under hardwire control or under PROM control, providing additional memory is added. The instruction address is set up to handle 16 Digital A and 16 Digital B words. Presently, 13 of each type are provided for. Growth capability for each requires minor changes in the TIP design.

4.8.2.6 Physical Description

The TIP consists of 19 circuit boards functionally partitioned to enable ease of modification and efficient test and debug. Present functional assignments are listed below.

Unique Boards	No. of Boards/Unit
Dual 128-channel Analog Multiplexer A2/A3/A4/A17	4
Dual 128-channel Digital "B" Multiplexer A14/A15/A18	3
DC/DC Converter A5	2
Dual A/D Converter A5	1
Programmer Logic A9/A13	2
Cross-strapping and Interfacing Board A10	1
Miscellaneous Logic Board A7/A11	2
CIU/CPU Buffer Board A6/A12	2
Interface/Misc. Logic Board A8	1
Harness Board A19	1

Each board is an Astro standard 6.6-by 6.5-inch assembly. These assemblies can carry up to 117 flat packs or 64 dual-in-line packages each. Each board has a harness-board connector of 100 or 120 pins and has located on the opposite board edge, space for mounting up to 128 usable pins of spacecraft harness connector (MICRO-DOT). The circuit boards, which have both a ground

and a power plane, are designed so that the integrated circuits are gap-welded to pins on the component side. On the wiring side, the units are interconnected by pincer welded wires connected to button-head terminals. This technology is fully automated from the point of schematic completion, through board fabrication and welded wiring. It enables ease of modification, high reliability processing, and minimum cost processing. In addition to the standard welded-wire boards, printed circuit assemblies carrying the same connectors and dimensionally identical to the welded-wire assemblies are used. These boards are not viable, i.e., DC/DC converters, high volume assemblies. The harness board through which the boards are interconnected are also of welded construction and are processed by the same automated drafting and fabrication system.

The entire assembly is housed in an aluminum container that is 8.750 inches high by 6.875 inches wide by 13.274 inches deep. The composite unit and container weigh approximately 15 pounds, and are designed to meet all spacecraft thermal and mechanical stress condition.

4.8.3 MANIPULATED INFORMATION RATE PROCESSOR (MIRP)

4.8.3.1 Requirements

4.8.3.1.1 General

The MIRP is a digital data processing unit which is required to operate as a part of the Data Handling subsystem. As a part of this subsystem, its primary function is to receive, process, and format AVHRR data into several simultaneous outputs for transmission to the ground. Additional data is internally generated by the MIRP for the purposes of ground synchronization, data identification, and measurement of AVHRR operational stability. Furthermore, the MIRP is required to interface with the TIP, AIP, CIU, XSU, and other spacecraft subsystems as shown in Figure 4.8.3-1.

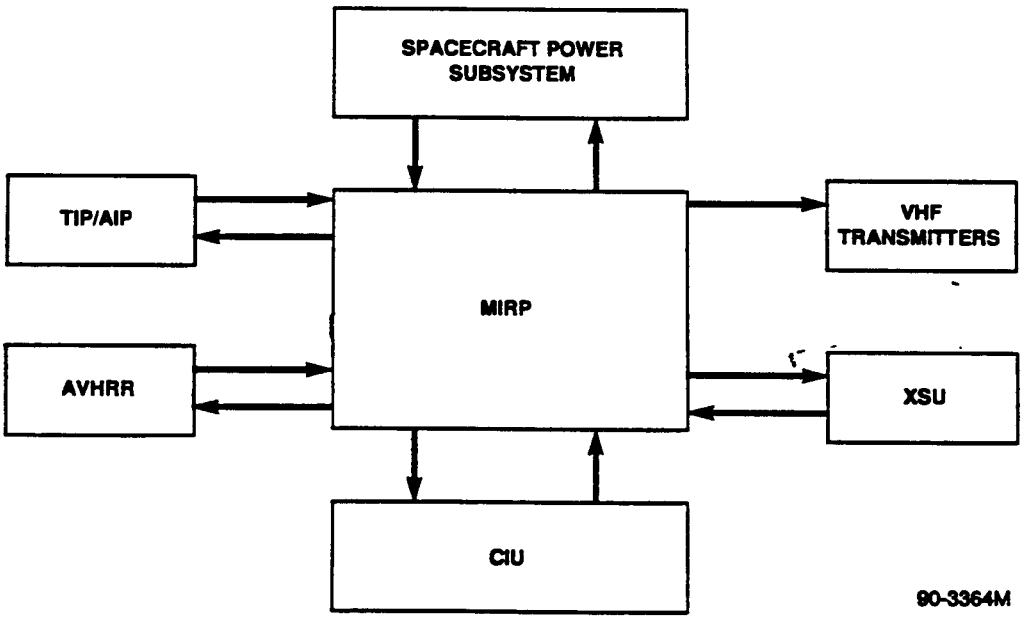


Figure 4.8.3-1. MIRP Operational Configuration

The MIRP is physically and electrically configured as a non-redundant assembly which contains its own DC/DC converter. When operating, it is required to perform the following basic functions:

a) Generate all internally required voltages from the +28 volt primary spacecraft power bus;

b) Provide a 0.9984 MHz clock to the AVHRR;

c) Accept and use external timing sources to develop all internal timing functions;

d) Respond to commands which establish internal states and operational modes within the MIRP;

e) Process AVHRR data into four different output formats, including one analog output;

f) Accept and buffer AMSU data and TIP data and time code outputs and insert them into the three digital output data formats;

g) Provide a means for randomizing the digital data on selected data outputs;

h) Provide for addition of parity check bits to selected data words;

i) Monitor and measure line to line AVHRR sync jitter and provide a means for rephasing the MIRP outputs to it if it exceeds a specified threshold;

j) Provide for operational back-up internal sync modes in the event of an AVHRR line sync failure;

k) Operate in two separate test modes using polynominal codes;

l) Interface and operate in a compatible manner with additional spacecraft subsystems as shown in Figure 4.8.3-1.

4.8.3.1.2 Interface

A more detailed description of the MIRP's position within the spacecraft system is presented in Figure 4.8.3-2.

As shown, the MIRP receives its primary power and ground inputs from the direct interfaces with the spacecraft power subsystem. Power from this input is used to operate the internal DC/DC converter; power switching is contained within the MIRP.

An additional +10 volt DC power input is supplied to the MIRP via an interface with the CIU. This is a specialized interface bus power which is used only to power certain input-output logic. Furthermore, the CIU interface provides the MIRP with all of its operational command data inputs.

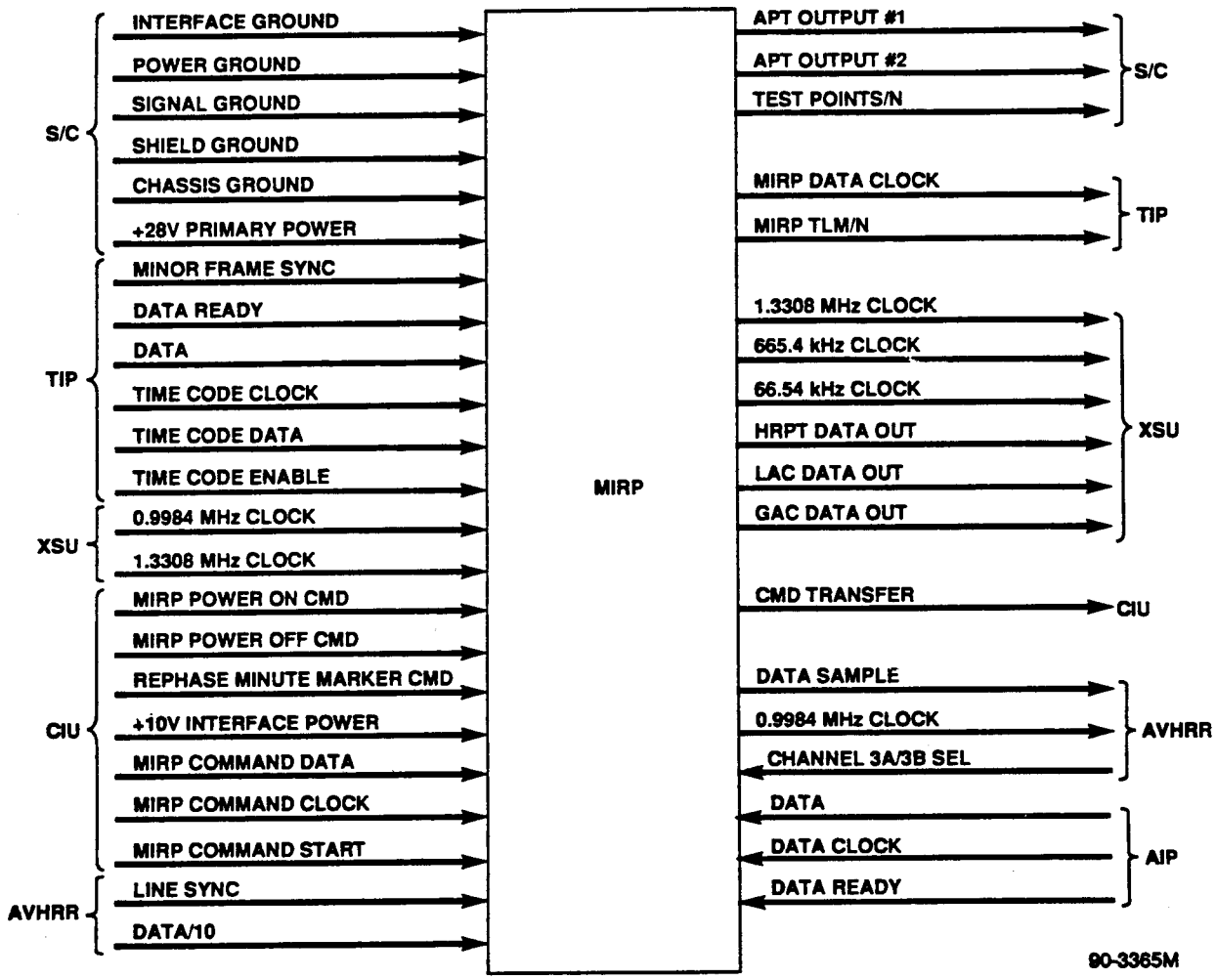


Figure 4.8.3-2. MIRP Interface Diagram

The MIRP interfaces with the XSU in order to receive the 0.9984 MHz and 1.3308 MHz primary clock inputs necessary for its operation. In return, the MIRP provides the XSU with three separate digital data streams with their associated data clocks. The XSU then cross-straps and switches the MIRP data to the proper Tape Recorder/Transmitter matrix.

The TIP interface lines provide for transfer of TIP Data and Time Code data to the MIRP. The MIRP buffer stores this data and then inserts it into the output frames at the proper times. In the other direction, the MIRP sends digital and analog telemetry outputs to the TIP.

The AIP transfers AIP data to the MIRP, which only uses the AMSU portion of the AIP data.

A dual interface exists between the MIRP and the two VHF transmitters which allows for direct transfer of APT analog data directly to the selected transmitter.

The last set of interface lines shown in Figure 4.8.3-2 are the primary interfaces with the AVHRR. The MIRP provides the AVHRR with its primary clock and a data sample line to initiate sampling of the digitized data at the proper times within each AVHRR scan line. In return, the AVHRR provides the MIRP with a line synchronizing pulse and ten parallel data lines which are the MIRP's primary source of data.

4.8.3.1.3 Command Requirements

The MIRP is required to alter selected operational modes and internal states in response to ground commands. Commands received by the MIRP will be in the form of a Pulse Discrete Command (PDC), or a Distinct Procedure Command (DPC). The command function determines which of the two forms is used. All commands are issued to the MIRP from the CIU.

The pulse discrete command is used for functions which are complementary parts, or for initializing or resetting purposes. For this type of command, each command function is assigned a dedicated command interface line. Activation of the command is accomplished by providing a 0.5 to 1.5 second pulse on the dedicated line. The MIRP uses the command pulse to latch an internal memory element such as a relay or flip-flop. For these commands, action is immediate; the MIRP responds to the command as soon as it is received.

A total of three Pulse Discrete Commands are required by the MIRP:

<u>MIRP Power ON</u> - Upon receipt of this command, the MIRP latches an internal power relay which connects the +28 volt primary spacecraft power to the internal DC/DC converter.

<u>MIRP Power OFF</u> - Upon receipt, the MIRP unlatches the power relay and removes the +28 volt power from the DC/DC converter.

<u>Rephase Minute Marker</u> - Upon receipt of this command, the MIRP resets the APT one-minute counter to a count of zero.

The MIRP also requires one DPC word to control the remainder of its commandable functions. Each DPC is initiated by the CIU and asychronously sent to the MIRP for execution. The DPC is a 16 bit binary word. Bits 1 through 3 and 4 through 6 of this word are each used to perform a 1 out-of-8 decode to determine which AVHRR channels are selected for the A and B sections of the APT output frame. Bit 7 is used to control the output data rephase operation; while bit 8 is used to control operation of a P-N code generated test mode output.

Bits 9 and 10 are used together to perform a 1-out-of-4 decode to determine which telemetry source is used in the APT output. Bit 11 determines whether the MIRP operates from AVHRR Sync or internal sync. Bits 12 and 13 are decoded to select incremental time shifts in the position of the internal sync. Bit 15 allows the MIRP to enter a special test mode which substitutes a P-N generator for the incoming AVHRR data. Bits 14 and 16 are currently unassigned and are treated as "spare" command bits available for future growth. (Most of the commands described above are detailed more explicitly later in this section.)

Each DPC word command bit is individually telemetered so that the exact operational mode of the MIRP is known at all times by observing the TIP telemetry data.

4.8.3.1.4 Operational Modes

The MIRP is required to operate in several distinct modes and many related sub-modes. The major operational modes are:

A) Normal Mode
B) Data Substitution Mode
C) Test Mode

When operating in Normal Mode, the MIRP is slaved to the AVHRR sync rate and uses AVHRR data to format its data frames. It takes a specified number of data samples at specified times during the 1/6 second AVHRR scan.

The data derived from this sampling process is then used to format four separate and simultaneous data outputs:

a) High Resolution Picture Taking (HRPT) Data;
b) Limited Area Coverage (LAC) Data;
c) Global Area Coverage (GAC) Data;
d) Automatic Picture Taking (APT) Data.

Both the HRPT and LAC data outputs utilize unprocessed AVHRR data to create the output formats. For the GAC data output, AVHRR data is processed according to a horizontal and vertical averaging algorithm which yields a lower resolution data. The APT output is the result of data processing which includes geometric correction, and averaging. The final output is an amplitude-modulated analog signal.

When operating in the Data Substitution Mode, the outputs are still processed as described above, however, the source of data input is an internally generated P-N code rather than AVHRR data. The substituted polynomial code is generated according to the equation $X^{11} + X^8 + X^5 + X^2 + 1$.

When operating in the Test Mode, the three digital outputs (HRP LAC, and GAC) are disabled. In their place is substituted a continuous P-N code which is generated according to the polynominal $X^{10} + X^5 + X^2 + X + 1$. During this mode, the APT output will operate normally using either AVHRR data or P-N substitute data in accordance with the present command status.

Each of the above modes, however, have related sub-modes:

A) Internal Sync Mode
B) Sync Shifting Mode
C) Sync Rephase Mode
D) APT Selection Modes

If the Internal Sync mode is commanded, the MIRP will use its own internal 6 pps sync in place of the incoming AVHRR sync. If the Internal Sync mode is operational, the Sync Shifting mode of operation may be additionally used to move the relative position of the sync pulse.

The Sync Rephase mode is normally operational and serves to maintain the MIRP output frames with specified phasing relative to the AVHRR scan. However, this mode may be disabled, so that the outputs are not locked.

The APT Selection mode has numerous combinations and permutations resulting from the selection of 1 of 5 AVHRR channels for each of two APT frame halves.

4.8.3.1.5 Output Data and Frame Organization

As previously noted, the MIRP is required to process AVHRR data into four simultaneous output data frames which are designated as HRPT, LAC, GAC, and APT. HRPT and LAC are both digital data outputs occurring at a minor frame rate of six frames/second. GAC is also a digital output, but it occurs at a frame rate of two frames/second. The APT output is an amplitude-modulated analog signal which occurs at a rate of one video frame every 64 seconds. The relative phasing between the four outputs is shown in Figure 4.8.3-3. Note that complete frames are shown for the digital data, but that only the first two video lines of APT Data are shown.

A more detailed presentation of the HRPT/LAC digital output frames is shown in Figure 4.8.3-4, while the GAC output frame is shown in Figure 4.8.3-5. Note that all frames are very similar in format, with only the numbers of words and output rates being different.

The HRPT and LAC frames are essentially identical, with the data being organized into three 11,090 ten bit word minor frames (Figure 4.8.3-4), which constitute a major frame. The minor frame rate is six frames/second which is identical to the AVHRR line rate. The minor frames are synchronized to the AVHRR reference pulse. The major frame rate of two per second is related to an integer number of TIP data samples. This simplifies the display of TIP data within the MIRP format. Each minor frame can be identified by a two bit data field in the identification word. The equivalent HRPT/LAC output serial data rate is 665,400 bps. The GAC data is organized into a 3,327 ten bit word frame (Figure 4.8.3-5). The frame rate is two frames/second and is equivalent to an output serial data rate of 66,540 bps. The frame is organized with 39 spare word positions contiguous with the TIP/AMSU data.

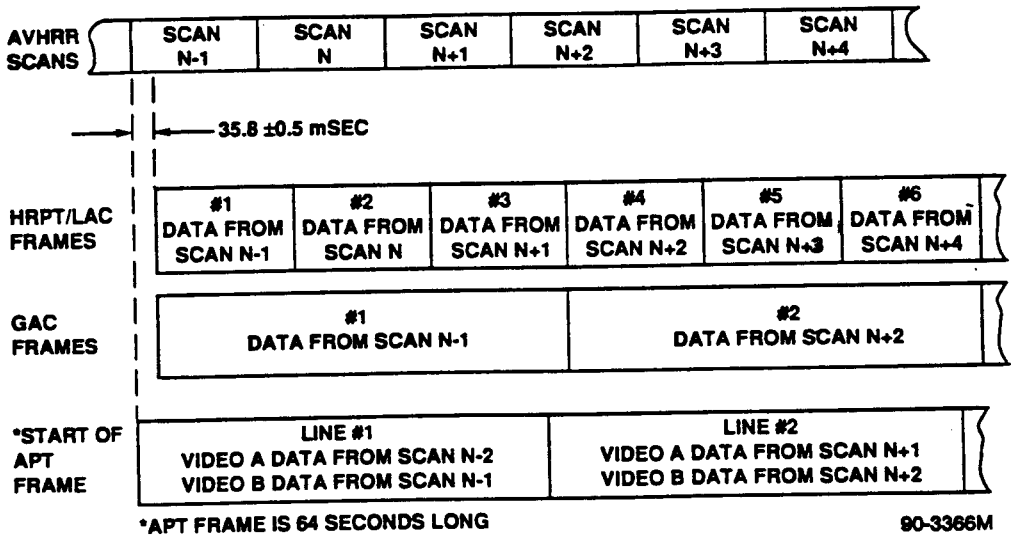
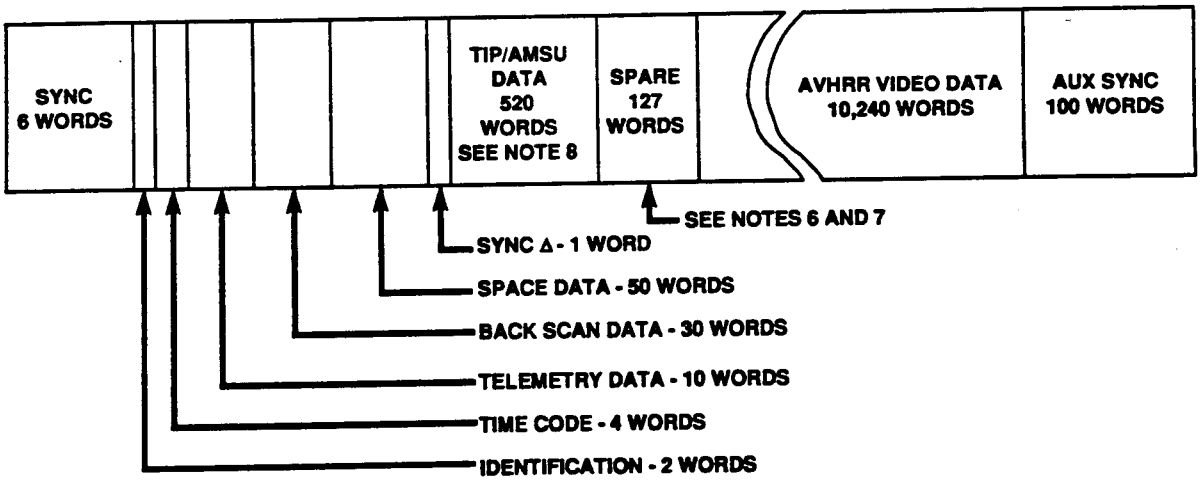


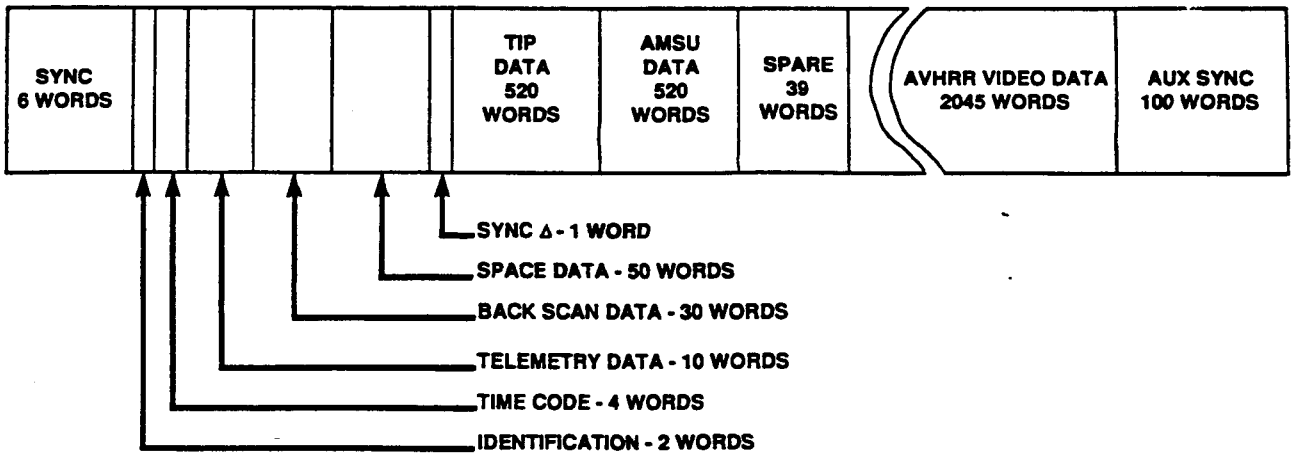
Figure 4.8.3-3. Relative Phasing of MIRP Output Frames



NOTES:
(1) MINOR FRAME LENGTH - 11,090 WORDS
(2) THREE MINOR FRAMES PER MAJOR FRAME
(3) MINOR FRAME RATE - 6 FRAMES/SECOND
(4) WORD LENGTH - 10 BITS/WORD
(5) WHERE BIT CONTENTS OF LAC WORDS ARE SPECIFIED (AS IN NOTE 7), THE SPECIFICATION APPLIES PRIOR TO DATA RANDOMIZING
(6) HRPT OUTPUT - ALL SPARES ARE 10TH DEGREE P-N CODE (BAR)
(7) LAC OUTPUT - ALL SPARES ARE DATA "0"
(8) TIP DATA IN FIRST FRAME; BACKFILL IN SECOND FRAME; AMSU DATA IN THIRD FRAME

90-3367M

Figure 4.8.3-4. HRPT/LAC Output Frame Formats



NOTES:
(1) MINOR FRAME LENGTH - 3327 WORDS
(2) FRAME RATE - 2 FRAMES/SECOND
(3) WORD LENGTH - 10 BITS
(4) SPARE WORDS SHALL BE DATA "0"
(5) WHERE BIT CONTENTS OF WORDS ARE SPECIFIED (AS IN NOTE 4), THE SPECIFICATION APPLIES PRIOR TO DATA RANDOMIZING

90-3368M

Figure 4.8.3-5. GAC Output Frame Format

As shown in both of these figures, the first 103 words of all digital frames is a standardized header structure. This header is allocated as shown in Table 4.8.3-1.

TABLE 4.8.3-1. HRPT/LAC/GAC/HEADER STRUCTURE

Word	Content	Notes
1-6	Primary Sync	Internally Generated
7-8	Identification Words	Internally Generated
9-12	Time Code	Supplied by TIP
13-22	Telemetry Data	
23-52	Back Scan Data	Supplied by AVHRR
53-102	Space Data	
103	Sync Delta Word	Internally Generated

The first six words of sync code are internally generated in the MIRP according to the polynominal $X^6 + X^5 + X^2 + X + 1$. This is the primary synchronizing data for ground lock.

The identification words which follow are used to carry information about the sync modes, minor frame ID, spacecraft address, and other MIRP status. The second ID word is currently unassigned and is designated as "spare". Time

code is supplied to the MIRP from the TIP, and is updated at a 1 kHz rate. Telemetry data is derived from sampling AVHRR data. The last header word is designated as the sync delta word which is an internally generated measure of AVHRR sync jitter. The allowable measurement range is $\pm 512\mu$ seconds.

The 520 words of TIP/AMSU Data which are contained in the digital formats consists of five contiguous frames (104 words each) of data supplied by the TIP/AIP. The data is furnished in 8 bit word lengths, which the MIRP converts to 10 bit words by adding two parity bits. TIP data appears in the first HRPT/LAC frames, backfill in the second, and AMSU data in the third.

A total of 10,240 words of Earth data is inserted into each HRPT/LAC frame. This data is unprocessed and is inserted into the frame in the same 5-channels-commutated format that is received from the AVHRR. However, the 2045 words of Earth Data inserted into the GAC frame is obtained by processing 10,240 data samples. The processing algorithm performs vertical data compression by using only every third AVHRR scan line. On the selected scan line, it performs horizontal averaging for (each of the five channels) by using an algorithm which averages four samples, and skips one. This reduces the 10,240 raw data words to 2045 averaged data words. The three additional left over words are discarded.

At the end of each digital frame is a 100 word P-N code which may be used as an auxiliary sync code. This is generated according to the polynominal $X^{10} + X^5 + X^2 + X + 1$.

All three of the above digital data frames are encoded in NRZ-L form as they are sent to the XSU. However, in order to assure that the data maintains a minimum number of signal transitions needed for processing, it is required that the MIRP perform randomization of the LAC and GAC data. HRPT data is <u>not</u> randomized since it is ultimately encoded in bi-phase by the XSU. This automatically provides the necessary transitions. Only the data between the primary sync and auxiliary sync is randomized. The randomization is performed by using the complemented output of the same 10th degree P-N generator used to develop the auxiliary sync.

The APT data output format is significantly different from the previous digital outputs. APT is an amplitude-modulated analog signal. Two channels of AVHRR data are time-division multiplexed into an output data stream. The AVHRR data is pre-processed to achieve both bandwidth reduction and geometric correction. The bandwidth and geometric correction algorithm employed is based on averaging each third line of AVHRR data using distinct algorithms for each of five regions defined by their subtended angle from the Nadir Pulse. The algorithm is summarized below:

Region 1 - ($\pm 17.3°$) - Average each contiguous group of four samples.

Region 2 - ($-34.7° \rightarrow -17.3°$, $+17.3° \rightarrow +34.7°$) - Average each contiguous group of two samples, skip one sample and repeat.

Region 3 - (-43.3° → -34.7°, +34.7° → +43.3°) - Average each contiguous group of two samples.

Region 4 - (-48.5° → -43.3°, +43.3° → +48.5°) - Consider a contiguous group of three samples, A, B, and C. Derive two output values.

$$\frac{A+B}{2} \text{ and } \frac{B+C}{2}$$

Region 5 - (-55.3° → -48.5°, +48.5° → +55.3°) - Use the input samples unmodified.

All processing is performed in the digital domain. The resultant output video is then D/A converted and filtered for multiplication into the output data.

The resulting format for one complete APT video line is composed of a sync interval, space data/minute marker interval, earth data interval, and a telemetry data interval. A total of 128 successive video lines form a complete APT frame. The line rate is two lines/second and the frame rate is one frame/64 seconds.

The multiplexed output data organization starts with a seven pulse synchronization signal. This signal will have a different rate for the each of the two video sections of the format. Sync A will be 1040 Hz and Sync B will be 832 Hz. Following the sync signals will be a time slot allocated to space data and minute time markers. The space data which is sampled for forty-seven periods of the 4160 Hz APT output clock will be derived from the first space data sample associated with the output channel which will be repeated forty times. The minute markers, which are derived from a command-resettable Minute Counter in the MIRP with 0.5 second resolution, overwrite the space data. These markers are repeated four times each time that they occur and are output as full amplitude video signals. Following the Space/Time Marker field in the format is the 909 samples video field. This is in turn followed by a forty-five period sixteen position TLM subcom field.

The table below defines the contents of the TLM subcom field, each sample of which is repeated for eight consecutive video lines.

1) Wedge 1 - Internally generated gray level
2) Wedge 2 - Internally generated gray level
3) Wedge 3 - Internally generated gray level
4) Wedge 4 - Internally generated gray level
5) Wedge 5 - Internally generated gray level
6) Wedge 6 - Internally generated gray level
7) Wedge 7 - Internally generated gray level
8) Wedge 8 - Internally generated gray level
9) Wedge 9 - Internally generated gray level (Zero Modulation)

10-13) AVHRR/2 Target Temperatures - 5 point subcom
14) AVHRR/2 Patch Temperature
15) AVHRR/2 Back Scan Sample
16) Channel Marker - Wedge signal corresponding to the channel being transmitted. For example if Channel 3b was being processed, Wedge 3 voltage step would be used in this slot. Wedge 6 is used for channel 3a.

The video reduction and geometric correction processing which produces 909 video samples has an effective bandwidth of 2080 Hz.

The signal is low pass-filtered prior to amplitude modulation to minimize frequency fold-over problems. The final APT output is AM modulated on a 2.4 kHz subcarrier and transferred directly to each of the 2 VHF transmitters, one of these transmitters is normally on full time to provide APT data.

4.8.3.2 Description

4.8.3.2.1 System Diagram

The complete block diagram for the MIRP is shown in Figure 4.8.3-6. The MIRP has its own DC/DC converter which converts the +28 Volt S/C power to the internally required voltages. There is a separate TIP Data and time code data block which interfaces with the TIP. It provides buffer storage for this data by utilizing 8192 bit dual memory banks; one for reading and one for writing. TIP data parity generators and read-out clock generators also reside in this section. Similar logic is utilized for the AMSU data.

A dedicated logic section serves to interface with the AVHRR. It contains all of the read-in clock generators, as well as data sampling logic, and the sync rephase logic.

Commands to the MIRP enter the command processing block where they are asynchronously received and stored to establish the operation of the other logic blocks.

The digital data processing sections consists mainly of dual memory banks for the storage of AVHRR data plus serial digital multiplex logic for the formation of the output frame formats. HRPT and LAC data is stored in common memory banks which are divided so that one is read while the other is written into.

GAC data processing is similar except that the AVHRR data is processed by the "Average four, skip-one" algorithm logic block prior to storage in memory. Approximately 130K bits of memory is required to provide buffering of the HRPT/LAC and GAC data input.

The APT data processing chain is separate from the HRPT/LAC/GAC logic. It consists of source selection logic, an arithmetic section to perform the APT algorithms, a dual memory bank for data storage, and a data formatter which is operated under PROM control. The multiplexed digital data is then D/A converted, filtered, and impressed upon a 2.4 kHz subcarrier.

All four of the MIRP data outputs and their associated clocks are individually buffered. The +10 volt interface bus is used for all input/output interface logic between the TIP, AIP, CIU, XSU and the MIRP. Specialized interfaces are used for signal paths between the AVHRR and the VHF transmitters. Telemetry and test points are also provided.

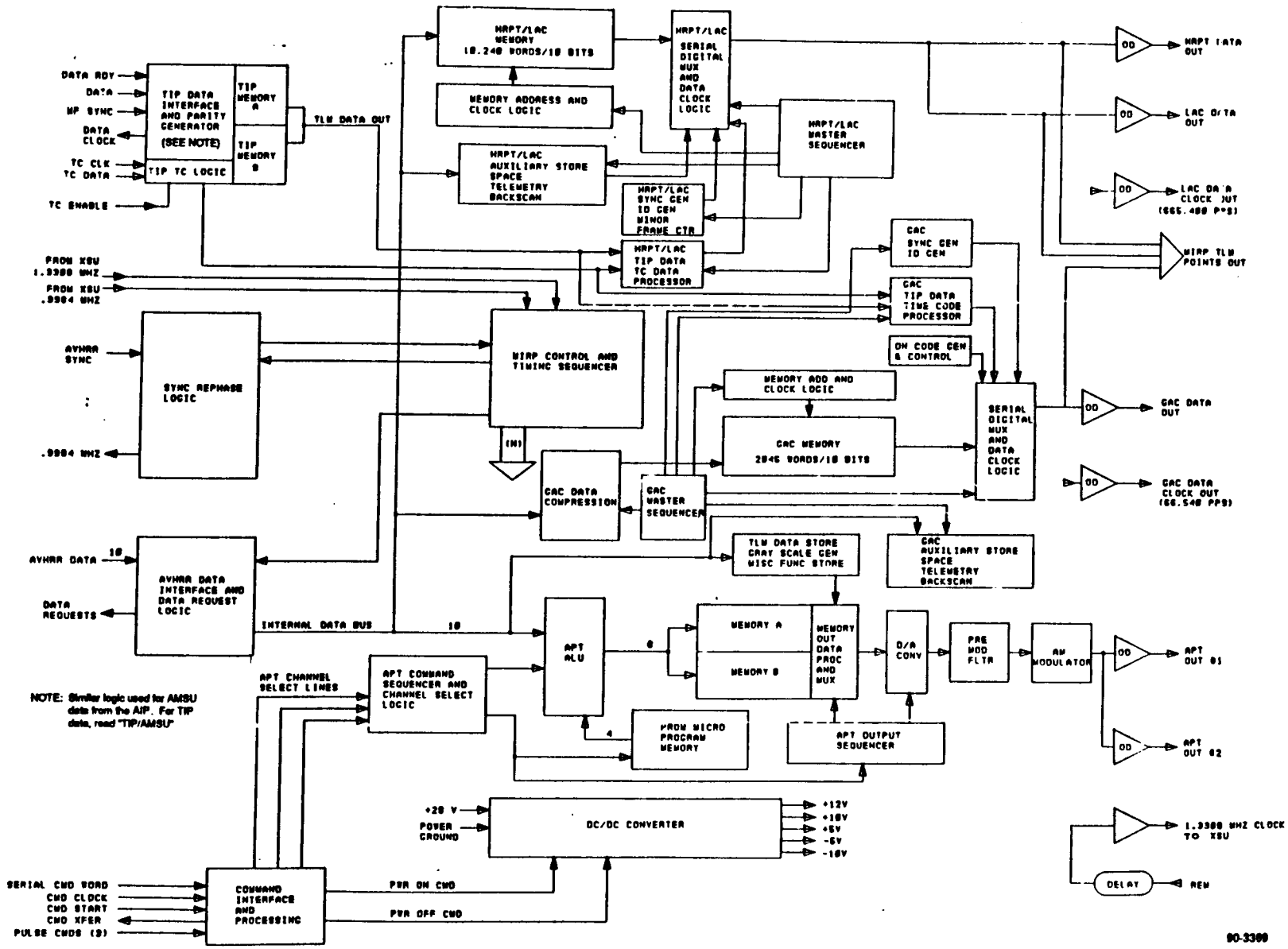


Figure 4.8.3-6. MIRP Block Diagram

4.8.3.2.2 MIRP Internal Clock System

The MIRP timing control pulses are derived from the two time base reference sources supplied from the XSU.

1. The Spacecraft Master frequency (SCM) of 0.9984 MHz which controls the information read-in rate;

2. The Readout Master frequency (REM) of 1.3308 MHz which controls the information readout rate.

These two reference frequencies are phase locked in a phase-lock loop system to maintain a constant ratio of $\frac{1,330,800}{998,400} = \frac{1,109}{832.}$

Each of the two reference frequencies is divided down in a Johnson counter. The outputs from each counter are decoded to provide multiple clock phases. Clocks associated with a particular counter are designated by a mnemonic symbol which completely defines that clock in terms of its frequency, phase, and duty cycle. Each mnemonic symbol consists of two parts:

1. A three-letter functional part defining the frequency and the reference source;

2. Set of numerals defining the phase, number of possible phases, and the duty cycle.

Thus, in a typical mnemonic symbol XYZ-k-n, the XYZ part identifies a particular Johnson counter from which the clock is derived, and thus the frequency and the reference source, n is the number of possible phases, k is the phase reference to phase 1 and the duty cycle is 1/n.

4.8.3.2.3 Command Processing

The MIRP receives all of its commands via the CIU interface. Pulse commands are simply buffered and then used to latch a memory element. However, the MIRP receives the majority of its commands in the form of a 16 bit serial DPC word. The DPC word, plus other associated control signals, are supplied to the MIRP from the CIU. This logical section receives the command data and holds it in buffer storage. The stored data is then used to control the operational modes of the MIRP.

This section consists primarily of a 16 bit command receiving register, a second level command storage register and an input command sequencer which controls the transfer of data from the CIU.

The transfer of command data is initiated by the CIU with a "Command Start" signal. When the MIRP is ready to receive the command, it responds with a "Command Transfer" signal. The CIU then clocks 16 bits of data into the MIRP's command receiving register. Data is transferred at a 102.4 kHz rate with the CIU shifting data on the negative-going clock edges, and the MIRP accepting it on the positive-going clock edges.

Control of data flow in the MIRP command receiving registers is provided by the input command sequencer. When a command is initiated, the sequencer sets the bit 1 position of the command receiving register to a data one and all other bit positions to data zeroes. Then as the command data is shifted in, the data one bit propagates down the register until it causes termination of the "Command Transfer" signal at the center of the 15th bit cell. The CIU continues clocking for one more bit to complete the 16 bit load. The sequencer then transfers the command data to the second level storage registers and performs inversion of the data at the same time.

All interfaces between the CIU and the MIRP are standard CMOS to CMOS "fast" interfaces operating from the +10V interface bus and return.

Telemetry for each of the 16 command bits is provided to the TIP. The outputs are Digital B type which provide 0 to +5 volt digital outputs.

4.8.3.2.4 TIP/AMSU Data Processing

The 8320 bps TIP data and the 8320 bits of AMSU data (input at 16.64 kbps), are input as serial data streams, and displayed in the HRPT/LAC and GAC formats. Data transfer to the MIRP is accomplished via a simple timing transfer routine. When the TIP (or AIP) output register is full, it sets a "Data Ready" flag; when the MIRP is ready it acknowledges the flag and supplies with cycles of a 66.54 kHz "Data Clock" to TIP. The positive transition of the clock shifts the data in the TIP serial output register and the negative transition stores the data in the MIRP. The first positive transition of the "Data Clock" resets the "Data Ready" flag. The AMSU portion of the AIP data is read in a similar manner, but with a 16.64 kHz clock, and the Data Ready, Clock, and Data are all provided by the AIP without handshaking from the MIRP.

A block diagram of the processing logic is shown in Figure 4.8.3-7. It consists primarily of memory and address logic, phasing logic, and a parity generator. Two memory banks are utilized. Each one consists of 16k bits of static C-MOS RAM. Thus, each memory bank has sufficient capacity to buffer five complete frames (0.5 seconds worth) of Data.

The MIRP receives and uses TIP minor frame sync to perform synchronization of the memory banks with the beginning of a TIP frame. The incoming TIP data is organized into eight bit words. The MIRP processes each word by adding an even parity bit in the ninth position and the inverse of the first bit in the tenth position. This coding enables a single bit error detection, and the detection of bit slip. The coding also guarantees a minimum transition density of ten percent, and increases the word size to ten bits which is the MIRP standard. TIP and AIP data, as presented in the MIRP formats, are each grouped in sets of 520 words. This is equivalent to one-half second of TIP data and one-half second of AIP data.

In the HRPT/LAC Processing, the collected TIP data is displayed in the first minor frame. The MIRP provides backfill during the second frame and AMSU data is displayed in the third frame. In the GAC Processing the 520 words are read out once per half second frame. In all modes, the formatted TIP data is read out contiguously and the AMSU data is read out contiguously. Readout of data from the memory banks is controlled by the multiplex logic related to the HRPT/LAC and GAC formatters.

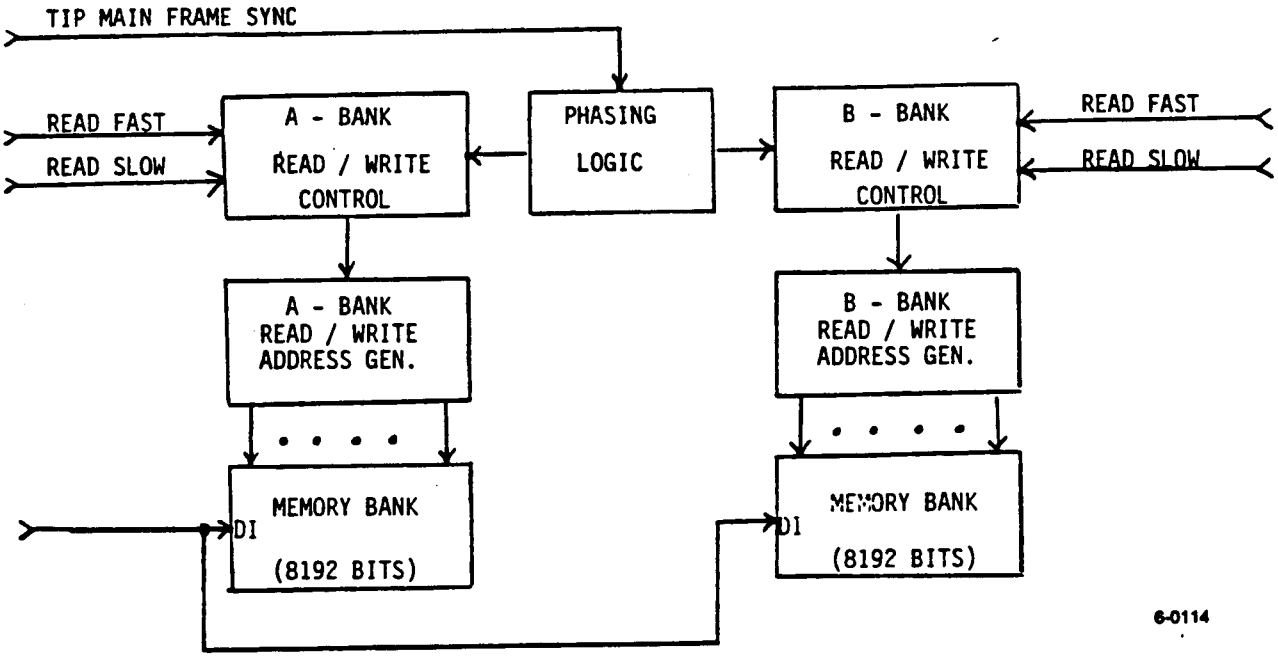


Figure 4.8.3-7. TIP Data Processing

The TIP and AIP are redundant units which provide all required cross-strapping internally before supplying the interface signals to the non-redundant MIRP and processes all single MIRP signals to the TIP/AIP to enable redundant TIP/AIP operation.

4.8.3.2.5 Time Code Processing

The MIRP receives time code data from the TIP and includes it in all digital output formats. The code is formatted in the NASA standard format and consists of 40 bits. The 40 bits of data are transferred from the TIP to the MIRP. The transfer occurs at a 66.56 kHz rate and is updated 1000 times/second. The MIRP receiving register is constantly allowed to update itself, except when a read-out into the output format is required. When this occurs, the update process is inhibited and the time code data is multiplexed directly into the output format. The inhibit process is properly phased to assure that the register always contains a complete code. It does this by allowing any update in progress to be completed before read-out begins. The time code register is interrogated four times per major frame, i.e., three times for HRPT/LAC and once for GAC. Updates occur between interrogations.

4.8.3.2.6 AVHRR/3 Data Sampling Process

The AVHRR/3 is the primary source of data for the MIRP. The interface connection between the MIRP and AVHRR/3 consist of a line sync pulse, a data sample pulse, and ten parallel output data lines. Both the AVHRR/3 and the

MIRP use the 0.9984 MHz clock as their primary timing source. This is provided to the MIRP by the cross-strap unit (XSU). The MIRP provides it to the AVHRR/3 in the proper phase to be consistent with MIRP processing.

The AVHRR/3 scan position is independent from the MIRP. The AVHRR/3 provides the MIRP with a 6 pps line sync pulse preceding each of its scans. The MIRP uses the sync pulse to index the timing of its sampling pulses so that the data is sampled at the proper interval during each scan. Both units are synchronous with the 0.9984 MHz clock. When each radiometer scan line is started, the AVHRR/3 provides a 100μ sec line sync pulse to the MIRP. The sync pulses occur at a nominal 6 pps rate. Upon receipt of the sync pulse, the MIRP begins a data sampling process which takes a specific number of samples at specified times during the scan line. The sampling process is initiated by the MIRP which outputs a data sample pulse to the AVHRR/3. The sample pulse is one clock period wide and is phased so that the negative-going edge of the 0.9984 MHz clock is centered within the sample pulse. When successive sample pulses are generated, they are output to the AVHRR/3 every 25 clock periods.

When the AVHRR/3 receives the sample pulse, it sequentially outputs five channels of digital data in the form of 10 bit parallel words. The order of the output is channel 1, channel 2, channel 3, channel 4, channel 5 with all channel data lasting for five clock periods. Transitions from channel to channel occur on the negative transitions of the clock. Channel 1 data becomes valid five clock periods after the center point of the data sample pulse. Channel 1 data ends and channel 2 begins after 10 clock periods. The process is continued until all five data channels are read out. The MIRP samples and stores the data from each of the channels at a time which is one clock period before the data is due to change.

Within each scan line interval, the MIRP performs data sampling in six different areas. These sampling areas are Space Data, Ramp Calibration, Earth Data, IR Target Temperature, Patch Temperature, and Back Scan Data. Each interval is available for sampling for a unique period of time. In some intervals, the AVHRR/3 only provides valid data on channels 3 and 4. MIRP sampling of each data interval is centered within the available time, and a different number of sample pulses are generated with each interval.

During the Space Data Interval, 10 data sample pulses are generated. The first pulse occurs 2.529 milliseconds after line sync, and the last pulse occurs at 2.754 milliseconds after sync. During this period, the MIRP has received 50 data words for processing, i.e., 10 words for each of the five channels.

Ramp Calibration data is sampled once, and results in 5 data words, one per channel. The MIRP samples the Earth Data period 2048 times, and retrieves 10,240 data words.

I.R. Target Temperature and Patch Temperature intervals are sampled once in the center of each interval. One data word is obtained from the channel 3 position in each interval. Both of these data intervals are sub-commutated once every five AVHRR/3 scans.

During the Back Scan period, the MIRP samples the AVHRR/3 ten times, but only uses the data from channels 3, 4, and 5 to obtain a total of 30 words.

Each of the sampling processes detailed above are performed for every AVHRR/3 scan line; i.e., six times per second, In those intervals where multiple samples are taken, the sampling is uniform and continuous at a rate equal to 25 periods of the 0.9984 MHz clock.

4.8.3.2.7 HRPT/LAC/GAC Data Processing

All data originates at the AVHRR input and thereafter diverges into four distinct processing paths. One path leads to the HRPT/LAC memory bank, while another leads to the GAC data compression logic before going to the GAC memory bank. The other two paths lead to auxiliary storage memories for HRPT/LAC and for GAC.

The main memory for the HRPT-LAC processing is composed of CMOS static RAMS and provides approximately 123 kilobits of storage capacity. The organization of the HRPT-LAC memory is shown specifically in Figure 4.8.3-8. It is word organized in three 4096 x blocks. This provides for 10,240 ten-bit words of HRPT/LAC data storage with half of the last 4096 x 10 block being unused. Due to the asynchronous nature of the read and write rates, an active block cannot be used to read and write at the same time. Thus, it is required that the reading and writing of the A, B, and C sections of the memory banks be staggered.

The front end of the GAC processing chain is more complicated due to the averaging required. It consists of two parallel paths.

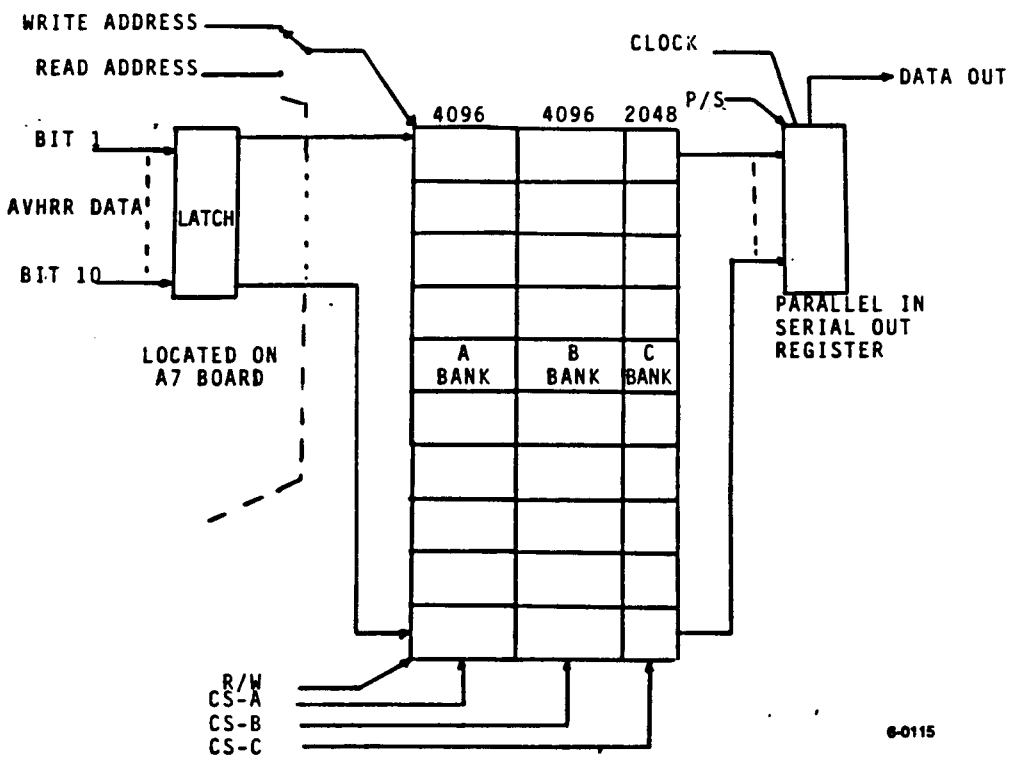


Figure 4.8.3-8. HRPT/LAC Memory Block Diagram

In order to provide sufficient time to average four AVHRR samples of each of the five channels, the input processing logic is replicated such that there is an A level set of algorithm processing hardware, and a B level set. Each set contains one 12 bit parallel in/parallel out binary adder, twelve 4 bit serial in/serial out shift registers, and a fifth register called the transfer (XFR) register. During the portion of the cycle that the data from each channel is being averaged over four samples, the XFR register operates as a parallel in/parallel out 12 bit register. When all five sums have been developed, they will be found stored in storage registers 1 through 5, and readout is accomplished by successive 10 bit serial readouts from the transfer register followed by parallel 12 bit transfer into the XFR register. In the 10 bit serial readout the second LSB is dropped. Prior to the accumulation of a new set of sums, the content of all registers are cleared and the carry in (1/2 LSB) to the 12 bit parallel adder is activated to provide round off to the nearest LSB. Partial sum accumulation occurs in the A level hardware, while serial readout occurs in the B level hardware, such that GAC memory data read-in is fed alternately from A and B.

Data is loaded into the memory in complete 10 bit words, so that each of the five GAC memory banks holds 409 words in the form of serially loaded bits.

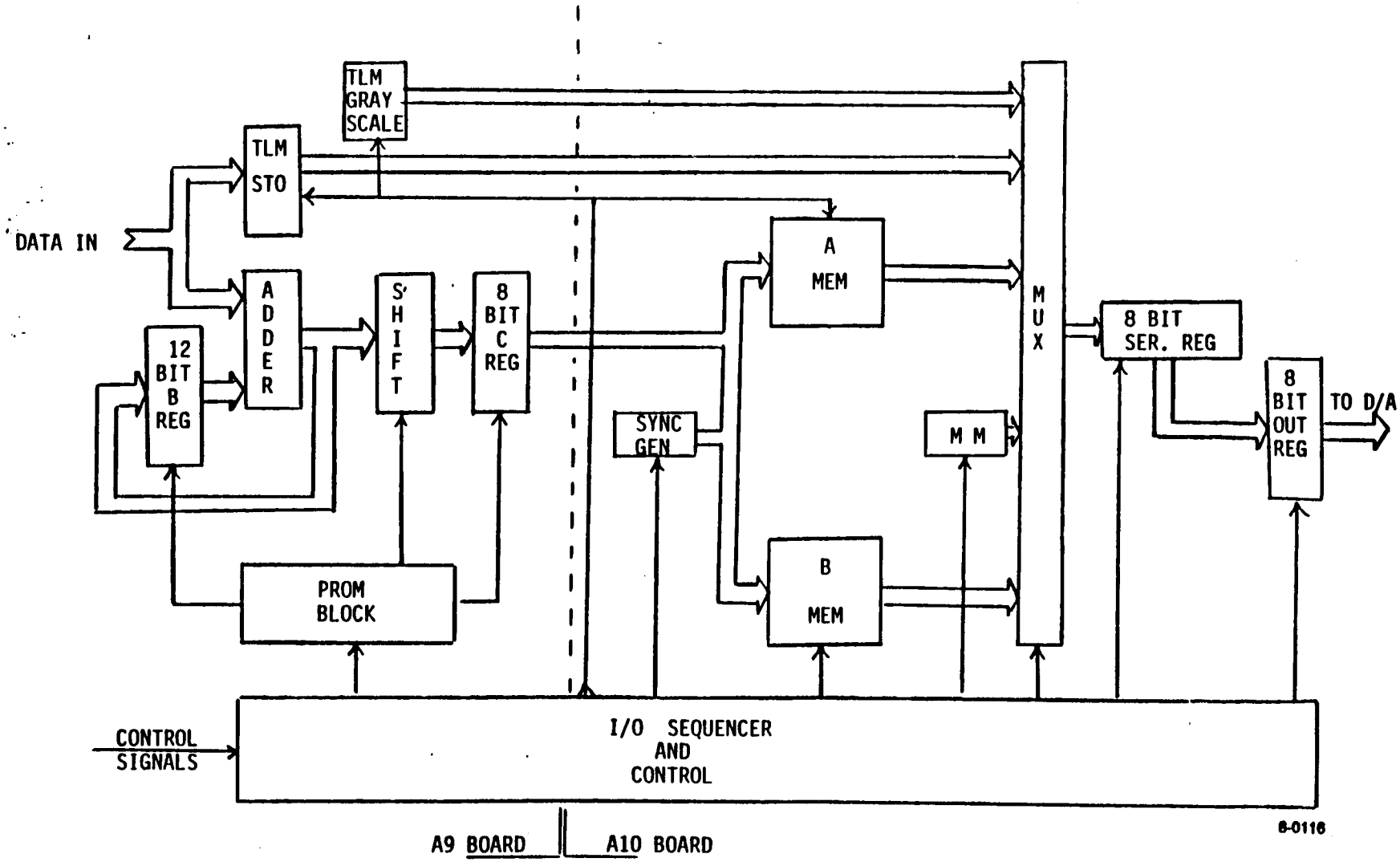
The remainder of the HRPT/LAC/GAC processing chains consists of auxiliary memories (1024 x 1 static COS/MOS RAMS), memory address generators, sequencers for control of directs external data inputs, and the final output data formatter and multiplex logic.

4.8.3.2.8 APT Data Processing

The APT Channel accepts 10 bit words consisting of Space Data, Earth Data, Back scan Data, and various Temperature Data. This data is processed and stored within the channel in digital format. The APT channel multiplexes the data with internally generated data including sync and gray scale wedges, digital data, once formatted, is passed to a D/A converter whose analog output is filtered and AM modulated onto the 2.4 kHz carrier. The modulator output is bandwidth limited and then routed to the transmitter. The AVHRR Channel 3A/3B telemetry point is monitored by the MIRP to know which gray scale wedge to use.

The block diagram for the digital portion of the channel is shown in Figure 4.8.3-9. It should be noted that the external data is received and processed in a 10 bit parallel format. However, upon completion of processing, the eight most significant bits of each word are stored serially in memory, and therefore the output is the result of eight bits or 256 levels, All of the 2048 APT digital data words are processed under PROM control, with one 4 bit PROM code being assigned to each word.

The AVHRR scan rate determines the input rate, and therefore one APT output line is produced for every three input scans. Since an APT line is defined as a Selected Channel A Segment, one of five, followed by a Selected Channel B Segment, one of five, two of every three input scans, with respect to Earth Data, are used in producing output video, the third scan of Earth Data being discarded. In implementing this, the required memory has been divided into two sections, A and B. The A Section is associated with SCAN 1 data and the B Section with SCAN 2 data.



MIRP APT CHANNEL, DIGITAL BLOCK DIAGRAM

Figure 4.8.3-9. MIRP APT Channel, Digital Block Diagram

APT anal processing consists of a standard eight bit D/A converter and filter preceding an AM modulator. The modulator is the only unique element in this chain. Its operation is based on the fact that the digitally derived 2.4 kHz Carrier contains no third harmonic and, therefore, the output of the modulator does not contain the carrier third harmonic and associated signal sidebands. This fact alleviated the problem associated with a squarewave chopper modulator of having to filter the third harmonic while maintaining the channel signal bandwidth. In this case, the first harmonic of consequence is the fifth, or 12 kHz. The output filter corner is at 6 kHz, well beyond the 4.8 kHz upper sideband. Operation of this modulation scheme requires timing which is not easily derived in a direct digital countdown from the available clock frequencies. Therefore, a COS/MOS phase-locked loop is used to derive the 28.8 kHz necessary for the modulator. Dual APT outputs are supplied directly to the two VHF transmitters.

4.8.3.2.9 Sync Delta and Rephase Operation

The MIRP performs the function of measuring the line-to-line sync jitter of the AVHRR. It does this by measuring the elapsed time difference between the AVHRR sync and the digitally derived internal sync of the MIRP, which is assumed to be stable. After this measurement is made, the resulting 10 bit sync delta word is output in the data frame. The normal range of delta measurement is approximately $\pm 30\mu$ seconds, but up to $\pm 511\mu$ seconds can be measured.

This measurement is also used to establish whether or not MIRP must rephase its outputs. The algorithm used for rephase is:

1) Rephase if the time difference between AVHRR sync and MIRP internal sync is greater than $\pm 256\mu$ sec for two successive measurements.

2) Rephase if the time difference between the syncs is greater than $\pm 512\mu$ sec for any one measurement.

Following power turn-on, the MIRP detects the first incoming AVHRR sync pulse and phases its outputs to it. The MIRP output phasing is now established and output data frames are generated continuously in this phase. In a parallel path, however, the MIRP continuously monitors the relative phasing between AVHRR sync and the MIRP internal sync generator. Using the algorithm previously described, the MIRP determines if a rephase operation is required.

When rephase is necessary, the execution of the actual rephase is delayed until the end of the HRPT/LAC major frame (end of a GAC frame). At this time, the MIRP begins examining the AVHRR sync line, and rephases the MIRP outputs to the first AVHRR sync pulse thereafter. Rephase immediately truncates the existing frames, and begins new frames at the new phase reference point. This new phasing is then maintained forever unless the sync measurement limits are again exceeded.

Indication that a rephase operation has occurred is supplied by bit 8 of the ID word in the header. This flag is repeated for twelve successive HRPT/LAC minor frames after rephase occurs.

4.8.3.2.10 P-N Code Generator Implementation

Within the MIRP design, three different configurations of polynominal code generators are used for various purposes.

Two sixth degree generators which operate according to the polynominal $X^6 + X^5 + X^2 + X + 1$ are used for generation of the primary sync codes for the digital formats. Two identical generators are needed since the sync must be developed simultaneously at two different rates for HRPT/LAC and for GAC.

Two additional tenth degree generators are used for development of the auxiliary sync code patterns at the end of digital formats. These operate according to the polynominal $X^{10} + X^5 + X^2 + X + 1$. It is also used for data randomization, and test mode operation.

Both the sixth degree and tenth degree generators consist of a serial shift register with exclusive-OR gates used to insert the output feedback. The sixth and tenth degree generators share the first six stages of a common shift register. This is possible since the sixth and tenth degree codes don't have to be developed simultaneously. Internal logic control determines whether the feedback comes from the sixth stage or the tenth stage, and thereby determines whether a sixth degree or tenth degree code is generated.

In addition, the MIRP also uses an eleventh degree polynominal generator and operates according to $X^{11} + X^8 + X^5 + X^2 + 1$. In this application, outputs from 10 of the 11 stages are brought out in parallel and used to substitute for AVHRR data. The entire shift register is clocked at a rate which allows all five channels of simulated AVHRR data to be identical.

4.8.3.2.11 Test Mode Implementation

The MIRP is capable of operation in either of two specialized test modes. Both of these modes are ground commandable, and are controlled by DPC words bit 8 and 15.

One of these test options is designated as the "Data Substitution" mode and it entails replacing the input AVHRR data with an eleventh degree P-N code data internally generated in the MIRP. When operating in this mode, all digital data formats are maintained, except that the data is derived from the code generator.

The other test option is designated simply as "Test" mode, and it entails replacing the output MIRP data with a tenth degree P-N code. When operating in this mode, all digital output frame formats are discontinued. In its place is substituted a continuously cycled P-N code. In actual implementation, there are two such paths within the MIRP due to the 10 to 1 difference between the HRPT/LAC and GAC output rates. The one shown in the block diagram operates at 665.4 KBS while the parallel path used for GAC operates at 66.54 KBS.

4.8.3.2.12 Summary of MIRP Characteristics

The summary of MIRP characteristics is as follows:

Parameter	Characteristics	
Size	8.8"H x 7.7"W x 9.4"D (Max)	
Weight	11.0 lb (Max)	
Power Consumption	11.0 watts (max)	
Logic Family	CD4000B Series Cos/Mos	
Memory Elements	Static 4K CMOS RAMS	
Memory Size	Approximately 150 kb	
Clock Sources	Two Required:	
	(a) 0.9984 MHz	
	(b) 1.3308 MHz	
Commands	(a) 3 Pulse Discrete Commands	
	(b) 16 Bit DBC Word	
Input Data Sources	(a) AVHRR Data	
	(b) TIP Data	
	(c) AMSU (AIP) Data	
AVHRR Inputs	10-Bit Parallel Words	
	@ 199.68k Words/sec	
	5 Channels commutated	
TIP Data	8-Bit Serial Words @ 66.54 kb/s	
AMSU (AIP) Data	8-Bit Serial Words @ 16.64 kb/s	
Outputs Formats	Four simultaneous outputs:	
	(a) HRPT	
	(b) LAC	
	(c) GAC	
	(d) APT	
Output Rates	(a) HRPT/LAC	665.4 kb/s
	(b) GAC	66.54 kb/s
	(c) APT	2 lines/sec
Output Frame Size	(a) HRPT/LAC	11,090 words
	(b) GAC	3,327 words
	(c) APT	128 lines
Output Frame Rates	(a) HRPT/LAC	6/sec
	(b) GAC	2/sec
	(c) APT	1 per 64 sec
Output Word Length	(a) HRPT/LAC/GAC	10 bits
	(b) APT	Analog
Output Encoding	(a) HRPT	NRZ-L (Un-Randomized)
	(b) LAC/GAC	NRZ-L (Randomized)
	(c) APT-AM 2.4 kHz subcarrier	
Frame Sync	(a) HRPT/LAC/GAC	60-bit PN code
	(b) APT 1	7 pulses @ 1040 Hz
	(c) APT 2	7 pulses @ 832 Hz
Auxiliary Sync	(a) HRPT/LAC/GAC	1000-bit PN code
	(b) APT	None

4.8.4 DIGITAL TAPE RECORDERS

4.8.4.1 Requirements

The five Digital Tape Recorders (DTRs) provide storage and playback of GAC, LAC, and TIP data. GAC and LAC data are intended for the two CDA stations. GAC is recorded continuously, including during playback. Capacity is provided to record GAC data during the worst-case sequence of orbits blind to the CDA stations. This requires recording for four orbits in a row. There is be at most one such sequence per day. Most days include instead a sequence requiring recording three orbits in a row. LAC is recorded for up to 10 minutes per orbit. TIP data is recorded on those orbits which are blind to the CDA stations but which allow contact with Lannion, France. Each day includes at least one such orbit. Most include two in a row. In those cases TIP data will be recorded continuously from the previous CDA contact until the second European playback, including during the first playback.

Two playback rates are provided for the CDA stations and a third lower rate for the European station.

One DTR will record TIP Boost Mode data during the boost phase. Any four of the five recorders can perform the mission,

4.8.4.2 Description

The DTRs are government-furnished equipment. . They are purchased by NASA-GSFC from GE Information Processing and Recording Systems in Camden, New Jersey.

The DTRs are identical and interchangeable. Each is a variation of the NASA standard 10^8 bit tape recorder. The principal variation is the use of two Transport Units (TUs) fastened to a single Electronics Unit (EU) to form a single DTR. This provides adequate tape capacity in a compact package while retaining the TU and EU designs from the Standard Recorder. The TUs are hermetically sealed; the EU is not.

Each TU contains 550 total feet of 1/4 inch by 1 mil tape, on coaxial reels with Negator tension spring and a direct-drive brushless d-c capstan motor. The record is in split-phase format at 9560 bits/in/track in all modes. Input data to the DTR is in NRZ-L format in all record modes. Playback output is in split-phase format in the two lower rate modes and NRZ-L format in the highest rate mode. GAC and LAC data are recorded on 8 parallel tracks. TIP data is recorded to 4 parallel tracks. Both the record and playback clocks are provided by the XSU, and the DTR maintains a specified phase relationship between the playback data and the XSU clock. The DTR erases old data in all record modes. All recording is in the "forward" direction. All playback is in the "reverse" direction except for a diagnostic "forward playback" mode which allows playing back a record more than once, and is also used as a "fast forward" mode.

The DTR electrical interfaces are shown in Figure 4.8.4-1. The data and clock interfaces are National DM 7830/7820A differential line driver/line receivers. The harness for these signals is shielded twisted pair. The other electrical interfaces are standard.

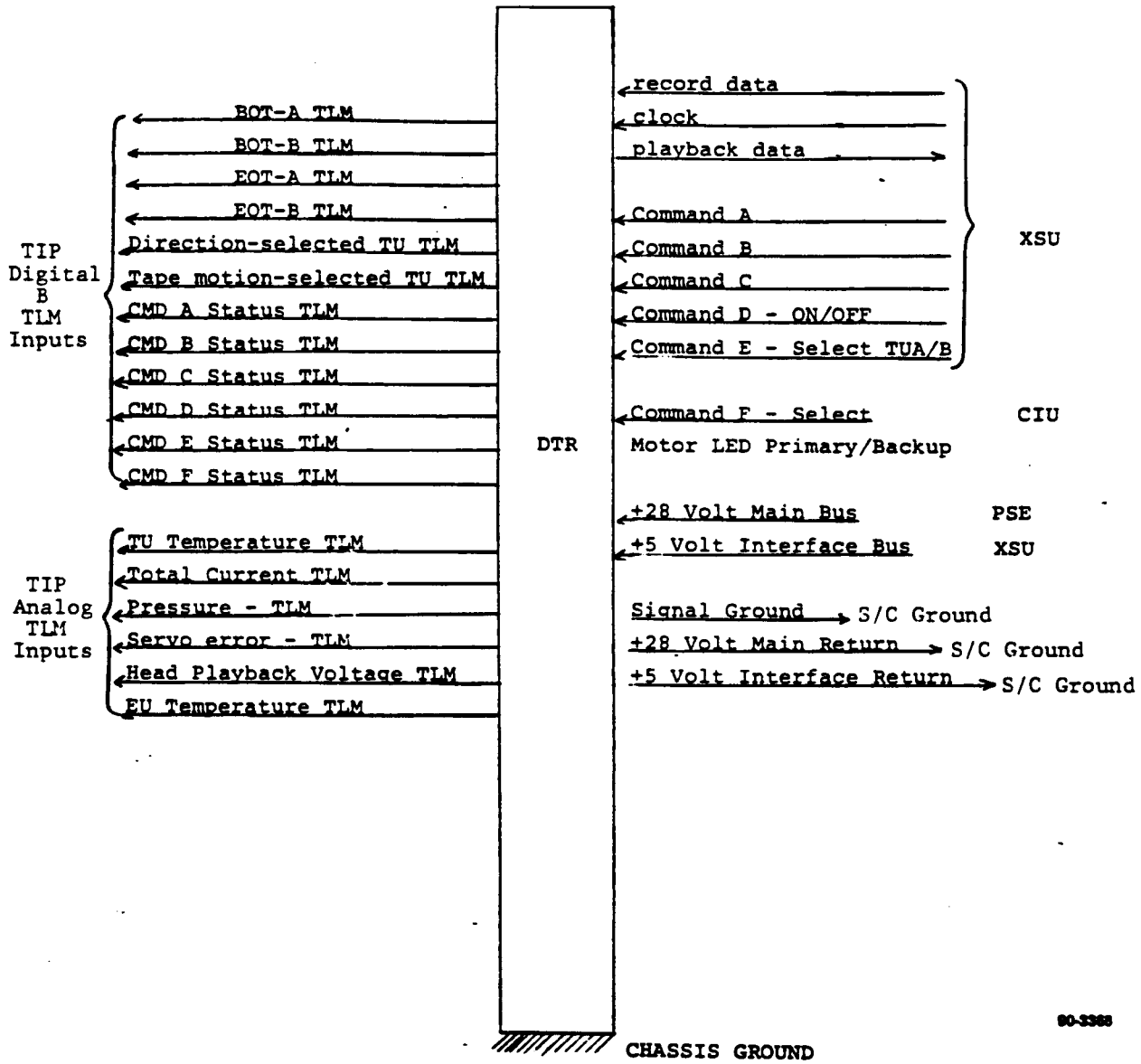


Figure 4.8.4-1. DTR Electrical Interfaces

The DTRs are mounted on ESM Panel 4. Each requires a conductive and radiative environment between 0°C and 35°C. The maximum angular momentum for each is 0.003 in-lb-sec in the X direction. The DTR is delivered to Astro assembled, including the interconnecting harness.

The DTR modes, commands and power requirements are summarized in Table 4.8.4-1. The DTR has redundant BOT and EOT sensing mechanisms. The primaries are comparisons of capstan and reel revolutions. The secondaries are LED/photo-transistors and optical windows in the tape. Either of the sensors will switch the

TABLE 4.8.4-1. DTR MODES, COMMANDS AND POWER

Record/Playback Mode Number	Name	Bit Rate	Format	Tape Speed in/sec	Command Status A B C D E	Total D-C Power Watts	Notes
(1)	Forward Playback	2.6616MB/S	NRZ-L	34.78	0 0 0 1 X	16	Diagnostic mode-permits moving tape forward without erasure for repeated playback
(2)	Record 8.32 KB/S	8.32KB/S	NRZ-L	0.217	0 0 1 1 X	7	TIP Orbit Mode
(3)	Record 16.64 KB/S	16.64KB/S	NRZ-L	0.435	0 1 0 1 X	7	TIP Boost Mode or AIP Orbit Mode
(4)	Record 66.54 KB/S	66.54KB/S	NRZ-L	0.87	0 1 1 1 X	7	GAC
(5)	Record 665.4 KB/S	665.4KB/S	NRZ-L	8.70	1 0 0 1 X	8	LAC
(6)	Playback 332.7 KB/S	332.7KB/S	Split-Ø-L	8.70	1 0 1 1 X	14	TIP or AIP
(7)	Playback 1.3308 MB/S	1.3308MB/S	Split-Ø-L	17.39	1 1 0 1 X	15	GAC or LAC
(8)	Playback 2.6616 MB/S	2.6616MB/S	NRZ-L	34.78	1 1 1 1 X	16	GAC or LAC
(9)	OFF	-	-	0	X X X 0 X	.2	
TUA	Select TU-A Submode	Determined by primary mode			X X X X 0		DC power determined by primary mode
TUB	Select TU-B Submode	Determined by primary mode			X X X X 1		DC power determined by primary mode
SF	Standby Fwd Submode	-	-	0	not entered by cmd.	2	Entered when DTR senses the tape extreme. Removes power from all but the mode command decoder.
SR	Standby Reverse Submode	-	-	0	not entered by cmd.	2	Same as above

DTR into standby. The primaries have the first chance to stop the tape and secondaries have the last. The DTR bit error rate is 5 in 10^7 at beginning of life and 1 in 10^6 at end of life. It is designed for 25,000 passes on each TU.

4.8.4.3 Summary of DTR Characteristics

The summary of DTR characteristics is as follows:

Parameter	Characteristics
Configuration	two TUs with 1 EU.
Tape	1/4 inch x 1 mil x 550 ft. total per TU
Number of tracks	4 for TIP/AIP data 8 for MIRP data
Packing density	9560 B/in per track
Tape storage	Coaxial reel to reel
Tape tensioning	Negator
Tape drive	direct-drive brushless dc motor
Life	25000 passes per TU
Error rate	5×10^7 (BOL), 1×10^6 (EOL)
Modes	see Table 4.8.4-1
Power	See Table 4.8.4-1
Bit rates and formats	See Table 4.8.4-1
Size	See Figure 4.8.4-1
Weight	21.9 lbs. including EU-TU harness

The required record/playback combinations are as shown:

Required Mode Combinations

Orbit Environment		Boost Environment	
Record Mode	Playback Mode	Record Mode	Playback Mode
2	6	3	None*
3	6		
4	7		
5	7		
4	8		
5	8		

*To be played on Mode 6 in orbit environment.

The minimum usable record length on each TU is as shown:

Minimum Usable Records

Record Mode	Record Length on Each TU (Minimum) Minutes	Bits	Playback Mode
2	225	1.125×10^8	6
3	113	1.125×10^8	6
4	113	4.50×10^8	7
4	113	4.50×10^8	8
5	11.3	4.50×10^8	7
5	11.3	4.50×10^8	8

4.8.5 CROSS STRAP UNIT (XSU)

4.8.5.1 Cross Strap Unit (XSU) Requirements

The XSU provides the interconnecting means between the various data sources, tape recorders, and S-Band transmitters. It also provides clock signals for several other units.

On command from the CIU either TIP, AIP, GAC or LAC data may be selected for recording by one or more of the five digital tape recorders. Commands for the tape recorders from the CIU are also distributed by the cross strap unit. Any tape recorder output or HRPT data may be routed to one or more S-Band transmitter. TIP/AIP real-time data may be routed to any S-Band transmitter, but only STX-2 and STX-4 can be connected to the omni antenna.

The clock signals for the TIP, MIRP, HIRS, SBUV, SEM, AMSU, and AIP are synthesized in the XSU from the 1.024 MHz reference provided by the CIU. Since these clocks may not be derived by integer division, phase locked loops must be used for synthesis. The frequencies are MIRP: 998.4 kHz and 1.3308 MHz, TIP: 998.4 kHz, instruments and AIP: 1.248 MHz. In addition, the XSU must supply the tape recorder playback clocks at 2.6616 MHz or 1.3308 MHz or 332.7 kHz. The short term stability requirement is four percent of one period of 2.6616 MHz (i.e., 15 ns jitter) for times from one to one thousand periods. These clocks are all fully redundant.

4.8.5.2 General Description

The cross strap unit consists of nine boards: A1 and A2 are synthesizers; A3 and A4 contain the recorder and transmitter selection logic; A5 is a spare board; A6 and A7 contain the command and telemetry circuits; and A8 and A9 are the redundant power converter boards. Figure 4.8.5-1 is a basic block diagram of the unit. The Digital Tape Recorders (DTR) and the S-Band transmitters (STX) are shown for clarity.

4.8.5.2.1 XSU Synthesizer Description

The 1.024 MHz reference is divided by 8 to 128 kHz and applied to phase detector $\phi 1$. A VCO operating at 4.992 MHz is divided by 39 and applied to the other input of $\phi 1$. The resulting error signal is filtered by F(s) 1 and used

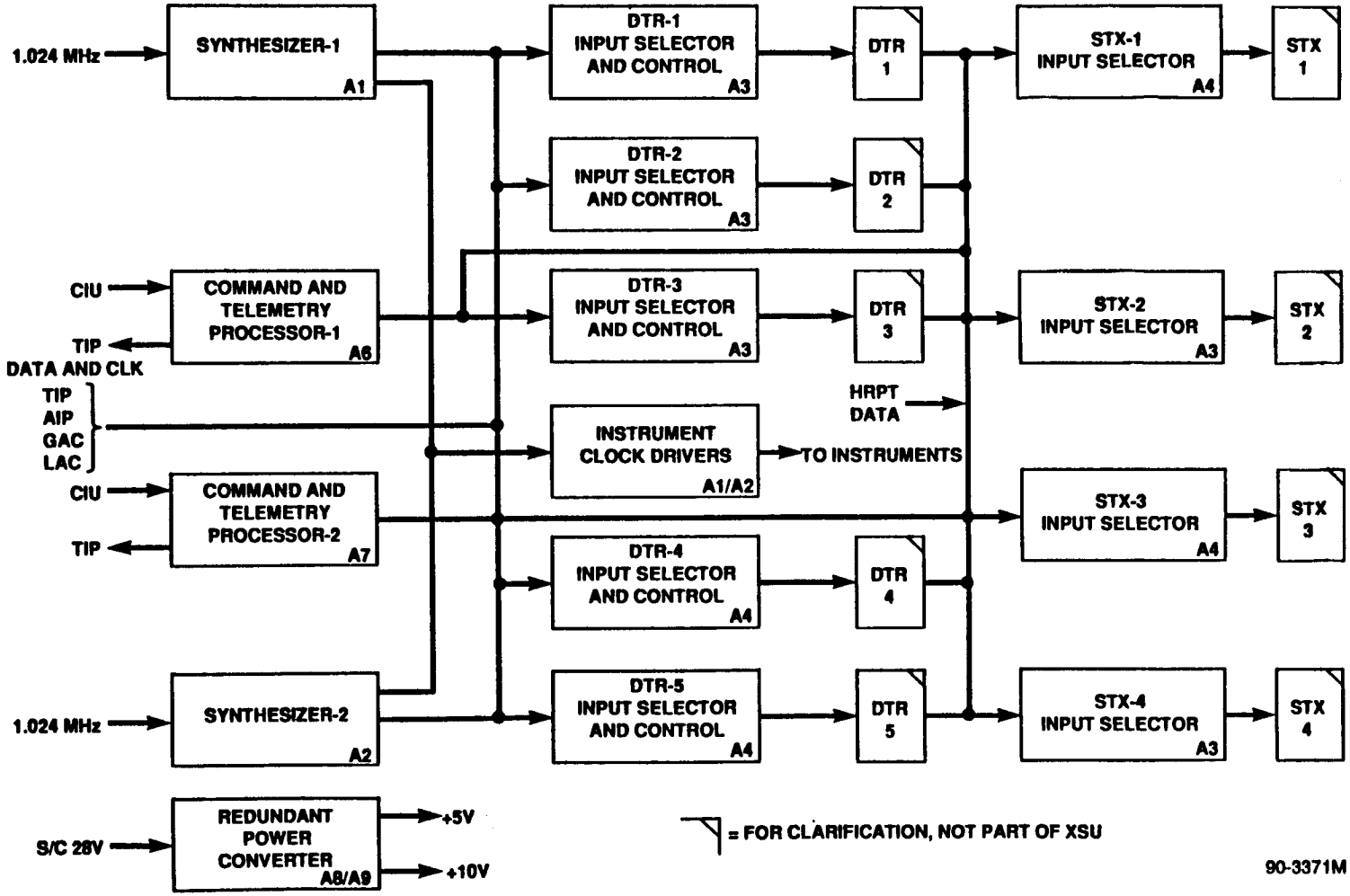


Figure 4.8.5-1. XSU Block Diagram

to phase lock the VCO. The 4.992 MHz output of the first phase locked loop is then divided by 1040 to 4.8 kHz and applied to phase detector $\phi 2$. The 4.992 MHz is also mixed with the 5.323 MHz from VCO_2. The lower side band of this mixing process yields 331.2 kHz which is separated by a low pass filter, LPF, and divided by 69 to 4.8 kHz. This is applied to the other input of $\phi 2$. The error signal is filtered by F(s) 2 and used to phase lock VCO2.

The A1 and A2 boards are identical. The synthesizers and dividers are redundant. Cross strapping is provided for each clock output.

The 4.992 MHz is divided by five to make the 998.4 kHz clocks for MIRP and TIP and by 4 to make 1.248 MHz for the instruments. The last divide by 2 to 1.248 MHz is done after cross strapping to provide as little asymmetry as possible. The 5.323 MHz is divided by 4 to make 1.3308 MHz for the MIRP. The lower loop operates at 5.3232 MHz in order to provide a good square wave at 2.6616 MHz. The division to 2.6616 MHz is done at both 10v and 5v.

Each board (A1 and A2) actually contains three sets of tape recorder TTL clocks signals. In addition, there is a single 624 kHz, 10v output to A6/A7.

4.8.5.2.1.1 Clock Cross Strapping. The COS/MOS clock cross strapping is done with 4001 NOR gates. The cross strap is done at 2.496 MHz so that a divide by two may be inserted prior to the 4041 interface. These three IC's are on the interface power with decoupling resistors to limit the drain to 100 ma. The 2.496 MHz signal is generated on the 10v XSU switched power. When the 10v is switched OFF, the bus is pulled to ground through a pair of 150 ohm resistors in parallel. This assures that the unused input of the 4001 does not float.

The DTR clock lines between the synthesizer board and the recorder logic board are TTL. Since an LPSTTL output looks like a logic "1" when unpowered, a NAND gate is used for cross strapping. Additionally a 10K resistor assures that the unused input will not float near the threshold level. Power is supplied to the cross strap ICs by an OR'd 5v.

4.8.5.2.1.2 5.3232 MHz Loop Dynamics. The loop filter is designed to provide a composite response having -12 dB/octave slope at low frequencies and changing just prior to the 0 dB cross over to -6 dB/octave. After crossing over, the response is changed back to -12 dB/octave to provide a minimum of 40 dB attenuation at the sampling frequency, Ws. The minimum phase margin occurs at minimum gain and as shown is 48 degrees. The resulting response is closed loop. The maximum over shoot is approximately 2.8 dB. The closed loop bandwidth varies from 1.1 Kr/s to 2.0 Kr/s. (175 Hz to 318 Hz)

4.8.5.2.1.3 4.992 MHz Loop Dynamics. The loop filter is designed to provide a -12dB/octave composite at low frequencies, changing to -6dB/octave just prior to the 0 dB cross over. Since the sampling frequency is at 804 Kr/s in this loop there is adequate attenuation without intentionally adding a pole after the zero dB cross over. There is, however, a pole due to the VCO input circuit that occurs at 80 Kr/s. The minimum phase margin is 46 degrees. The response is closed loop. Maximum over-shoot is about 3.8 dB and minimum closed loop bandwidth is 1.20 Kr/s (191 Hz).

The lower side band of the mixing process is separated out by the low pass filter. The resulting sine wave must be squared up to present a normal logic swing to the divide by 69. The mixer implementation is by an exclusive OR circuit arrangement. The regular CMOS, CD4030, exclusive OR gate is not fast enough for these frequencies. The low pass filter is an 0.5 dB Tchebyshev having three elements. The limiter portion of a CD4046 PLL is used to square up the filter output.

4.8.5.2.2 Recorder and STX Logic Description

The Recorder Logic boards, A3 and A4, each contain three DTR selectors and two STX selectors consists of several multiplexer chips which control the routing of data and clock signals, plus the control logic necessary to decode incoming commands and drive the multiplexer address lines.

Commands are input to the A3/A4 board on the seven bit parallel Command Bus (CB). Each selector, or unit, is connected to one line of the eight bit parallel Unit Select Bus (USB). The particular unit for which a command is intended is pulsed on its unique USB line, at which time the command is stored in the selector's internal registers.

There are two Command Buses and two Unit Select Buses, one of each associated with each redundant side of the XSU. Only the active one is gated into the selector.

Each selector is associated with one external device. There are five DTRs and four STXs, leaving one spare DTR selector (located on the A3 board) and no spare STX selectors. The 2284738 boards are all identical and interchangeable. A3 or A4 functions are determined solely by harness-board wiring. Refer to Figures 4.8.5-2 and 4.8.5-3.

Power for the selectors is obtained by OR-ing the XSU redundant internal supplies. 10 volts is diode-OR'd for each selector individually, but 5 volts is OR'd within the DC/DC converters giving a single +5.2 volt bus. Each selector is resistor current limited in the 10 volt line to 50 ma for short circuit fault protection. 5 volt protection is provided by a transistor current sensing switch, set to latch off at greater than about 220 ma.

4.8.5.2.3 Command/Telemetry Description

The Command/Telemetry boards, A6/A7, are comprised of three major sections:

1) MIRP, TIP, and DTR data receivers and format converters
2) Command registers and logic
3) Telemetry registers and logic

Those elements of the board which are redundant and associated with side 1 (i.e., the A8 power supply) are on the A6 board, while A7 is associated with side 2. The 2284743 boards are identical and interchangeable; which functions they perform depend solely on which slot, A6 or A7, they are plugged into.

4.8.5.2.3.1 <u>Digital A Telemetry</u>. XSU digital telemetry consists of a status readout of commands previously sent to the XSU. Telemetry is transferred to TIP by a digital A serial interface conforming to the requirement of the

BITS 1-4 SELECT XSU FUNCTION					BITS 5-16 DEFINE MODE OF SELECTED XSU FUNCTION													
XSU MODE CMD BITS 1	2	3	4	SELECTED XSU FUNCTION	5	6	7	8	9	10	11	12	13	14	15	16	MODE OF SELECTED XSU FUNCTION	
0	0	0	0	RECORD/PLAYBACK-DTR #1	1	1	0	0	0	1	X	X	X	X	X	X	1	FORWARD PLAYBACK
0	0	1	0	RECORD/PLAYBACK-DTR #2	0	0	0	0	1	1	X	X	X	X	X	X	2	RECORD TIP ORBIT
0	1	0	0	RECORD/PLAYBACK-DTR #3	0	1	0	0	1	1	X	X	X	X	X	X	3	RECORD AIP ORBIT
0	1	1	0	RECORD/PLAYBACK-DTR #4	0	0	0	1	0	1	X	X	X	X	X	X	4	RECORD TIP BOOST
1	0	0	0	RECORD/PLAYBACK-DTR #5	0	1	0	1	0	1	X	X	X	X	X	X	5	RECORD AIP BOOST
					1	0	0	1	1	1	X	X	X	X	X	X	6	RECORD GAC
					1	1	1	0	0	1	X	X	X	X	X	X	7	RECORD LAC
					0	0	1	0	1	1	X	X	X	X	X	X	8	PLAYBACK 332.7 KB/S
					0	1	1	1	0	1	X	X	X	X	X	X	9	PLAYBACK 1.3308 MB/S
					1	0	1	1	1	1	X	X	X	X	X	X	10	PLAYBACK 2.6616 MB/S
					X	X	X	X	X	0	X	X	X	X	X	X	11	DTR OFF
					X	X	X	X	X	X	0	X	X	X	X	X	SA	SELECT TU-A SUBMODE
					X	X	X	X	X	X	1	X	X	X	X	X	SB	SELECT TU-B SUBMODE

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Figure 4.8.5-2. Mode Command Logic

BITS 1-4 SELECT XSU FUNCTION					BITS 5-16 DEFINE MODE OF SELECTED XSU FUNCTION													
XSU MODE CMD BITS 1	2	3	4	SELECTED XSU FUNCTION	5	6	7	8	9	10	11	12	13	14	15	16	MODE OF SELECTED XSU FUNCTION	
1	0	1	0	TRANSMITTER INPUT-STX #1	0	0	0	X	X	X	X	X	X	X	X	X	1	STX INTERFACE OFF
1	1	0	0	TRANSMITTER INPUT-STX #2	0	0	1	X	X	X	X	X	X	X	X	X	2	XMIT PLAYBACK FROM DTR #1
1	1	1	0	TRANSMITTER INPUT-STX #3	0	1	0	X	X	X	X	X	X	X	X	X	3	XMIT PLAYBACK FROM DTR #2
0	0	0	1	TRANSMITTER INPUT-STX #4	0	1	1	X	X	X	X	X	X	X	X	X	4	XMIT PLAYBACK FROM DTR #3
					1	0	0	X	X	X	X	X	X	X	X	X	5	XMIT PLAYBACK FROM DTR #4
					1	0	1	X	X	X	X	X	X	X	X	X	6	XMIT PLAYBACK FROM DTR #5
					1	1	0	X	X	X	X	X	X	X	X	X	7	XMIT SPLIT-PHASE-L
					1	1	1	X	X	X	X	X	X	X	X	X	8	XMIT HRPT

NOTE X = DON'T CARE STATE

90-3373M

Figure 4.8.5-2. Mode Command Logic (Continued)

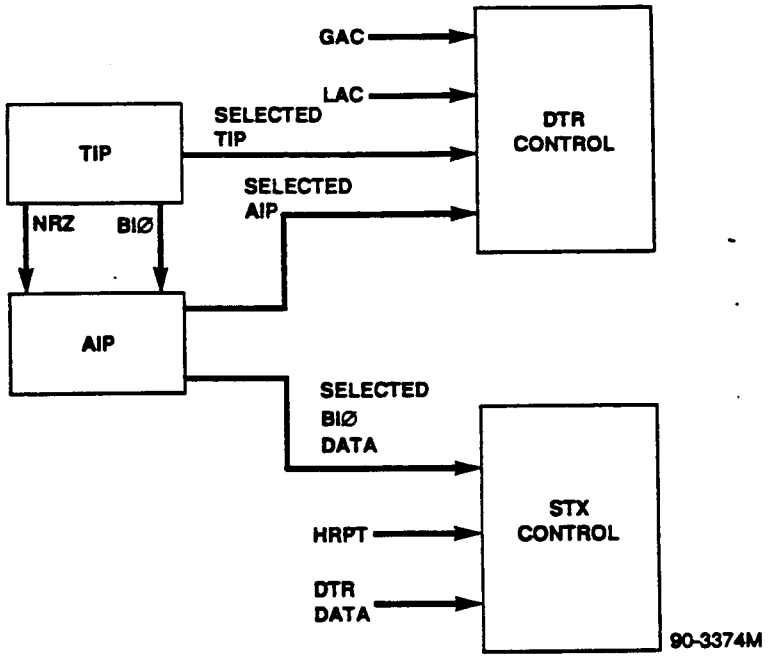

Figure 4.8.5-3. DHS Data Paths

General Instrument Interface Specification (IS-2280259). Commands to the XSU are stored in the command storage registers of the DTR/STX selectors in the A3/A4 board. Refer to Figure 4.8.5-4.

4.8.5.2.4 DC-DC Converter Description

Each power supply unit contains a DC-DC converter and two voltage regulators, which serve as the interface between the spacecraft power source and the load electronics. The DC-DC converter is a high-efficiency two transformer square wave oscillator with the low power (output) transformer operating in the saturating mode and the high power (output) transformer operating in the linear mode. The input to the converter contains an RFI filter and LC filter to reduce the chopped currents that are fed back on to the spacecraft regulated bus. The oscillator is transformer-coupled to each of the two voltage regulators. The input square waves are rectified, filtered and series regulated. The series regulators use negative feedback to control the output voltage and impedance. The XSU supplies the +5 volt interface power for the DTRs, CIU, and SSE.

DIGITAL-A WORD NUMBER	XSU FUNCTION	WORD CONTENT
1	RECORD/PLAYBACK - DTR #1	BITS [1 2 3 4 5 6 7] RECORD/PLAYBACK MODE. ENCODED THE SAME AS BITS 5-11 OF THE XSU MODE COMMAND. BIT [8] SPARE.
2	RECORD/PLAYBACK - DTR #2	
3	RECORD/PLAYBACK - DTR #3	
4	RECORD/PLAYBACK - DTR #4	
5	RECORD/PLAYBACK - DTR #5	
6	TRANSMITTER INPUT - STX #1	BITS [1 2 3] TRANSMITTER INPUT MODE. ENCODED THE SAME AS BITS 5-7 OF THE XSU MODE COMMAND. BITS [4 5 6 7 8] SPARE.
7	TRANSMITTER INPUT - STX #2	
8	TRANSMITTER INPUT - STX #3	BITS [1 2 3] TRANSMITTER INPUT MODE. ENCODED THE SAME AS BITS 5-7 OF THE XSU MODE COMMAND. BIT [4] 0 = XSU SIDE 1 ON, 2 OFF 1 = XSU SIDE 2 ON, 1 OFF
	TRANSMITTER INPUT - STX #4	BITS [5 6 7] TRANSMITTER INPUT MODE. ENCODED THE SAME AS BITS 5-7 OF THE XSU MODE COMMAND. BIT [8] SPARE.

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Figure 4.8.5-4. XSU Mode Status Telemetry

4.8.5.3 Summary of Characteristics

The XSU characteristics are summarized as follows:

Record data switching to any of 5 DTRs in NRZ-L format.

DATA	SOURCE	BIT RATE, KB/S
TIP	TIP NRZ-L	8.32 (orbit), 16.64 (boost)
AIP	AIP NRZ-L	16.64
GAC	MIRP	66.54
LAC	MIRP	665.4

Playback and real-time data switching to any of STXs with jitter <0.05 bit period and asymmetry <2 percent.

DATA	SOURCE	BIT RATE KB/S	FORMAT FROM SOURCE	FORMAT TO STX
TIP Playback	Any DTR	332.7	Split-ϕ-L	Split-ϕ-L
GAC Playback	Any DTR	1330.8	Split-ϕ-L	Split-ϕ-L
LAC Playback	Any DTR	1330.8	Split-ϕ-L	Split-ϕ-L
GAC Playback	Any DTR	2661.6	NRZ-L	NRZ-L
LAC Playback	Any DTR	2661.6	NRZ-L	NRZ-L
HRPT	MIRP	665.4	NRZ-L	Split-ϕ-L
TIP/AIP*	TIP/AIP Split-Phase Interface	8.32 (orbit)	Split-ϕ-L	Split-ϕ-L
		16.64 (boost)	Split-ϕ-L	Split-ϕ-L

Mode command storage and transfer to 5 DTRs - 9 primary, 4 submodes.

Full-time clock outputs

DESTINATION	FREQUENCY	LEVEL, VOLTS	MAXIMUM ASYMMETRY
HIRS/3	1.248 MHz	10	5%
AMSU-A1	1.248 MHz	10	10%
SEM	1.248 MHz	10	5%
AMSU-A2	1.248 MHz	10	10%
SBUV/2	1.248 MHz	10	5%
AMSU-B	1.248 MHz	10	5%
AIP	1.248 MHz	10	10%
AIP	1.248 MHz	10	5%
MIRP	0.9984 MHz	10	5%
(2) TIP	0.9984 MHz	10	5%
Spare	0.9984 MHz	10	5%
MIRP	1.3308 MHz	10	5%
Spare	1.3308 MHz	10	5%

*Normally connected to STX #2 only.

Serial mode commands from CIU.

Subcommutated mode status telemetry to TIP.

Loss from single-point failure restricted to a single data input or output, or a single DTR.

Size - 7.62"W, 7.8"L, 8.8"H

Weight - 8.9 lbs

Power - mode dependent - 13.7 watts (max)

4.8.6 AMSU INFORMATION PROCESSOR (AIP)

4.8.6.1 AMSU Information Processor (AIP) Requirements

The AIP is a medium-rate data processor which accepts data from the three AMSU instruments at a combined data rate of 7.20 kbps and from the TIP at 8.32 kbps. The AIP creates three data streams from its inputs: 1) an 8.32 kbps data stream consisting of only AMSU data which is sent to the Manipulated Information Rate Processor (MIRP) for inclusion in data sent to the MIRP High Resolution Output, Limited Area Coverage High Resolution Stored Output (LAC), and Global Stored Medium Resolution Output (GAC); 2) a 16.64 kbps NRZ-L data stream made up of both AMSU data and TIP data which is sent to the XSU for routing to the DTRs; and 3) a 16.64 kbps bi-phase data stream of combined AMSU/TIP data is sent to the XSU for direct transmission. Also, the AIP, upon command, routes TIP data at either 8.32 kbps or 16.64 kbps to the XSU in bi-phase format or both bi-phase and NRZ-L formats.

The AIP is a redundant unit within a common assembly. One of the redundant sides is always powered. The AIP is designed such that a single point failure will not prevent getting AMSU data to both the MIRP and the XSU.

4.8.6.2 General Description

4.8.6.2.1 Inputs

The interfaces between the AIP and the other spacecraft units are illustrated in Figure 4.8.6-1. Inputs to the AIP can be categorized as clocks/sync, data, commands, and power, as shown in Table 4.8.6-1.

The following clock and sync signals are input to the AIP:

a. 1.248 MHz Clock - The AIP is provided with a 1.248 MHz clock per AIP side from the XSU from which all internal timing is derived. The clock is a nominal square wave having a frequency of 1.248 MHz, and stability as defined by IS-3267415. The symmetry is 50 $\pm$10%.

b. TIP major frame - The AIP is provided with a major frame pulse from the TIP. The pulse is 240 μsec and occurs at a rate of 32 sec in orbit mode and 16 sec during boost mode. The AIP synchronizes this signal with the 1.248 MHz clock.

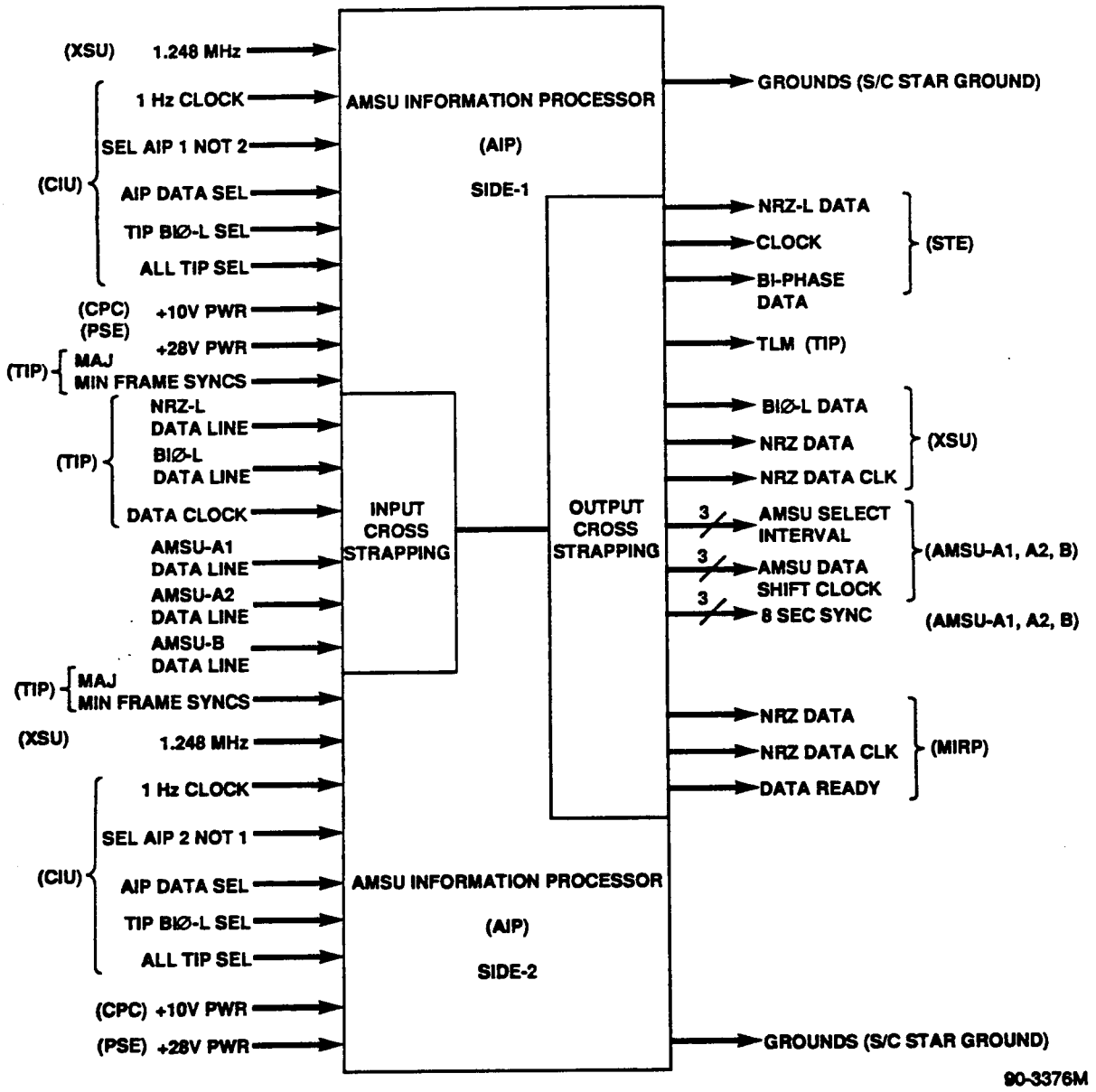


Figure 4.8.6-1. AIP Interface Diagram

TABLE 4.8.6-1. AIP INPUT SIGNALS

SOURCE	NAME	INTERFACE TYPE
CIU	Pulse Discrete Cmds	
	Select AIP 1 Not 2	Slow
	Select AIP 2 Not 1	Slow
	Select AIP Data Stream	Slow
	Select TIP Bi-phase Data Stream	Slow
	Select ALL TIP Data Stream	Slow
AMSU-A1	AMSU A1 Digital Data	Fast
AMSU-A2	AMSU A2 Digital Data	Fast
AMSU-B	AMSU B Digital Data	Fast
TIP	NRZ Data Clock	Fast
	NRZ Data Line	Fast
	Major Frame Sync	Fast
	Bi-phase Data	Fast
	Minor Frame Sync	Fast
XSU	1.248 MHz Clock	High Speed
PSE	28 Volt Power	N/A
CPC	10 Volt Interface Power	N/A

* The "Fast", "Slow", and "High" speed Interface Types are defined in RCA 2629668.

c. TIP minor frame sync - The AIP is provided with a minor frame pulse from the TIP. The pulse is 240 μsec and occurs at the output of Bit 0, word 0 of each TIP minor frame. This signal occurs at a rate of .1 sec during orbit mode and 0.05 sec during boost mode. The AIP synchronizes this signal to the 1.248 MHz clock.

d. CIU 1 Hz sync - The AIP is provided with a 1 Hz sync from the CIU. This signal is used in conjunction with the TIP major frame sync to generate the AMSU 8-second sync outputs from the AIP.

The CIU provides the AIP with pulse discrete command lines for the purpose of selecting which side of the redundant AIP is to be placed into operation and which AIP mode is to be used. The command lines are specified as follows:

a) Select AIP 1 not 2
b) Select AIP 2 not 1
c) Select AIP data mode
d) Select TIP bi-phase data mode
e) Select ALL TIP data mode

The ALL TIP mode of the AIP is designed to be used with the TIP boost mode, in which TIP data is output at 16.64 Kbps. TIP data frames are then received by the AIP twice as fast. The AIP should be commanded into the ALL TIP mode before the TIP is put into boost mode, and commanded out of ALL TIP mode after the TIP leaves boost mode. This will insure that no conflict occurs in

reading TIP data from the memories in the AIP. Also, after leaving ALL TIP mode, that first AIP frame will correctly contain the previous frame of TIP data. This is also the last frame of data output during ALL TIP mode. No damage to, or lockup of, the AIP will occur if this sequence is not followed. Word 103 of AIP minor frame may be corrupted if the TIP is in boost Mode and the AIP is not in ALL TIP mode. The use of the AIP data mode or TIP bi-phase data mode do not require any AIP/TIP command sequencing.

TIP data is received on non-redundant interfaces from the selected TIP side. Both NRZ and bi-phase data are input to the AIP. Processing using these inputs is described in Section 4.8.6.2.3.

The AIP provides commutation and formatting capability for the three AMSU instruments: AMSU-A1, AMSU-A2, and AMSU-B. Each AMSU interface consists of a data line which is presented to the AIP by the AMSU; and a continuous 16.64 kHz clock line, a select interval line, and a sync signal which are presented by the AIP to the AMSU to permit data transfer.

Digital information is accepted during the select interval. When not selected, the AMSU data source will be in either an active or inactive state. The user's first (most significant) bit of information will be established; i.e., reaching 90 percent of its value, at the first negative-going transition of the first clock pulse after the AMSU Select Interval goes active. The second through sixteenth most significant bits will be established by the negative-going transition of the remaining fifteen shift pulses. These bits will remain at their levels until the next negative-going transition of the next shift pulse. Data is clocked into the AIP on the positive-going transition of the clock pulse. The select signal generated by the AIP is pulsed at the end of the sixteenth bit time if more data words are to be read from the selected AMSU. This signal will go to its inactive level after all words are read.

The AMSU Data multiplexer is designed such that a single first level multiplexer failure will not contaminate more than one AMSU Data input channel. Each AMSU instrument is cross-strapped to both AIP sides.

4.8.6.2.2 Outputs

The outputs from the AIP are shown in Figure 4.8.6-1. Outputs from the AIP can be categorized as test points, telemetry, data to the XSU, data to the MIRP and AMSU handshaking signals as shown in Table 4.8.6-2. Generation and usage of the data signals are described in Section 4.8.6.2.3. The AIP provides the following telemetry points:

a) Analog - DC/DC Converter Status Side 1
DC/DC Converter Status Side 2

b) Discrete - AIP 1 SELECTED NOT 2
AIP 2 SELECTED NOT 1
AIP DATA MODE SELECTED
TIP BI-PHASE DATA MODE SELECTED
ALL TIP DATA MODE SELECTED

TABLE 4.8.6-2. AIP OUTPUT SIGNALS

Receiving Unit	Name	Interface Type
MIRP	Data Line	Fast
	Data Enable	Fast
	Data Clock	Fast
AMSU-A1	8 Sec Sync	Fast
	A1 Data Select	Fast
	Data Clock	Fast
AMSU-A2	8 Sec Synch	Fast
	A2 Data Select	Fast
	Data Clock	Fast
AMSU-B	8 Sec Sync	Fast
	B Data Select	Fast
	Data Clock	Fast
XSU	Data Line (NRZ-L)	Fast
	Data Clock	Fast
	Bi-phase Data	Fast
TIP	Telemetry	N/A
STE	NRZ-L Data	N/A
	Data Clock	N/A
	Bi-phase Data	N/A
	AIP Minor Frame Sync	N/A

* The "Fast" Interface Type is defined in RCA 2629668.

4.8.6.2.3 Processing

An overall block diagram of the AIP is shown in Figure 4.8.6-2. The AIP is designed to:

a. Receive data from AMSU-A1, -A2, and -B at a combined data rate of 7.20 kbps.

b. Receive NRZ-L data from the TIROS Information Processor (TIP) at a data rate of 8.32 kbps or 16.64 kbps.

c. Receive bi-phase data from the TIP at a data rate of 8.32 kbps or 16.64 kbps.

d. Output TIP data or combined AMSU/TIP data, in NRZ-L and bi-phase format, commandable by ground command, to the Cross Strap Unit (XSU).

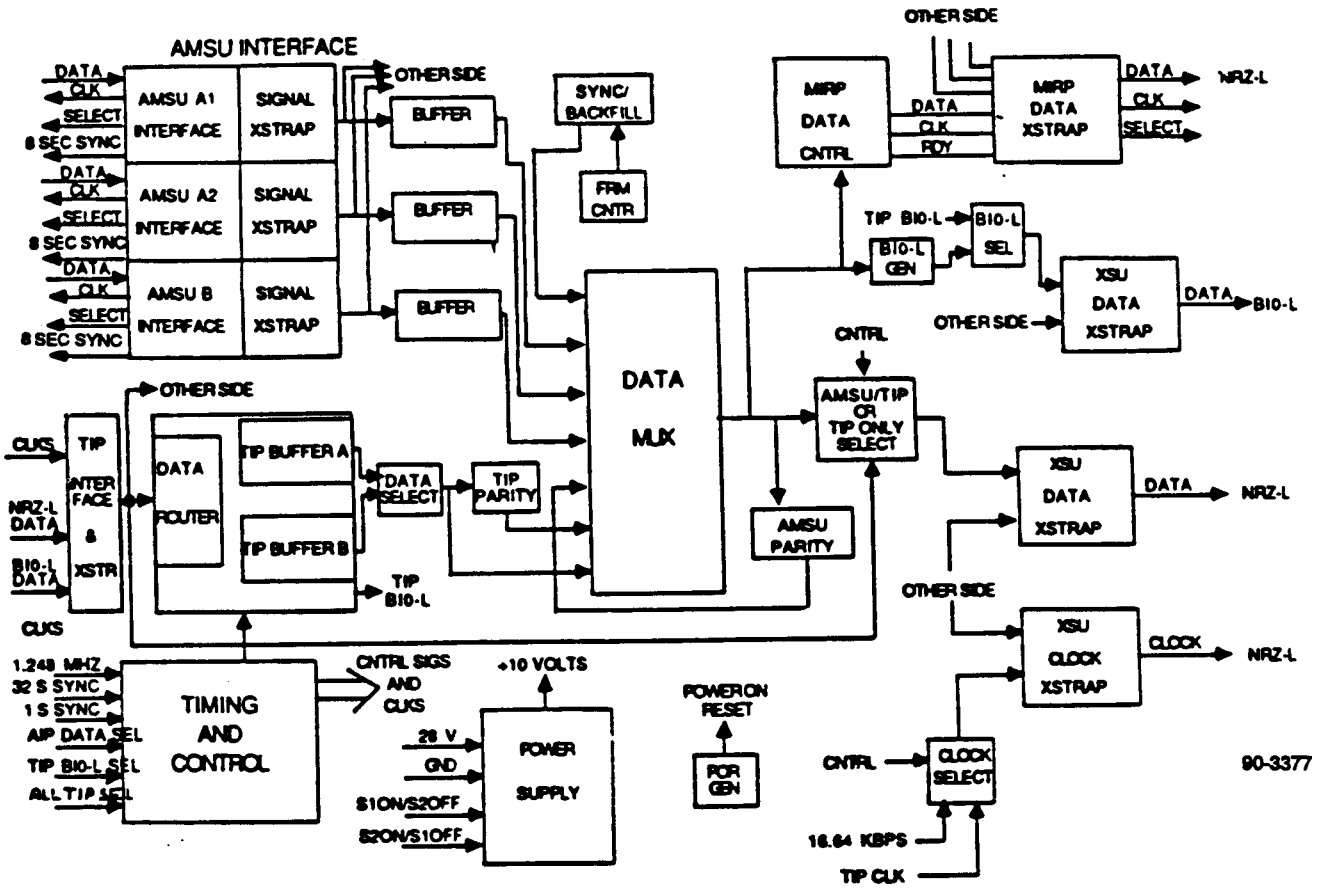


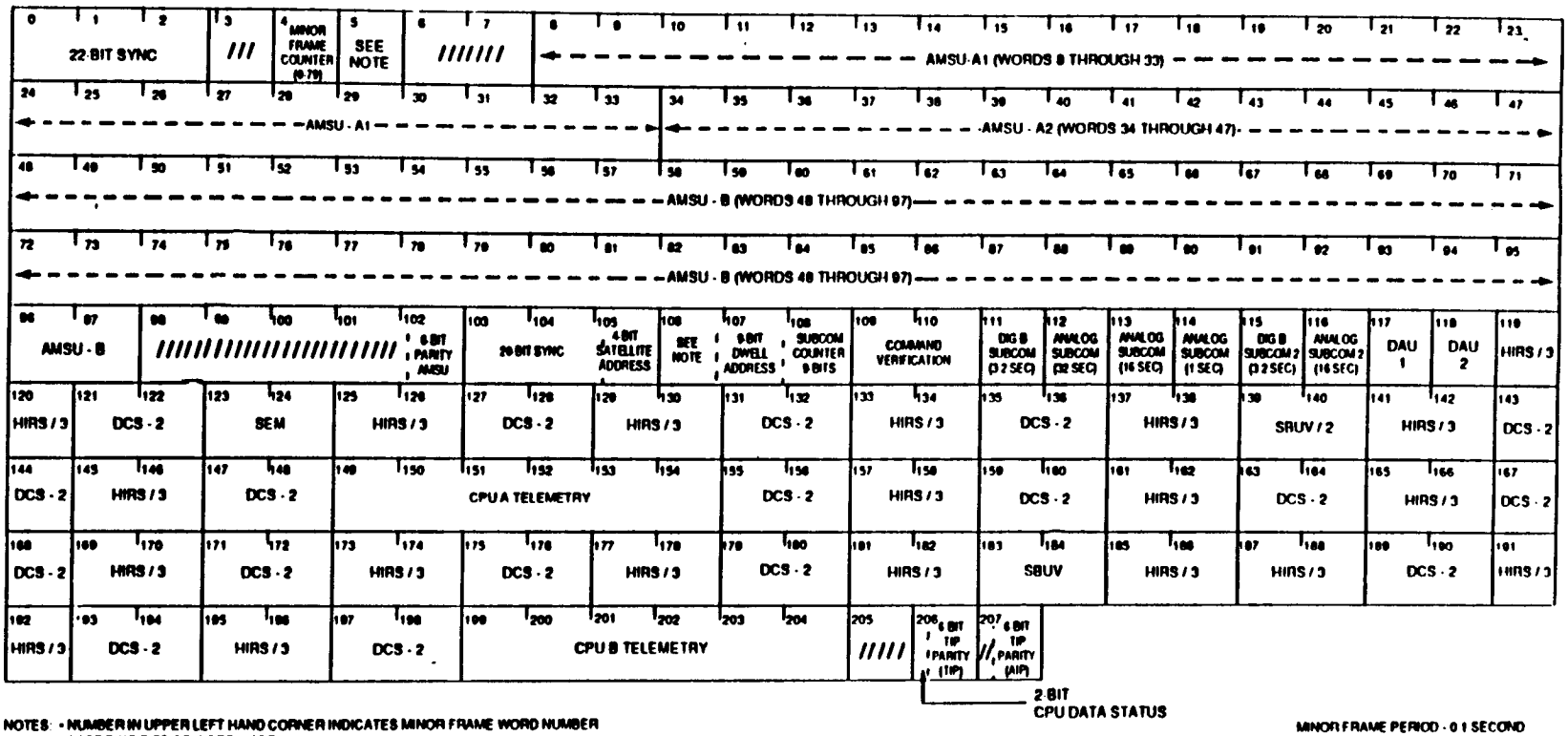
Figure 4.8.6-2. AIP Block Diagram

e. Output to the MIRP at 8.32 kbps, AMSU data conforming to the frame format of Figure 4.8.6-3, words 0 through 103 in NRZ-L bit stream format.

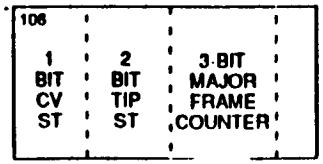
f. Provide AMSU-A1, -A2, and -B with synchronization, select interval, and data clock signals.

The AIP, upon command, generates a data stream consisting of AMSU data and TIP Orbit mode data as shown in Figure 4.8.6-3. The AIP output data rate for this data product is 16.64 kbps. This data is available to the XSU in both NRZ-L and bi-phase formats separately.

The AIP continuously generates a data stream consisting exclusively of AMSU data. This data stream's format is identical to words 0 through 103 of Figure 4.8.6-3. The AIP output data rate for this data product is an average of 8.32 kbps. It is sent at a 16.64 KBS rate, but only the first half of the AIP frame is utilized by the MIRP. This data is available to the MIRP in NRZ-L format.



NOTES:
- NUMBER IN UPPER LEFT HAND CORNER INDICATES MINOR FRAME WORD NUMBER
- LAST TWO BITS OF WORD 2 ARE 00
- /// WORD LOCATIONS ARE SPARE AND CONTAIN CODE 01010101
- FIRST SIX BITS OF WORD 5 ARE 000000 LAST TWO BITS ARE 8-SECOND FRAME COUNTER
- WORDS 103 THROUGH 206 ARE IDENTICAL TO A TIP ORBITAL MODE MINOR FRAME'S WORDS 0 THROUGH 103



MINOR FRAME PERIOD - 0.1 SECOND
OUTPUT DATA RATE - 16.64 KBPS

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Figure 4.8.6-3. AIP Output Format

The AIP is input TIP data, in both NRZ-L and bi-phase format, from the TIP at a rate of 8.32 kbps (for TIP orbit, dwell and CPU dump modes) or 16.64 kbps (for TIP boost mode). Upon command, the AIP outputs TIP bi-phase data and AMSU/TIP NRZ-L data, or TIP data in both bi-phase and NRZ formats, to the XSU without any processing.

These modes are summarized as:

1) AIP data mode
2) TIP bi-phase data mode
3) ALL TIP data mode

These modes are selectable by command. Table 4.8.6-3 shows the AIP modes and the corresponding data outputs.

TABLE 4.8.6-3. AIP MODES

Mode	Command	Data Outputs		
		Bi-Phase Data to XSU	NRZ Data to XSU	NRZ Data to MIRP
AIP Data	Select AIP Data Stream	AMSU/TIP Data Combined	AMSU/TIP Data Combined	AMSU Data Only
TIP Bi-phase Data	Select TIP Bi-phase Data Stream	TIP Data Only	AMSU/TIP Data Combined	AMSU Data Only
All TIP Data (Used for Boost Mode)	Select ALL TIP Data Streams	TIP Data Only	TIP Data Only	AMSU Data Only

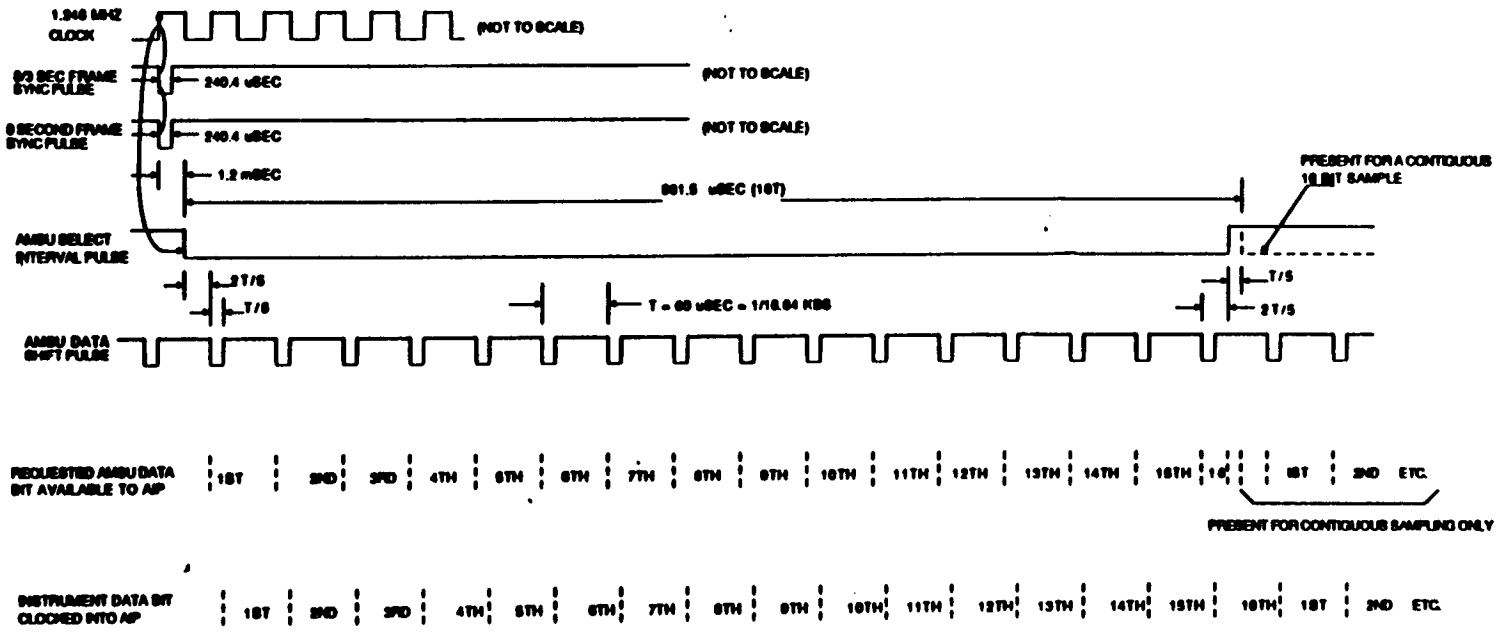
The AIP is organized into three discrete functions. The A1 board contains the series-pass regulators (utilizing LM 723 elements) for both AIP sides. The A2/A5 boards contain the processing electronics, and the A3/A4 boards contain the timing circuitry. A harness board interconnects the other five boards.

The timing of the data interface with the AMSU instruments is shown in Figure 4.8.6-4. AMSU data is input in the sequence shown in Figure 4.8.6-5. Outputs to the MIRP and XSU are controlled as shown in Figures 4.8.6-6 and 4.8.6-7, respectively. The overall input/output timing is shown in Figure 4.8.6-8. Sync signal timing is shown in Figure 4.8.6-9.

The functions of the processor boards are:

- TIP input data switched memory
- TIP memory switching and read/write control
- AMSU-A1, -A2, -B data switched memory
- AMSU-A1, -A2, -B memory switching and read/write control
- Sync word generator; backfill generator
- AMSU and TIP data parity generators
- Data output MUX
- Major and minor frame counters
- Minor frame word output control
- Power on reset generator

AIP AMSU DATA INTERFACE (16.64 KBS)



NOTES:

(1) LOGIC 1 (ACTIVE LEVEL) = GROUND
(2) INSTRUMENT DATA OUTPUT INTERFACE TO BE ACTIVE ONLY DURING SELECT INTERVAL PERIOD
(3) TI/TOB-H STANDARD FAST INTERFACE WILL BE USED FOR TRANSFER OF ALL DATA AND CONTROL SIGNALS.
(4) GROUND REFERENCED TO INTERFACE GROUND.
(5) AMSU SELECT AND SHIFT PULSES ARE CLOCKED BY LOW TO HIGH TRANSITION OF 1.248 MHz CLOCK
(6) AMSU SELECT INTERVAL DELAY FROM THE 0 SEC SYNC PULSE IS 1.23MSEC±30USEC FOR AMSU A1 13.7MSEC±30USEC FOR AMSU A2, AND 20.43MSEC±30USEC FOR AMSU B.

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Figure 4.8.6-4. AIP/AMSU Digital Interface

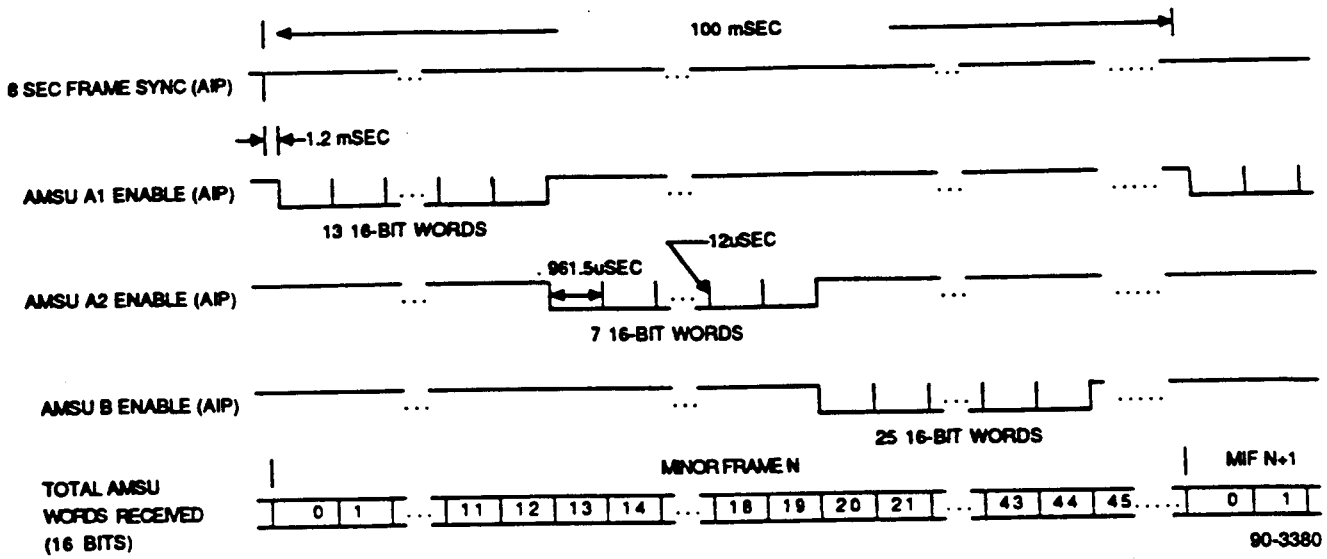

Figure 4.8.6-5. AIP/AMSU Data Input Sequence

Figure 4.8.6-10 is a block diagram of the processor boards. Figures 4.8.6-11 and 4.8.6-12 show the ASMU data buffer operation and memory switching, while Figures 4.8.6-13 and 4.8.6-14 show the same for the TIP data interface.

A block diagram of the timing boards is shown in Figure 4.8.6-15. The timing board functions are:

- AMSU-A1, -A2, -B data interface and cross-strap
- TIP data interface
- Timing generator
- MIRP data control
- MIRP data output cross-strap
- XSU data and clock selection (NRZ)
- XSU data output cross-strap (NRZ)
- AIP or TIP data only selection
- AIP bi-phase generator
- XSU bi-phase data selection and cross-strap

The AIP frame contains several special words. They are described in the following paragraphs:

The AIP generates a 22-bit sync code at the beginning of each frame as shown in Figure 4.8.6-3. The AIP outputs the following sequence with the most significant bit first:

Minor Frame Word 0	Minor Frame Word 1	Minor Frame Word 2
11110011	01101010	000000
MSB		LSB

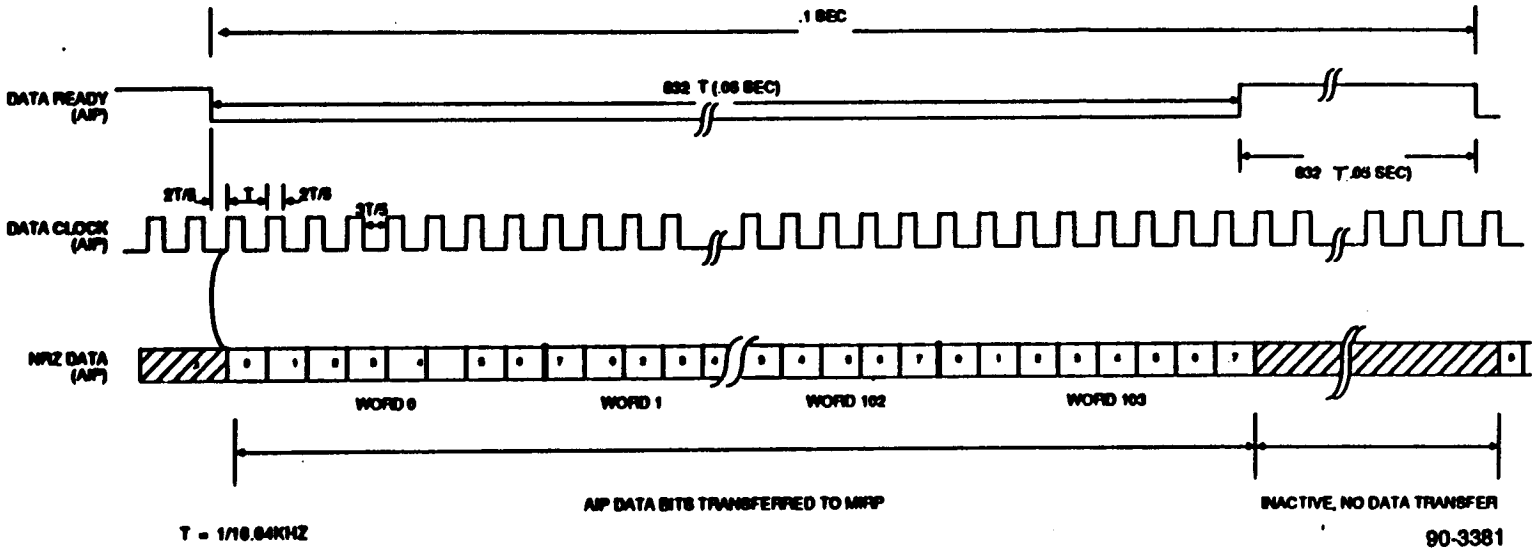

Figure 4.8.6-6. MIRP Data Transfer Timing

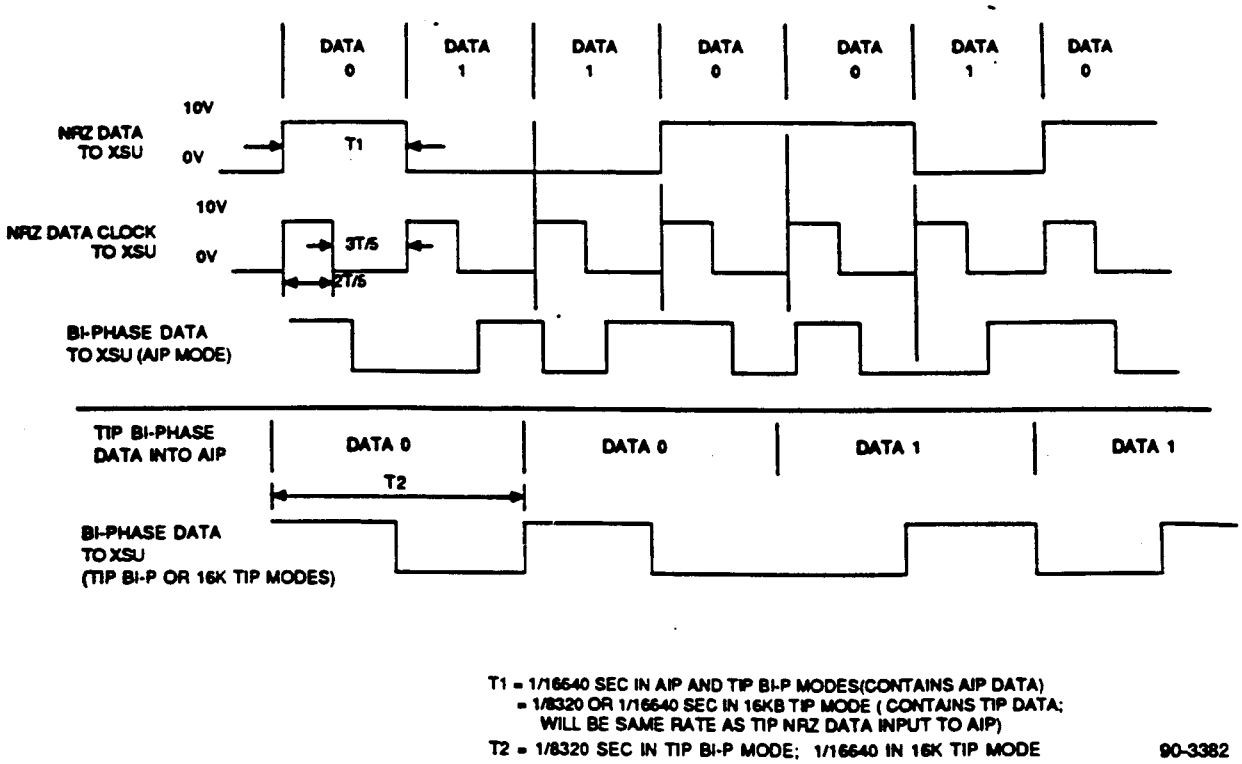

Figure 4.8.6-7. Cross-Strap Unit Data Transfer Waveforms

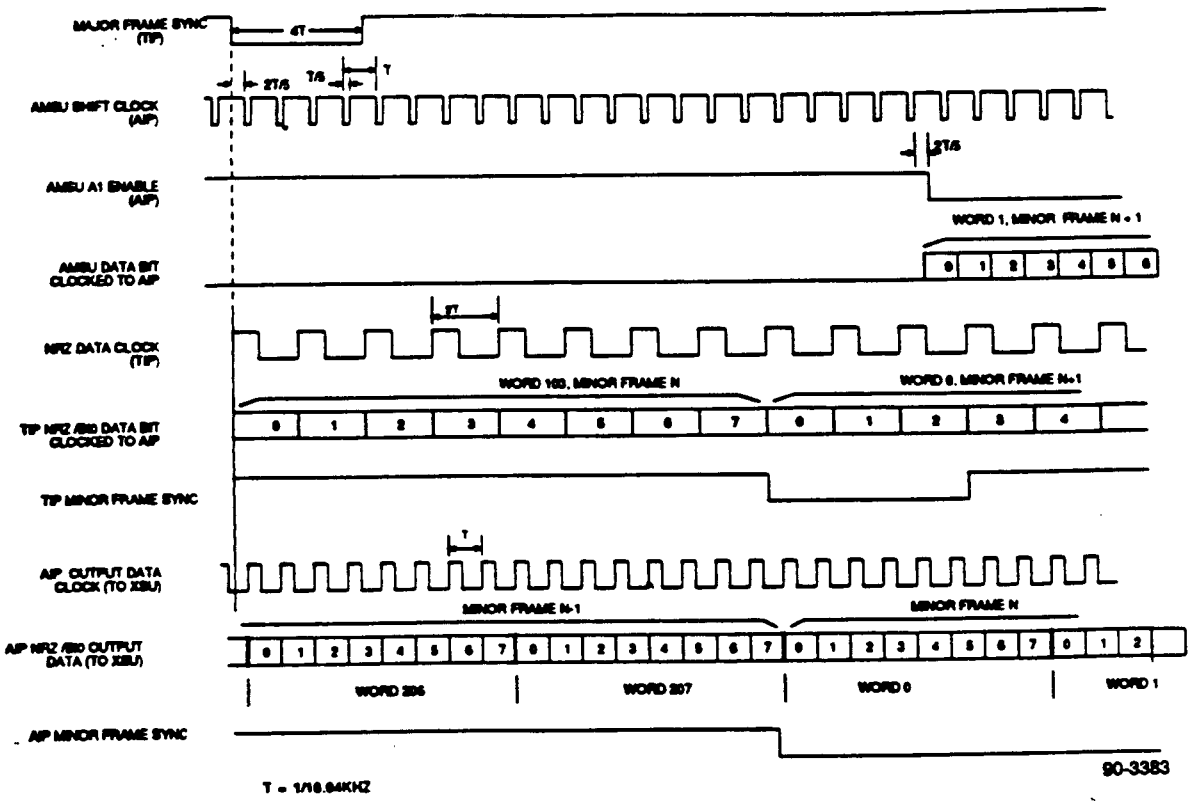

Figure 4.8.6-8. AIP Input/Output Timing

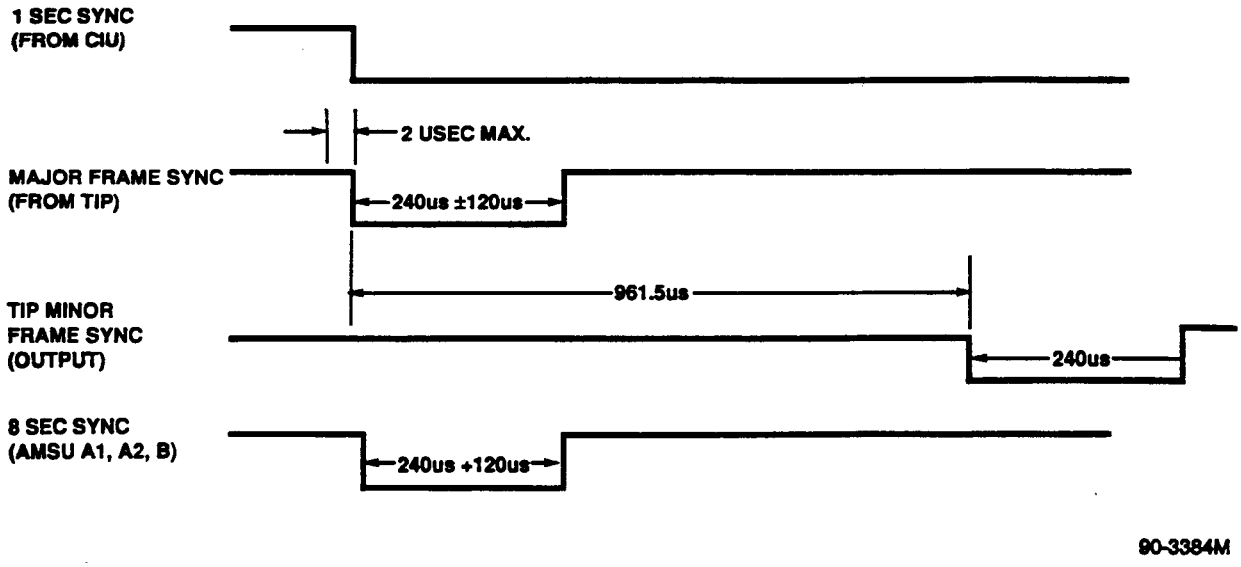

Figure 4.8.6-9. AIP Generated Sync Signals

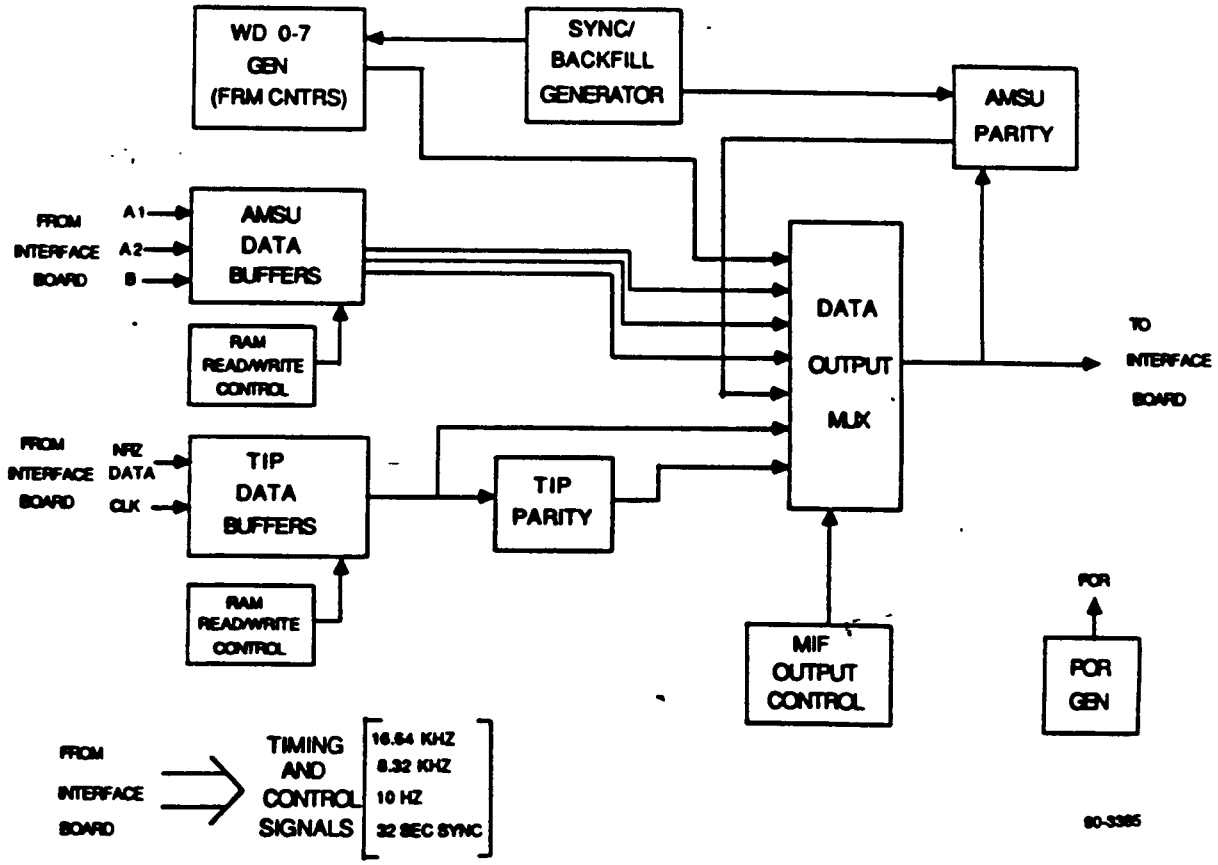

Figure 4.8.6-10. A2/A5 Processor Board Block Diagram

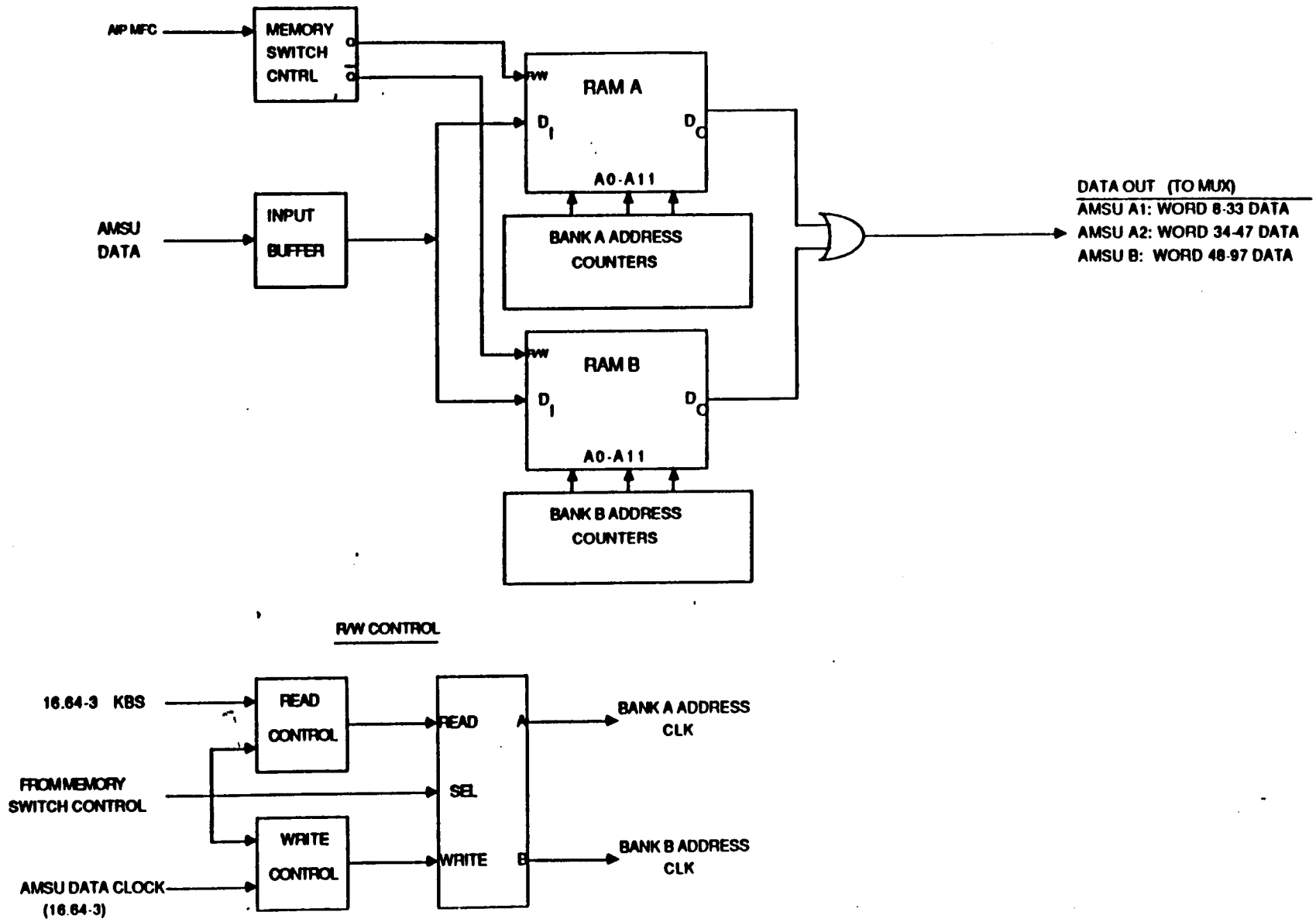

Figure 4.8.6-11. AMSU Data Buffer Block Diagram

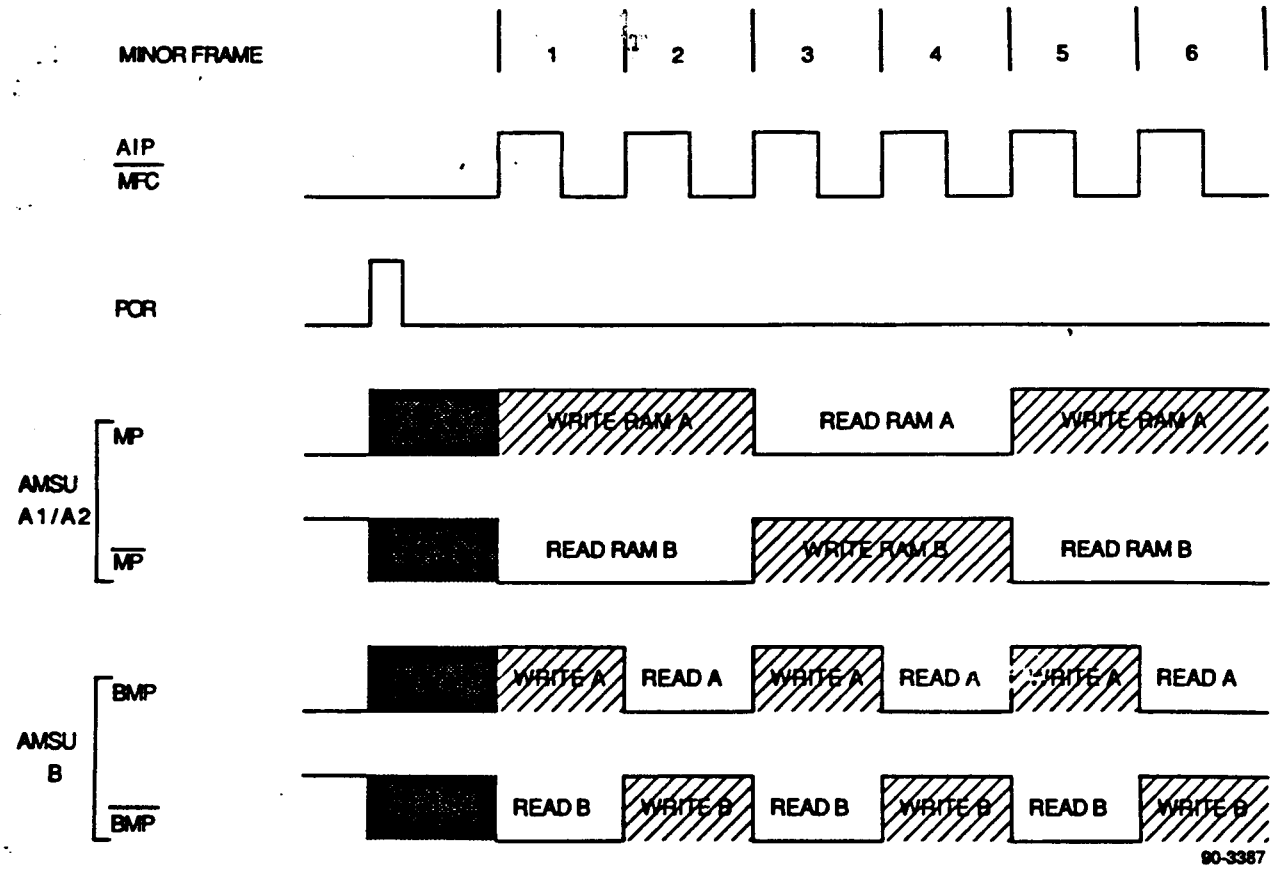

Figure 4.8.6-12. AMSU Memory R/W Switching

The AIP generates a count of minor frames which occurs once every 0.1 seconds. The counter contains an 8-bit binary representation of the minor frame count and is inserted into the minor frame format as shown in Figure 4.8.6-3. Code 00000000 represents Minor Frame 0 and Code 01001111 represents Minor Frame 79. When inserted in the minor frame format, the MSB is first. The minor frame counter is updated at the beginning of each minor frame and resets at the end of Minor Frame 79.

The AIP generates a count of major frames which occurs every 80 minor frames. Bit 7 and 8 of minor frame word 5 will count 8-second intervals, the count overflowing to 0 synchronous with the TIP 32-second major frame pulse.

Bits 3 through 8 of Minor Frame Word 102, as shown in Figure 4.8.6-3, are used for an even parity check on AMSU Data. The bits have the following interpretation:

Bit	Interpretation
3	Even parity check on data contained in Minor Frame Words 2 through 18.
4	Even parity check on data contained in Minor Frame Words 19 through 35.
5	Even parity check on data contained in Minor Frame Words 36 through 52.
6	Even parity check on data contained in Minor Frame Words 53 through 69.
7	Even parity check on data contained in Minor Frame Words 70 through 86.
8	Even parity check on data contained in Minor Frame Words 87 through 101 including Bits 1 through 7 of Minor Frame Word 102.

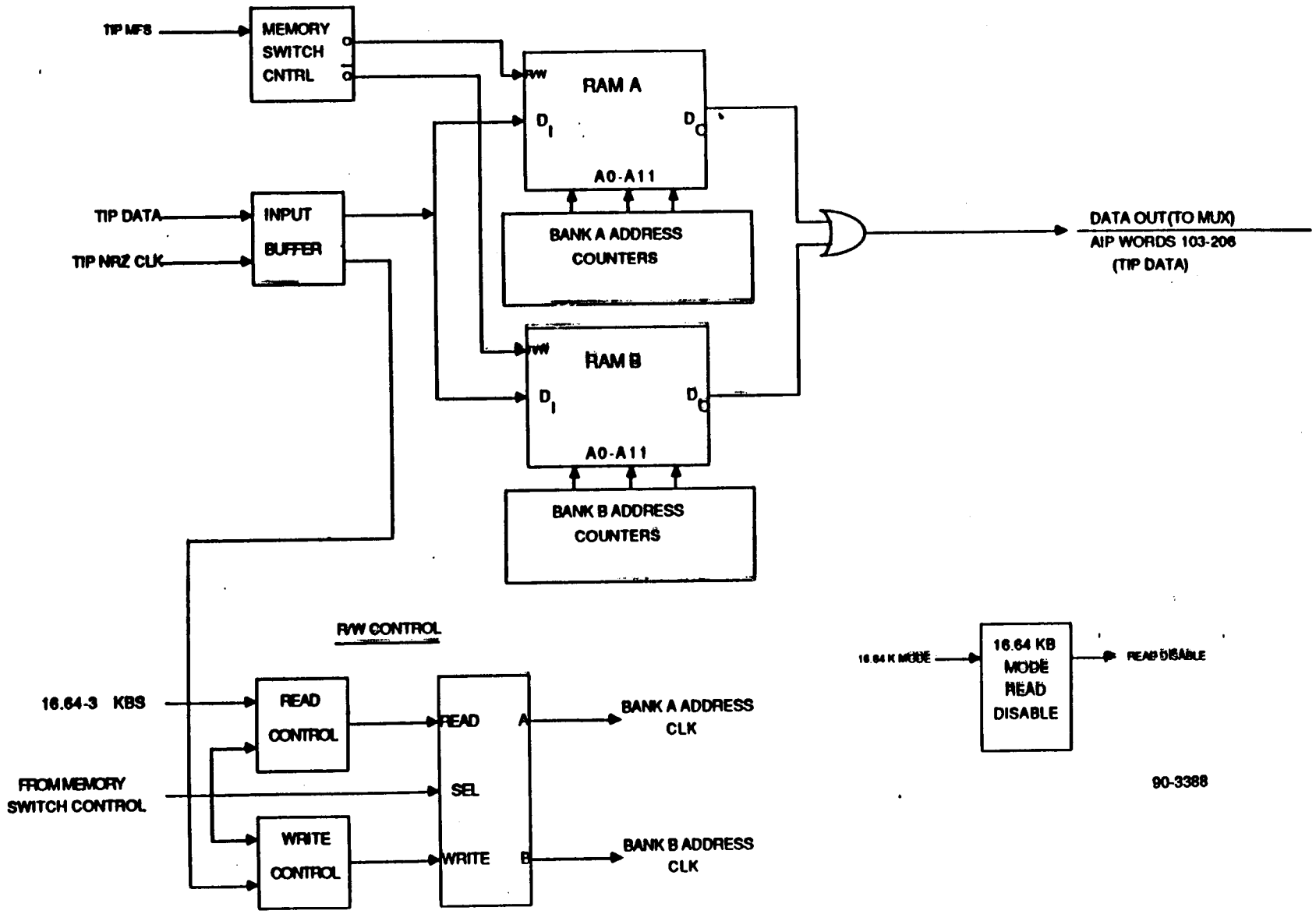

Figure 4.8.6-13. TIP Data Buffer Block Diagram

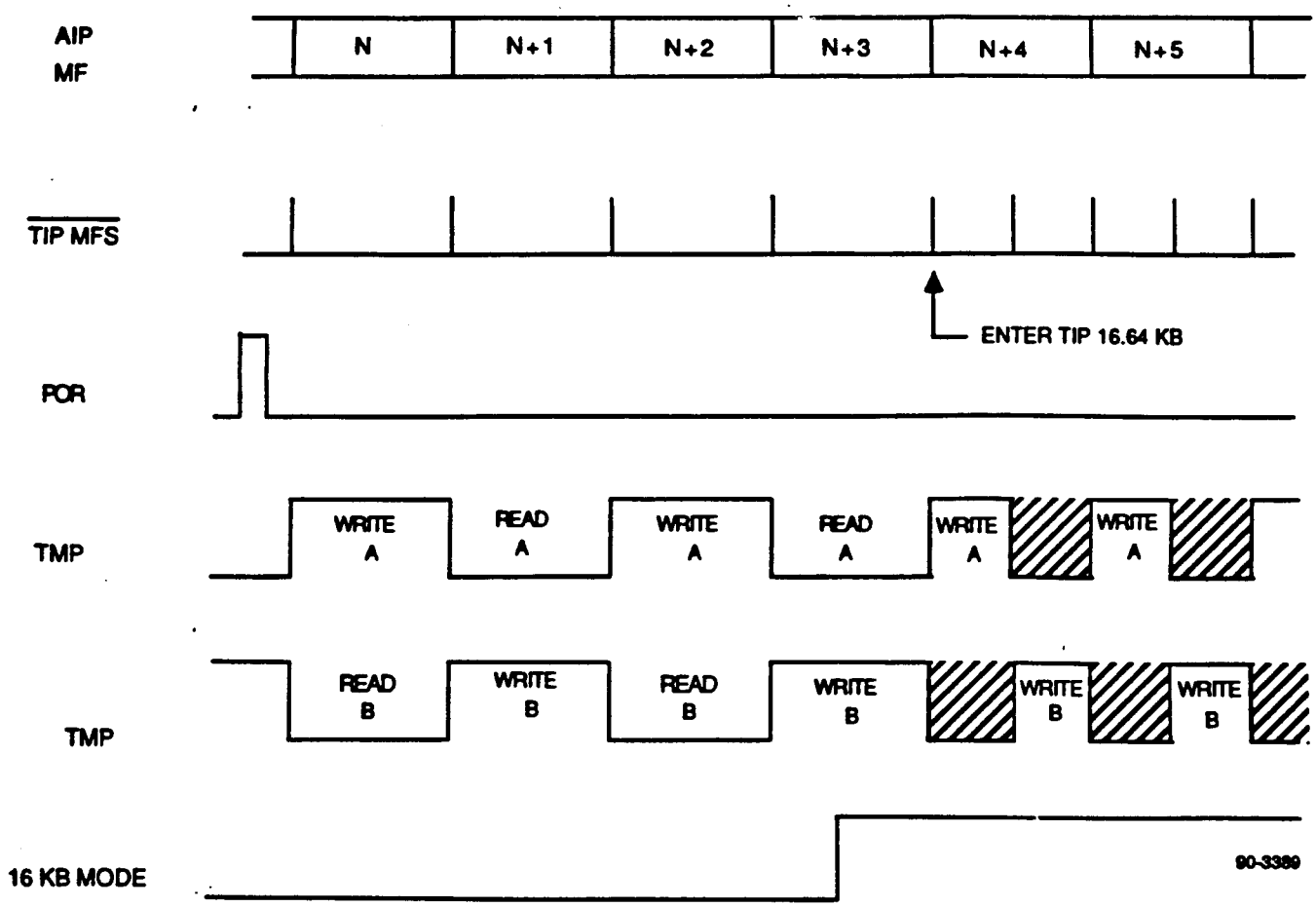

Figure 4.8.6-14. TIP R/W Memory Switching

Bits 3 through 8 of Minor Frame Word 207, as shown in Figure 4.8.6-3, are used for an even parity check on TIP Data. The bits have the following interpretation:

Bit	Interpretation
3	Even parity check on data contained in Minor Frame Words 105 through 121.
4	Even parity check on data contained in Minor Frame Words 122 through 138.
5	Even parity check on data contained in Minor Frame Words 139 through 155.
6	Even parity check on data contained in Minor Frame Words 156 through 172.
7	Even parity check on data contained in Minor Frame Words 173 through 189.
8	Even parity check on data contained in Minor Frame Words 190 through 205 including Bits 1 through 7 of Minor Frame Word 206.

This parity word amounts to a recalculation of the TIP parity which was calculated by the TIP (AIP word 206).

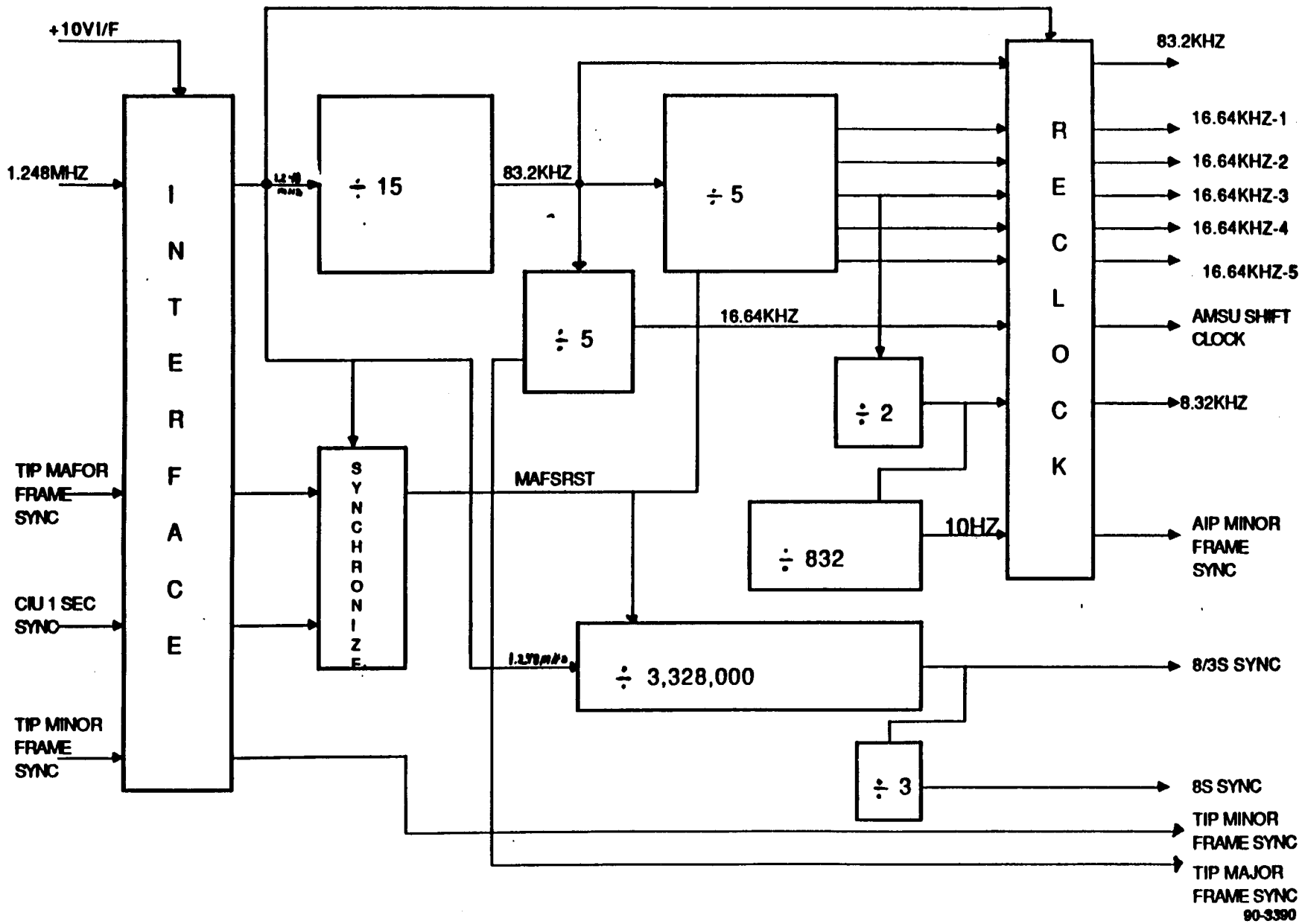

Figure 4.8.6-15. Timing Generator

4.8.6.3 Summary of AIP Characteristics

The AIP has the following characteristics:

Parameter	Characteristics
Inputs	AMSU-A1, -A2, -B at combined data rate of 7.2 kbps
	TIP Bi-phase and NRZ data at 8.32 or 16.64 kbps
	Clock/sync signals from XSU, TIP, and CIU
Outputs	NRZ-L Data to MIRP at 16.64 kbps (only the first 8.32 kb are used)
	NRZ-L and bi-phase data to the XSU at 16.64 kbps
	NRZ-L and bi-phase data to STE
Commands	Five pulse discrete commands to select one redundant side and the operating mode
Telemetry	Housekeeping telemetry to the TIP
Fault Tolerance	Except interface to non-redundant AMSU instruments, no single fault will prevent AMSU data from being output by the spacecraft
Size	8 inch long by 7.6 inch wide by 8.25 inch high
Weight	8 pounds
Power	10 MA @ 10V; 100 MA @ 28V

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4.9 COMMAND AND CONTROL

The basic function of the Command and Control Subsystem (C&CS) is to provide ascent guidance from booster separation through orbital injection, and to control the spacecraft attitude and operating modes on orbit. This control is exercised in accordance with commands and data received from the ground stations, supplemented by signals and data supplied by other spacecraft subsystems.

4.9.1 COMMAND AND CONTROL DESCRIPTION

A basic functional block diagram of the Command and Control Subsystem is shown in Figure 4.9.1-1. As shown, the C&CS consists of the following units:

- Redundant Crystal Oscillator (RXO)
- Controls Interface Unit (CIU)
- Standard Controls Processor 1 (CPU1)
- Standard Controls Processor 2 (CPU2)
- Signal Conditioning Unit (SCU)
- Controls Power Converter (CPC)
- CIU Annex (CXU)
- Decryption/Authentication Unit (DAU)

The RXO contains 2 highly stable, crystal controlled frequency sources, either of which is automatically selected to provide both 5.12 MHz signals to the CIU timing circuits. Each oscillator is placed within a temperature controlled Dewar flask oven, which provides a short term frequency stability of ± 1 part in 10^8 per day at +15°C and a long term stability of ± 1 part in 10^6 over 3 years.

Each CPU is a miniature, general purpose data processor operating in fractional fixed-point, 2's complement arithmetic. The CPU provides the computational capabilities required for real time, "hands-off" attitude control and for other data processing as required for satellite monitoring and control. Each CPU contains 32K words of read/write memory; the instruction set provided in the microprogram control ROM provides facilities for addressing memory, fetching instructions and data, performing arithmetic and logical operations, and loading and storing data.

The CIU contains all of the circuitry necessary to receive and verify command messages, to generate the various clock and timing signals required throughout the spacecraft, to coordinate the operation of the two CPUs, and to transfer data and control signals between each CPU and other spacecraft units. In effect, the CIU serves as the switching center between the CPUs and the remainder of the spacecraft.

The SCU contains the non-standard interface circuits for signals between the CIU and the remainder of the spacecraft. Standard interface logic such as CMOS and TTL interface directly with CMOS logic in the CIU; non-standard interface signals such as control coil drive current are provided by discrete component circuits within the SCU.

The CPC is located physically within the CIU container. The CPC provides the +10V and -10V power required by the CIU and CPUs and provides the +10V common bus distributed to external units for use as a common CMOS interface power bus.

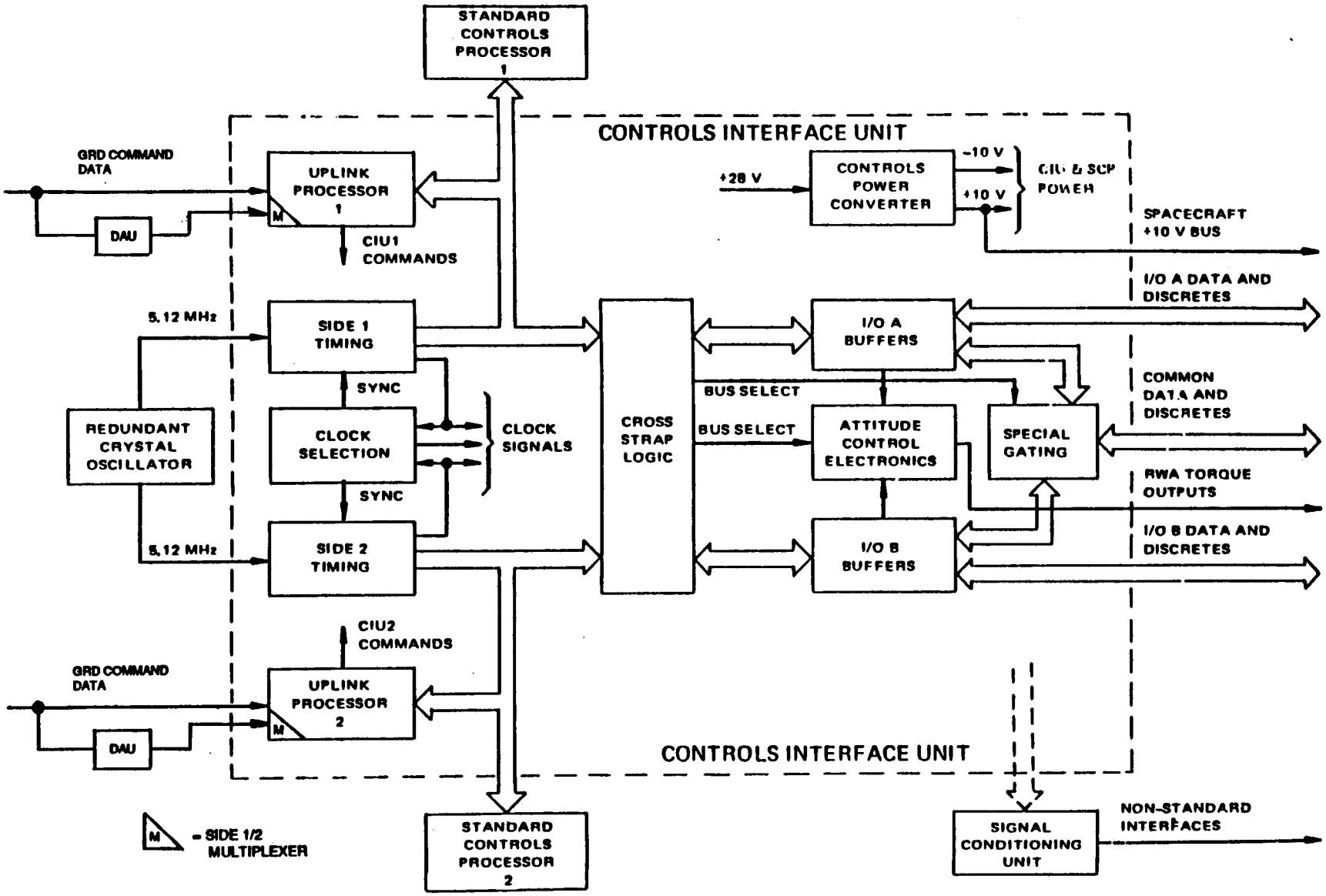


Figure 4.9.1-1. Command and Control Subsystem Block Diagram

4.9.2 EQUIPMENT DESCRIPTION

4.9.2.1 Redundant Crystal Oscillator

The Redundant Crystal Oscillator (RXO) is a highly stable, crystal controlled frequency source. As shown in Figure 4.9.2-1, the oscillator design features a dual oscillator selected by logic circuits and fed to two output signal jacks. The "in use" oscillator is automatically selected based on the outputs from amplitude and temperature failure detectors.

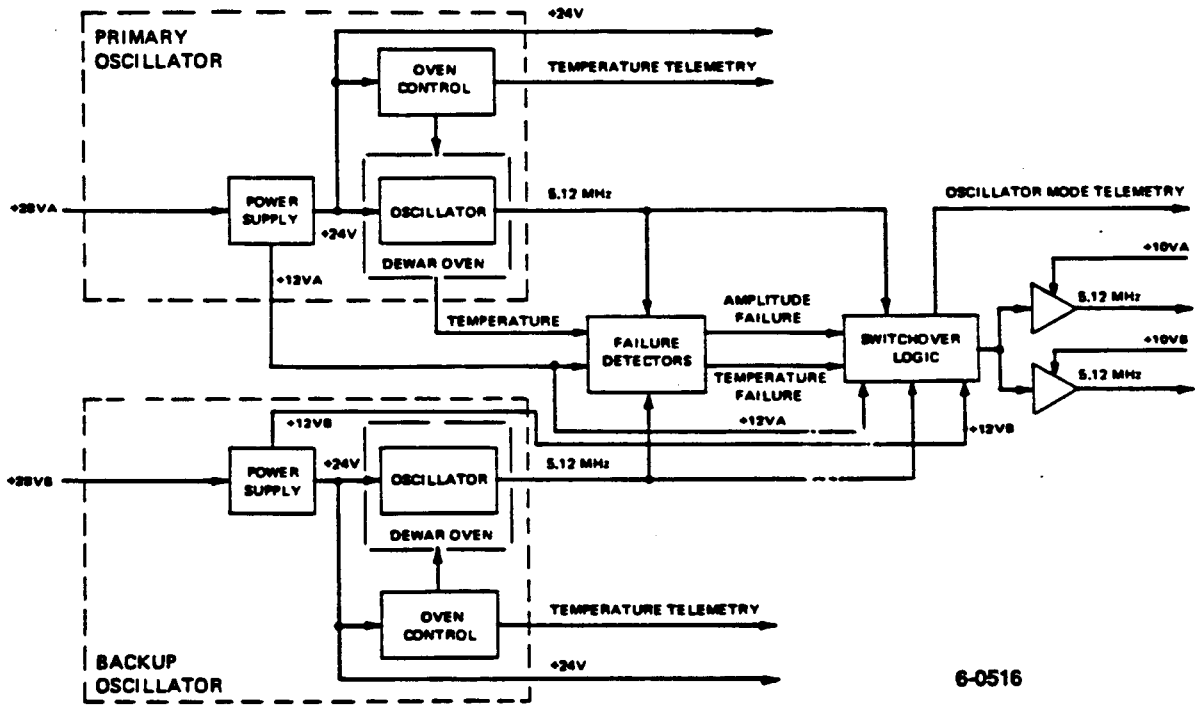


Figure 4.9.2-1. Redundant Crystal Oscillator Functional Block Diagram

The two crystal oscillators are designated the primary oscillator and backup oscillator, and are identical in configuration. Each oscillator is powered from an independent +24 volt regulator; each oscillator is housed in a separate Dewar flask oven assembly, the temperature of which is controlled by an independent oven control circuit. A temperature telemetry signal is provided from each ovencontrol circuit.

Outputs from both oscillators are fed to amplitude detectors, which sense the condition of the oscillators. The primary oven temperature is also fed to a temperature detector, which senses the condition of the primary oven. These signals provide failure indications to the switchover logic. The logic circuitry then automatically determines which oscillator is to provide the output signal. The RXO can be ground-commanded to the backup oscillator via a CIU decoded command. This ground selection is accomplished by shorting the primary oven-temperature reference source, simulating a primary oven temperature failure.

4.9.2.1.1 Redundant Crystal Oscillator Description

4.9.2.1.1.1 Design Approach. The design of the RXO is conventional, except for the oscillator assembly; modular construction is used throughout the unit, with integrated circuits utilized where possible.

The oscillator circuit boards are placed inside a Dewar flask oven to provide the required frequency accuracy and stability while minimizing power requirements. Proportional oven control heaters are provided to maintain the oven temperature at a fixed value. After assembly, the oscillator components are solidly encapsulated to retain the heat and to provide additional cushioning.

Electromagnetic interference is controlled by the solid physical construction of the unit and by filters in the power and control leads.

4.9.2.1.1.2 Operating Modes. The RXO operating modes are:

- Primary
- Backup

In the primary operating mode, the primary oscillator is providing the 5.12 MHz output signal; in the backup operating mode, the backup oscillator is providing the 5.12 MHz output signal.

Switchover from one operating mode to the other is automatic, based on the outputs from an amplitude failure detector for each oscillator and a temperature failure detector for the primary oscillator. Failure threshold points for the switchover logic are $\pm 5.0°C$ variation in temperature in the primary oscillator oven, 3.8 volts dc or less in the detected primary oscillator amplitude, and 2.0 volts dc or less in the detected backup oscillator amplitude.

All of the possible failure detection combinations and commanded modes are shown in the truth table in Table 4.9.2-1. Note that, regardless of the number of failures detected, one of the oscillators is always connected to the output.

4.9.2.1.1.3 Design Characteristics. The performance characteristics of the RXO are summarized in Table 4.9.2-2.

4.9.2.1.1.4 Physical Description. The RXO is a single, rectangular assembly, as shown in Figure 4.9.2-2. The housing contains 10 printed circuit boards and two independent Dewar flask oven assemblies. As shown in Figure 4.9.2-3, the printed circuit boards for the oscillator and buffer amplifier are mounted inside the oven; the oven control and voltage regulator boards are mounted inside the Dewar flask, but outside the oven; and the failure detector and switchover logic boards are mounted outside the Dewar flask, over the feedthrough terminal compartment.

After assembly, the oscillator components are solidly encapsulated with foam, which is used both to retain the heat inside the Dewar flask and to provide additional cushioning for the oscillator components.

TABLE 4.9.2-1. RXO FAILURE TRUTH TABLE

Condition	Failure Detector			RXO CMD Mode	Mode	
	Primary Amplitude	Backup Amplitude	Primary Temperature		Primary	Backup
1	+	+	+	Primary	1	
2	-	+	+	Primary		1
3	+	-	+	Primary	1	
4	-	-	+	Primary	1	
5	+	+	-	Primary		1
6	-	+	-	Primary		1
7	+	-	-	Primary	1	
8	-	-	-	Primary	1	
9	+	+	+	Backup		1
10	-	+	+	Backup		1
11	+	-	+	Backup	1	
12	-	-	+	Backup	1	
13	+	+	-	Backup		1
14	-	+	-	Backup		1
15	+	-	-	Backup	1	
16	-	-	-	Backup	1	

+ Operating
- Failed

4.9.2.1.2 Functional Description

4.9.2.1.2.1 Oven. The oven controller circuit is a proportional controller, providing power as required to maintain the oven temperature at a constant value. As shown in Figure 4.9.2-4, the controller consists of a bridge network with a thermistor in one leg, a differential amplifier, and a heater element.

4.9.2.1.2.2 Thermistor. The thermistor is the temperature sensing element. Any change in temperature results in a thermistor resistance change, which is reflected as a voltage change at the input to the differential amplifier. The differential amplifier then causes proportionally more or less current to flow through the heater winding, driving the oven temperature back toward its equilibrium value.

The heater winding is wound around the oven body, providing an even source of heat and a stable ambient temperature.

TABLE 4.9.2-2. RXO DESIGN CHARACTERISTICS

Parameter	Value
Output Frequency	5.12 MHz square wave
Frequency Stability	
Short Term at Constant Temperature Between -5°C and +45°C	± 1 part in 10^8 per day
Long Term	± 1 part in 10^6 over 3 years
Operating Temperature	-5 to +45°C
Operating Modes	Primary and Backup
Mode Switchover Threshold	
Primary Oven Temperature	± 5.0°C variation
Primary Oscillator Amplitude	<3.8 Vdc
Backup Oscillator Amplitude	<2.0 Vdc
Telemetry	
Operating Mode (Discrete)	
Primary	0 V
Backup	+4 V
Primary Oven Temperature	Analog Curve
Backup Oven Temperature	Analog Curve
Power Requirements (Maximum)	
+28 Vdc	180 mA
+10 Vdc	20 mA
Size	4.875 x 6.0 x 2.125 (inches)
Weight	1.6 lbs

A second thermistor sensor is provided for the purpose of telemetering the oven temperature. In the primary oscillator a third thermistor is used for sensing in the temperature failure detector circuit.

4.9.2.1.2.3 Oscillator. The crystals used in the RXO oscillator circuits are of the FC cut type. They exhibit very low aging characteristics, typically in the order of one part in 10^{10} per day. The crystal is a 3rd overtone cut crystal, mounted in a "C" type holder using a three pin mount, which provides excellent mounting and minimum sensitivity to shock and orientation.

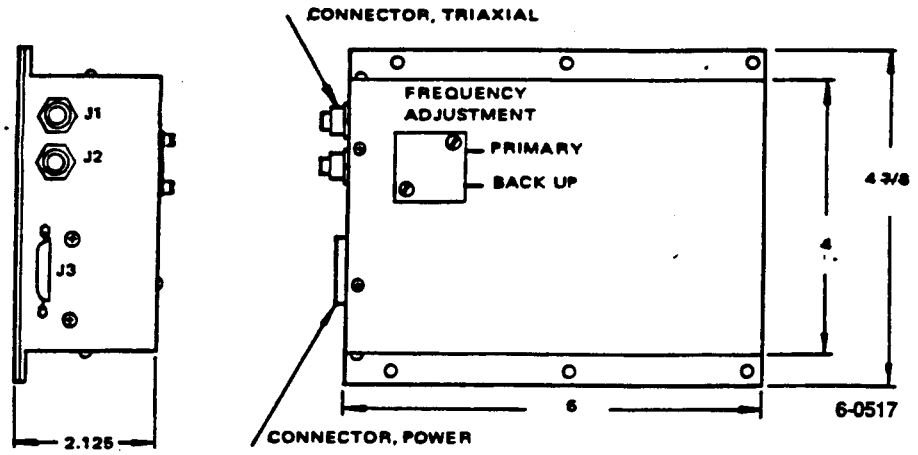


Figure 4.9.2-2. RXO Physical Configuration

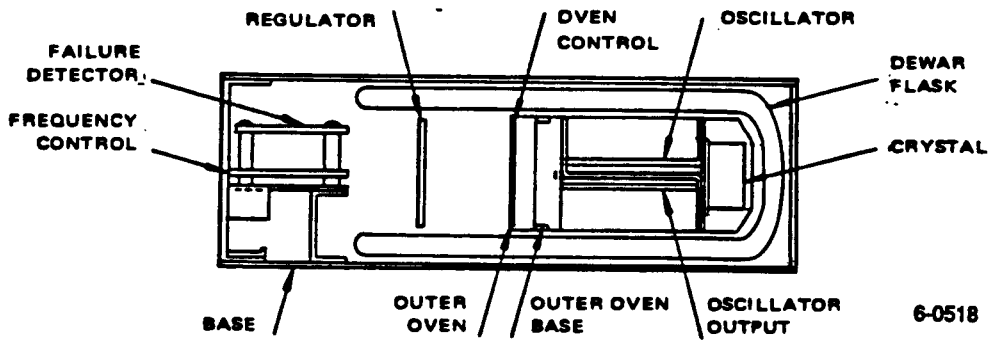


Figure 4.9.2-3. RXO Internal View

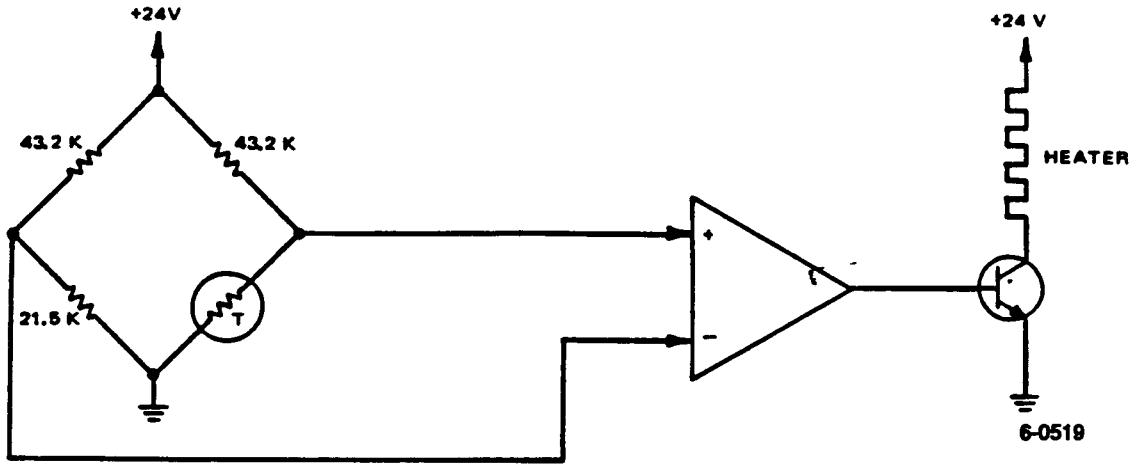


Figure 4.9.2-4. Oven Temperature Controller

A fine frequency adjust potentiometer control is provided in a circuit which uses a V947 varactor diode as the frequency changing component. As the potentiometer is adjusted the voltage applied to the varactor diode changes the capacitance of the diode, resulting in a commensurate change in oscillator frequency.

4.9.2.1.3 Failure Detector and Switchover Circuitry

The failure detector circuitry receives the 5.12 MHz signal outputs of the primary oscillator and the backup oscillator, and a signal from a thermistor in the primary oscillator oven. These three signals are thresholded and used to drive the logic circuits in the frequency selector circuits. In accordance with the presence or absence of these three signals as shown in Table 4.9.2-1, the switchover circuitry selects one of the oscillators for providing the output signal.

The backup oscillator select input signal is also fed to the failure detector circuits, to enable the selection of the backup oscillator as the signal source, both during ground test and by command in orbit.

4.9.2.1.4 Telemetry

There are three telemetry signals provided by the RXO:

- Oscillator Mode
- Primary Oven Temperature
- Backup Oven Temperature

The oscillator mode telemetry provides a discrete output signal indicating whether the primary or backup oscillator is providing the output signal. This signal is 0 volts in the primary mode, or +4 volts in the backup mode.

The primary oven and backup oven telemetry signals are analog signals provided via a thermistor sensor in each oven. These signals indicate the operating temperature of the primary and backup ovens, thus providing a primary indication of the health of the RXO.

4.9.2.1.5 Command

The RXO receives a command line from the CIU which enables ground selection of the RXO backup mode. This selection is accomplished by grounding the RXO primary oven temperature reference input voltage (RXO backup oscillator enable command line) to the comparator in the failure detector circuit. This results in an indicated primary oven temperature failure and RXO mode selection as per Table 4.9.2-1. The inactive state of this command provides an open circuit to the RXO which allows normal operation of the failure detection circuits for RXO selection. The command does not require a clock signal from the RXO to execute, thus the RXO can be commanded whether or not there is an RXO output.

4.9.2.2 Controls Interface Unit (CIU)

The Controls Interface Unit (CIU) contains all of the circuitry (primarily digital logic) necessary to generate the various clock and timing signals required by the C&CS and other spacecraft units, to coordinate the operation of the two

C&CS CPU's, and to transfer data and control signals between each CPU and other spacecraft units. The Controls Power Converter (CPC), which is described in Section 4.9.2.5, is located physically within the CIU container and supplies all ±10V power used by the CIU and CPUs. The +10V common bus from the CPC is distributed from the CIU to external units for use as a common COS/MOS interface power bus.

The functions performed by the CIU may be summarized as follows:

1. Receipt and decoding of command messages and data from the GSTDN-Compatible Command Receiver Demodulator (GRD), either directly or through the Decryption/Authentication Unit, and transmission of appropriate data to the CPU.

2. Receipt and buffering of data from various other spacecraft units or from other parts of the CIU, and transmission of this data to the appropriate CPU.

3. Receipt and buffering of data and control signals from either CPU, and transmission of this data to the appropriate spacecraft unit or to a part of the CIU.

4. Receipt and buffering of control signals from other spacecraft units or from parts of the CIU and transmission of these signals as priority interrupts or as flags to the appropriate CPU. Some priority interrupts may be disabled by the associated CPU.

5. Cross-strap switching of certain interface lines to allow selective connection of either CPU to either of two interface trunks. This switching is normally controlled from software in the CPU selected for this purpose by ground command. CPU status monitoring logic is provided, to detect software or hardware errors in either CPU. If the control CPU fails, the other CPU is automatically placed in control of the cross-strap switching.

6. Distribution of clock frequencies to both CPUs and to other spacecraft units and sections of the CIU.

7. Provision of a Time Code Counter (TCC) and associated buffers to allow either CPU to determine "real time".

8. Conversion of power from +28 volts to ±10 volts as required for CPU and CIU operation and provision of a +10 volt interface bus to other spacecraft units.

4.9.2.2.1 Design Description

A functional block diagram of the CIU is shown in Figure 4.9.2-5. As shown, the CIU includes clock and timing generation logic, uplink processors, CPU interface control logic, CPU/CIU I/O bus control logic, spacecraft interface buffers and control logic, attitude control electronics, and power on reset generators.

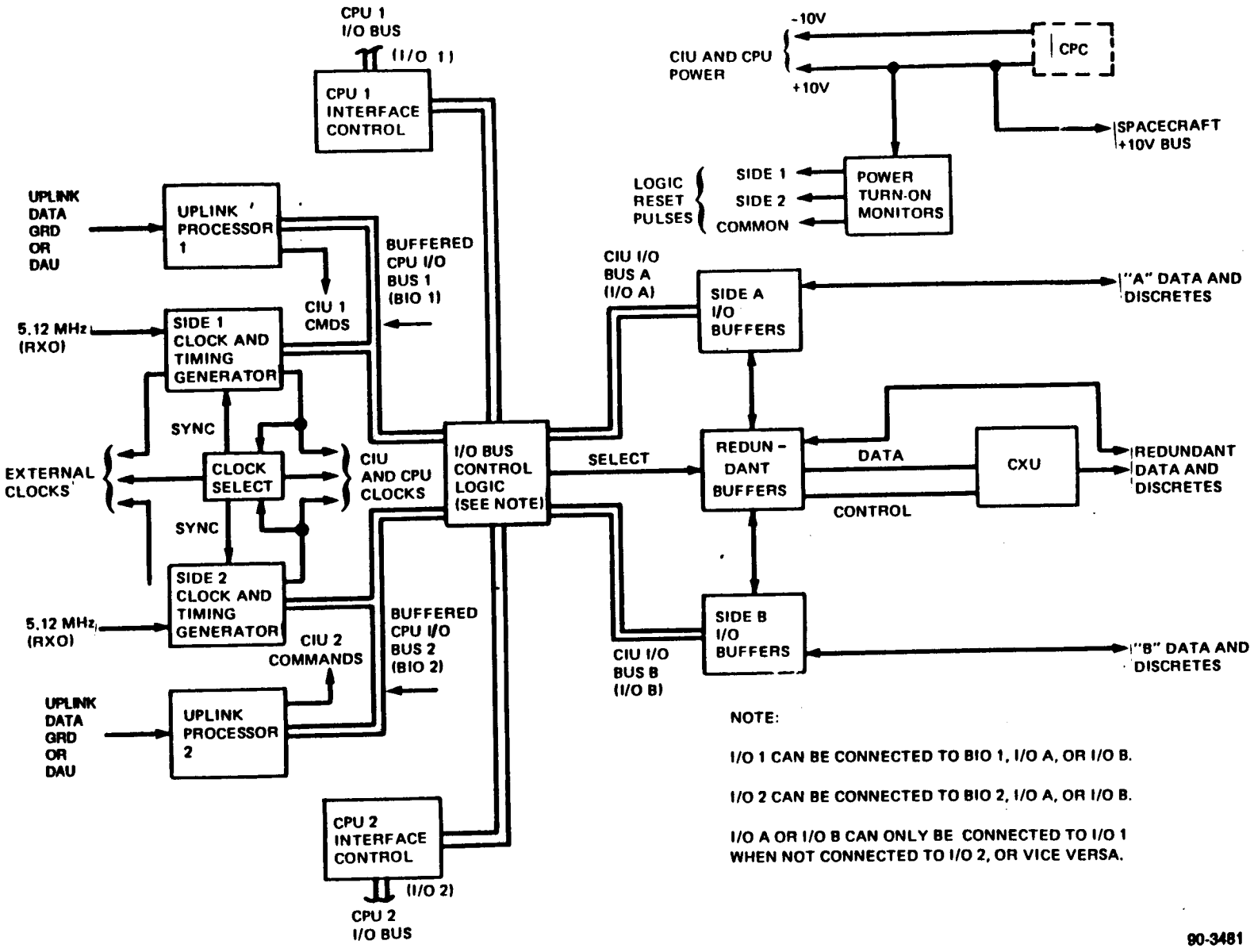


Figure 4.9.2-5. CIU Functional Block Diagram

The clock and timing generation logic utilizes digital countdown chains and frequency synthesizers to reduce the 5.12 MHz RXO clock input to lower-frequency clocks and timing (sync) signals required by the CPUs, the CIU, and other spacecraft units.

The uplink processors contain the logic required to input uplink data from the GRD or DAU at 2 Kbps. They examine the uplink words for correct address and length, detect GRD sync, and perform single error correction. The uplink processors decode and execute CIU (hardware) commands, or output uplink message words to the CPUs as CPU commands or data words according to the designation (CIC) codes. CIU (hardware) decoded commands via the uplink processors are used to control redundancy states of the CIU, CPUs, and RXO.

The CPU interface control logic provides for the buffering and reclocking of data and control signals transferred between the CIU and the CPUs. These operations minimize loading on the high speed I/O buses and re-establish critical timing relationships among data, control signals, and clocks.

The I/O bus control logic establishes the unambiguous connections between each buffered CPU I/O bus and one of the CIU I/O buses.

The spacecraft interface buffer and control logic includes storage registers and sequencers as required to permit the asynchronous transfer of serial data and discretes between the CPUs and the various spacecraft units (including the CIU).

The attitude control electronics decodes and converts digital torque commands from the enabled I/O bus interface buffer into analog torque control levels for output to the RWAs, and also converts the analog RWA tachometer signals into digital speed and direction signals for input to the CPU.

The reset generators sense the absence, then application, of power on one or all of the +10V buses from the CPC; upon (re)application of power on any of these buses, the reset generator provides a power-on-reset pulse output to initialize the CIU logic powered from the reactivated bus.

4.9.2.2.1.1 Design Approach. The basic functional organization of the CIU is shown in Figure 4.9.2-6. As shown, the CIU is essentially a dual unit, with fully independent timing, uplink processor, and interface control logic for each CPU (sides 1 and 2) and redundant spacecraft interface (I/O) buffers (buses A and B).

Side 1 logic is associated uniquely with CPU1 to ensure the logical integrity of, and uplink access to, the CPU1 I/O bus; side 2 logic replicates side 1 and is associated uniquely with CPU2. All non-CPU functions (CIU command decodes) are redundantly performed by the two uplink processors and the resulting outputs are logically combined as appropriate. The selection of either side 1 or side 2 timing signals as the source of common clocks is controlled by CIU commands.

The I/O bus control logic contains switching gates to connect CPU1 to either bus A (normal) or bus B (crossed) and CPU2 to the remaining bus. The I/O bus configuration is normally controlled by CIU commands, but the I/O bus control

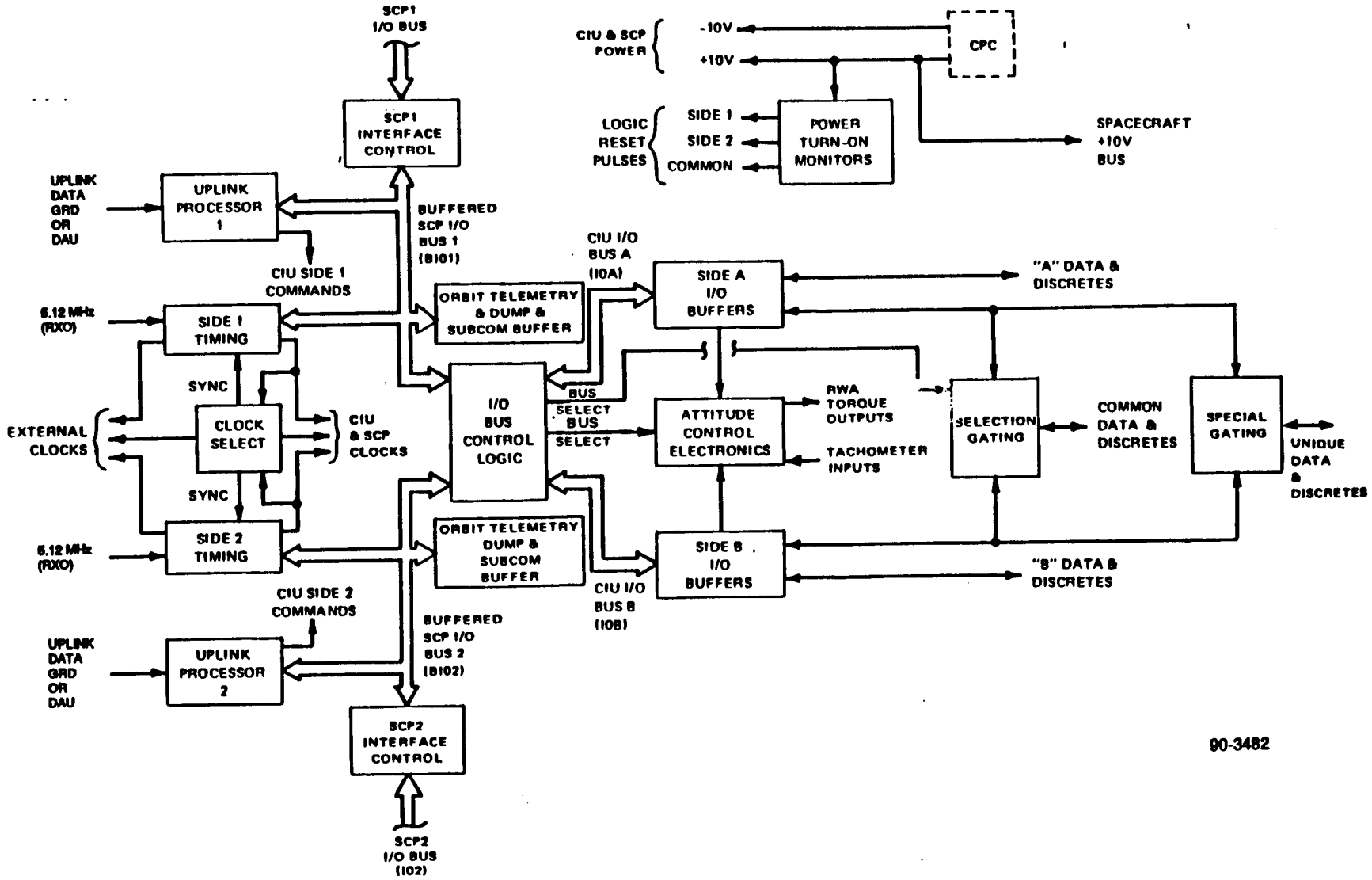


Figure 4.9.2-6. CIU Design Organization

logic enables the control CPU, via software, to cross buses to output to the non-control bus, and also to override the ground-designated selection of which bus is "master."

The power turn-on monitors include separate detectors for the +10V-1 and +10V-2 which provide unique logic reset pulse outputs to initialize only that logic powered by the bus being turned on. At initial power turn on or total power interrupt, both reset pulse outputs are generated, initializing the entire CIU and both CPU's; any subsequent interruption of +10V-1 or +10V-2 produces a reset pulse only for CPU1/side 1 logic or CPU2/side 2 logic as appropriate.

4.9.2.2.1.2 Operating Modes. The operating modes of the CIU are controlled both internally within the CIU and in response to control signals from the CRD via the uplink processor.

The operating modes controlled internally within the CIU include the uplink processor states, the many states of the data and control buffers, the interrupt controller states, and the cross strap gating selection. These internal operating modes are described fully in Section 4.9.2.2.2. The operating modes controlled in response to control signals from the uplink processor are described in the remainder of this section.

4.9.2.2.1.2.1 CPU Power Control. Power to CPU1, CPU2, and to the associated electronics in the CIU is controlled in response to four control signals from the uplink processor.

- CPU1 Power On
- CPU1 Power Off
- CPU2 Power On
- CPU2 Power Off

On receipt of the CPU1 Power On control signal, the power is turned on to CPU1 and CIU side 1; on receipt of the CPU1 Power Off control signal, the power is turned off to CPU1 and CIU side 1 if and only if CPU2 and CIU side 2 are not already off. In an analogous manner, power to CPU2 and CIU side 2 is controlled in response to the CPU2 Power On and CPU2 Power Off control signals.

Since the uplink processor uses the same power supply as the associated CPU (CPU1 and uplink processor 1 from +10V-1, for example), CPU1 power can only be controlled from uplink processor 2 and CPU2 power can only be controlled from uplink processor 1. The uplink processor generates a 'Pulse Type' command to execute these commands.

4.9.2.2.1.2.2 CPU Selection. One of the two CPUs is selected as the master CPU in response to one of two control signals from the uplink processor.

- Select CPU1
- Select CPU2

On receipt of a Select CPU1 or 2 command, the selected CPU is placed in control, provided that CPU is reporting OK. When in control, the master CPU determines the state of the cross strap switch, connecting CPU1(2) to I/O-A(B). The control CPU also may veto the ground commanded bus selection.

When either Select CPU command is received, both CPU status indicators are reset to the OK state, allowing the CPU to remain "on-line" if it is healthy. The uplink processor generates a 'Level Type' command to execute these commands.

4.9.2.2.1.2.3 CIU Clock Selection. One of the two CIU clocks is selected in response to one of two control signals from the uplink processor.

- Select Clock 1
- Select Clock 2

On receipt of the Select Clock 1 control signal, the timing signals from clock countdown timing chain 1 are selected as the primary spacecraft timing source; on receipt of the Select Clock 2 control signal, the timing signals from clock countdown timing chain 2 are selected as the primary spacecraft timing source. The uplink processor generates a 'Level Type' command to execute these commands.

4.9.2.2.1.2.4 Bus Selection. Where redundant buffers are used, the source of external data and command discretes is selected to be either a buffer on the I/O-A bus or a buffer on the I/O-B bus. Selection is in response to two control signals from the uplink processor.

- Select Bus A
- Select Bus B

On receipt of the Select Bus A control signal, the redundant buffers on the I/O-A bus are connected to the CIU command interfaces; on receipt of the Select Bus B control signal, the redundant buffers on the I/O-B bus are connected to the CIU command interfaces. The uplink processor generates a 'Level Type' command to execute these commands. The selection established by ground station command may be changed by the CPU which is in control via an output discrete set by software labeled Veto Bus Selection. When activated, this discrete will cause the selected bus to be changed from that selected by ground station command to the other redundant bus.

4.9.2.2.1.2.5 CPU Memory Selection. Memory modes to CPU1 and CPU2 are controlled in response to four control signals from the uplink processor.

- Select CPU1 Memory Normal
- Select CPU1 Memory Swap
- Select CPU2 Memory Normal
- Select CPU2 Memory Swap

On receipt of the select CPU1 memory normal control signal, the CPU1 command line is set to +10 volts, logic 0 (memory normal). On receipt of the select CPU1 memory swap control signal, the CPU command line is set to 0 volts, logic 1 (memory swap). In an analogous manner, memory mode to CPU2 is controlled in response to the select CPU2 memory normal and CPU2 memory swap control signals.

The controls signals from uplink processor 1 select CPU1 memory mode and conversely the control signals from uplink processor 2 select CPU2 memory mode. The uplink processor generates a 'Level Type' command to execute these commands. These commands enable the designated memory selection but do not actually cause a change. A CPU reset command is required to accomplish the change.

4.9.2.2.1.2.6 RXO Mode Selection. One of the two RXO modes is selected in response to two control signals from the uplink processor.

- Select RXO Primary Mode
- Select RXO Backup Mode

On receipt of the select RXO primary mode control signal, the uplink processor will provide an open circuit (open collector) to the RXO backup oscillator enable command line. On receipt of the select RXO backup mode, the uplink processor will provide a short to ground (0 $\pm$.3 volt) to the RXO backup oscillator enable command line. The uplink processor generates a 'Level Type' command to execute these commands.

4.9.2.2.1.3 Design Characteristics. The general design characteristics of the CIU are given in Table 4.9.2-3.

The CIU external data transfer buffering logic consists of data input buffers, data output buffers, and special control and gating logic. Most of these buffers are used to transfer data between external interfaces (with other parts of the spacecraft and/or with other parts of the CIU) and the I/O-A or the I/O-B interfaces. The remainder of the external data transfer buffer logic is used to transfer data between other parts of the CIU or external units and the dedicated buffered CPU I/O (BIO1 and BIO2) interfaces.

4.9.2.2.1.4 Physical Description. The CIU consists of an electronics box containing 23 welded wire circuit boards, one welded wire harness board, and, within a separate compartment, a CPC assembly. The major construction features of the CIU are shown in Figure 4.9.2-7. Distribution of the CIU functions and of the I/O buffers are shown in Table 4.9.2-4.

Most of the data buffers are located on 11 modular I/O buffer boards. These boards interface with either the I/O-A bus, with the I/O-B bus, or with both buses. Necessary differences in buffer functions i.e., output voltage, power-on-reset state, etc. are implemented by appropriate wiring of the CIU harness board, which interconnects all CIU circuit boards.

Three different types of I/O boards are used:

1. Type 1 contains one 16-bit Serial Input Buffer (SIB), two 16-bit Serial Output Buffers (SOB), and two 16-bit Parallel Output Buffers (POB). This board type connects to a single I/O bus and is generally used for non-redundant commands.

2. Type 2 contains the same complement of buffers as the type 1 board, but provides for cross strapping of signals for serial and parallel buffers from a redundant source. These boards are used in pairs with one connected to the I/O-A bus and the second connected to the I/O-B bus. The external signals are then connected to buffers on one of the two redundant buses under control of the Bus Selection control signal generated within the CIU.

TABLE 4.9.2-3. CIU DESIGN CHARACTERISTICS

Parameter	Value or Description
Data Input/Output Interfaces	
Type	Serial NRZ; MSB first standard
Bit Rate	102.4 kbs standard
Level Conventions	+10V or +5V = False or Data Zero 0V = True or Data One
Discrete Input/Output Interfaces	
Type	Bi-level; single-ended
Level Conventions	+10V or +5V = Off, False, or Inactive 0V = On, True, or Active
High Frequency Clock Interfaces	
Range	200 kHz to 5.12 MHz
Waveform	Squarewave; duty cycle 50 ±5%
Voltage Levels	0V/+10V nominal
Transmission	COS/MOS to COS/MOS via 93 ohm Triax cable; inner shield used as AC return
Interface Power Buses	+10V ±5%; +5V ±5%
Redundancy	Dual Power Converter with separate ±10V outputs and common +10V output Separate isolated timing, access, and interface logic for CPU Redundant clock outputs selectable by command Separate complement of spacecraft I/O buffers for each CPU; CPUs interchangeable on ground command via software
Power Consumption	<7.0 W at +28V
Size	17.6 x 7.6 x 9.3 inches
Weight	<23.6 lbs.

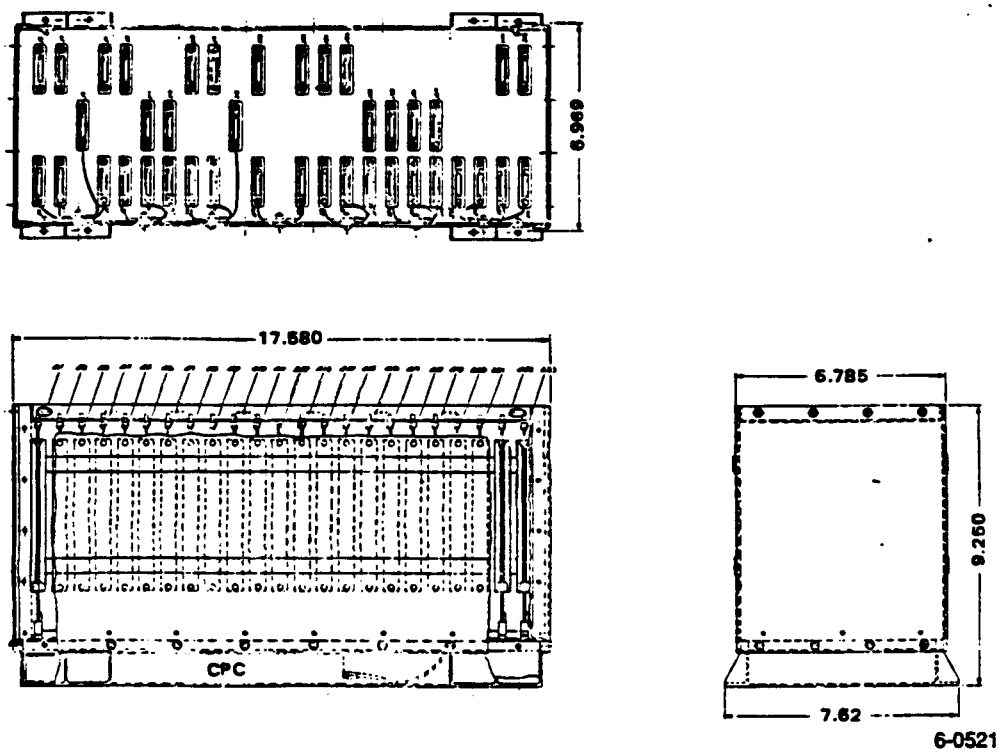


Figure 4.9.2-7. CIU Physical Configuration

3. Type 3 contains eight 16-bit parallel output buffers. This board connects to both the I/O-A and the I/O-B buses. Half of the POBs are connected to each bus and cross strapping is performed on the board under control of the Bus Selection control signal to provide a capacity of four redundant type POBs.

4.9.2.2.2 Functional Description

The CIU may be divided into six distinct functional blocks: power turn-on monitors, CPU interface controllers, clock and timing generators, uplink processors, I/O bus control logic, and I/O circuits.

4.9.2.2.2.1 Power Turn on Monitors. The power turn-on monitors combine analog and digital design techniques to bootstrap detect the interruption of power (loss of voltage) on any or all of the +10V buses from the CPC and, upon re-application of power, generate a one-shot logic reset pulse specific to the interrupted bus (or buses). A complete schematic diagram of the power turn on monitors is shown in Figure 4.9.2-8.

The Power-On-Reset 1 (POR1) pulse is generated whenever +10V-1 power (from the CPC) turns on. Normally, this follows application of +28 volt input power to CPC converter A. Similarly, the Power-On-Reset 2 (POR2) pulse is associated with turn on of +10V-2 power and the application of +28 volt input power to CPC converter B.

TABLE 4.9.2-4. CIU BUFFERS

		Buffer Totals							
Board No.	Function	POB		PIB		SOB		SIB	
		R	NR	R	NR	R	NR	R	NR
3/10	RWA Control	1		1					
4/9	Timing				4				
5/8	Uplink Processor				2				
6/7	CPU Interface	1							
11/12	Miscellaneous		2						3
1/2/13/14/15	I/O Type 1		10			2	6	1 +1/2 +1/2	1
16/17/18/19/20/21	I/O Type 2	6				6		2 +1/2 +1/2	
22/23	I/O Type 3	8							
Total		16	12	1	6	8	6	5	4

Notes: R = Redundant Buffer = 2 Buffers with same address
NR = Nonredundant Buffer

The Power-On-Reset Spacecraft (PORS) pulse is generated if the POR1 and POR2 pulses occur simultaneously, or if either occurs while the "other side" power is off; either of these conditions is indicative of a total power interrupt affecting the +10V common (spacecraft) bus as well as the +10V-1 and +10V-2 buses. Redundant circuits are used and one (PORS-A) is distributed to circuits on the A side of the CIU while the other (PORS-B) is distributed to circuits on the B side of the CIU.

4.9.2.2.2.1.1 Reset Pulse Generation. The POR1 and POR2 pulse generators are functionally identical; a description of the POR1 generator follows.

When the +10V-1 bus is unpowered, there is a sufficiently low equivalent load impedance to maintain the bus at virtual ground; the gate input coupling capacitor C11 is fully discharged.

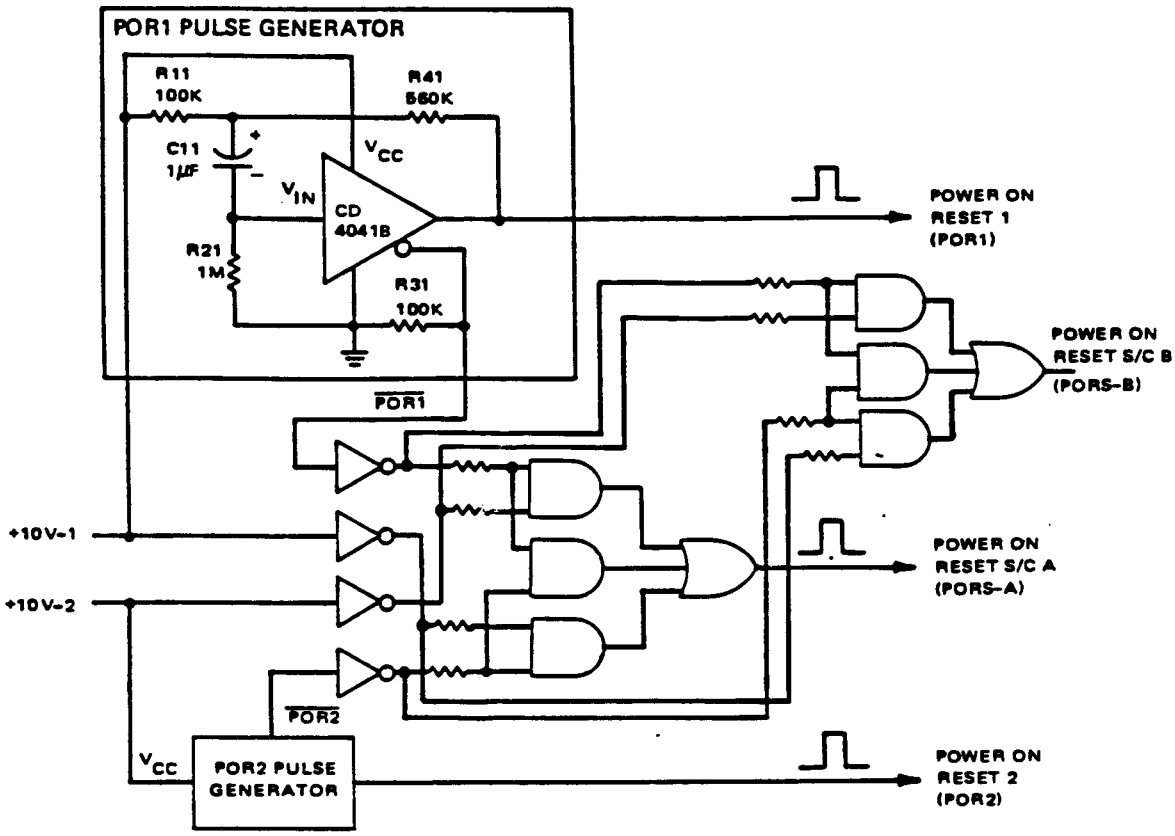


Figure 4.9.2-8. Power Turn-On Monitor Circuits

The bus turn-on time is negligible compared to the time constant of the capacitor charge circuit (≈1 second), so that at turn-on the gate input voltage (V_{in}) is

$$V_{in} = 10V \left[\frac{1\ \text{Meg}}{1\ \text{Meg} + (100K) \quad (560K) \div (660K)} \right] = 9.2V$$

producing a high (active) gate output to the POR1 line. Capacitor C11 then charges through R11/R41 and R21 with a nominal time constant (τ) of

$$\tau = \left[\frac{100K \times 560K}{660K} + 1\ \text{Meg} \right] (1 \times 10^{-6} F) = 1.08 \text{ second.}$$

The gate output remains high until V_{in} falls below +5V (nominal), or until the voltage across C11 is approximately 5V. Since

$$V_{C11} = 10 \left[1 - e-t/t^{-t/r} \right],$$

V_{C11} = 5V at t = 0.75 seconds (nominal).

The logical presence of (POR1 "and" $\overline{+10V-2}$) or (POR1 "and" POR2) produces PORS.

A similar analysis shows that the interruption of the +10V-1 bus for 0.75 seconds (nominal) or more re-enables the reset pulse generator.

Under a worst case combination of component values and CD4041B thresholds, the minimum reset pulse duration is 0.23 seconds. This is more than adequate to maintain the reset(s) until buses have stabilized and relay states have been established (<<100 msec).

4.9.2.2.2.1.2 Command and Control Subsystem Initialization. At spacecraft power turn-on, the design of the CPU Power Controller in the SCU (Paragraph 4.9.2.4) and the CPC (Paragraph 4.9.2.5) assure that the spacecraft +10V common bus and at least 1 of the 2 CPU +10V buses (+10V-1 and/or +10V-2) are activated, producing a PORS pulse. The occurrence of PORS automatically activates both the CPU1 On and CPU2 On control signals to the SCU via the uplink processors, assuring that both CPU +10V busses are activated. At spacecraft power turn-on, therefore, the integrated C&CS design assures complete activation of both CPUs and all CIU logic. Logic interlocks prevent the subsequent generation of PORS when only 1 of the 2 CPU +10V buses is interrupted at a time.

4.9.2.2.2.1.3 CIU Initialization. As previously noted, each of the three reset pulse outputs is used to initialize (where required) that portion of the CIU logic powered by the associated +10V bus. Since the +10V spacecraft (common) bus is used to power all external interfaces and all CIU logic except for the CPU interface controllers and uplink processors, the basic CIU configuration and interface signal levels are initialized only at spacecraft power turn on (PORS). The remainder of the CIU comprises two identical logic segments, each associated uniquely with one CPU and powered by the same +10V bus (-1 or -2) supplied to that CPU; each of these logic segments is re-initialized (POR1 or POR2) each time the associated CPUs power is turned on to preclude spurious I/O operations during the power transient. The specifics of logic initialization will be identified as applicable in the remainder of this section; a general summary is as follows:

1. Spacecraft Power-On-Reset (PORS)

   - Turns on the power to at least 1 CPU
   - Puts the CIU in Orbit mode with both CPU CAPs closed
   - Resets both CPU status flags to OK

- Generates side 1/side 2 timing sync and resets time code counter
- "Selects" clock 1 as the master time base and source for cross strapped clocks
- Connects CPU1 to I/O-A, CPU2 to I/O-B
- Selects CPU1 to be in control
- Presets Bus Select A to be active
- Sets output discretes to known state

2. Power On Reset 1 or 2 (PORn)

- Generates CPUn Restart (software reset) and sets CPUn interrupt masks
- Clears Uplink Processor 1 and 2 data checking and command decode logic to inactive states

4.9.2.2.2.2 Uplink Processors. Each Uplink Processor (UP) receives serial digital words from the GSTDN Command Receiver Demodulator (GRD) or the Decryption/Authentication Unit (DAU) and supplies digital words or decoded control signals to other CIU functions. The two uplink processors are functionally identical units, designated UP1 and UP2, one of which is shown in Figure 4.9.2-9. The uplink processors examine the incoming serial data to verify proper format and to determine the processing to be performed on the data.

UP1 is restricted to communicate only with CPU1 via BIO1 and the interrupt 1 (INT1) lines, and is powered from the same bus as CPU1. Similarly, UP2 communicates only with CPU2 and is powered with CPU2. Execution of some CIU decoded commands can be via either uplink processor.

The major functions of the Uplink Processor are:

- Synchronizes the DAU and CIU to the GRD Data Stream
- Receives 32-bit commands from a GRD or DAU at 2000 bps
- Provides cross-strapping for two DAUs
- Single error correction/double error detection is provided with a (32,25) hamming code
- Checks the address of each data word against a unique processor address coded by a connector selectable address patch
- Controls and executes CIU decoded commands
- Passes data, commands, and status to the CPU via a bio bus for words with valid addresses or double-bit errors
- Provides a data hold time of 15.5 mS

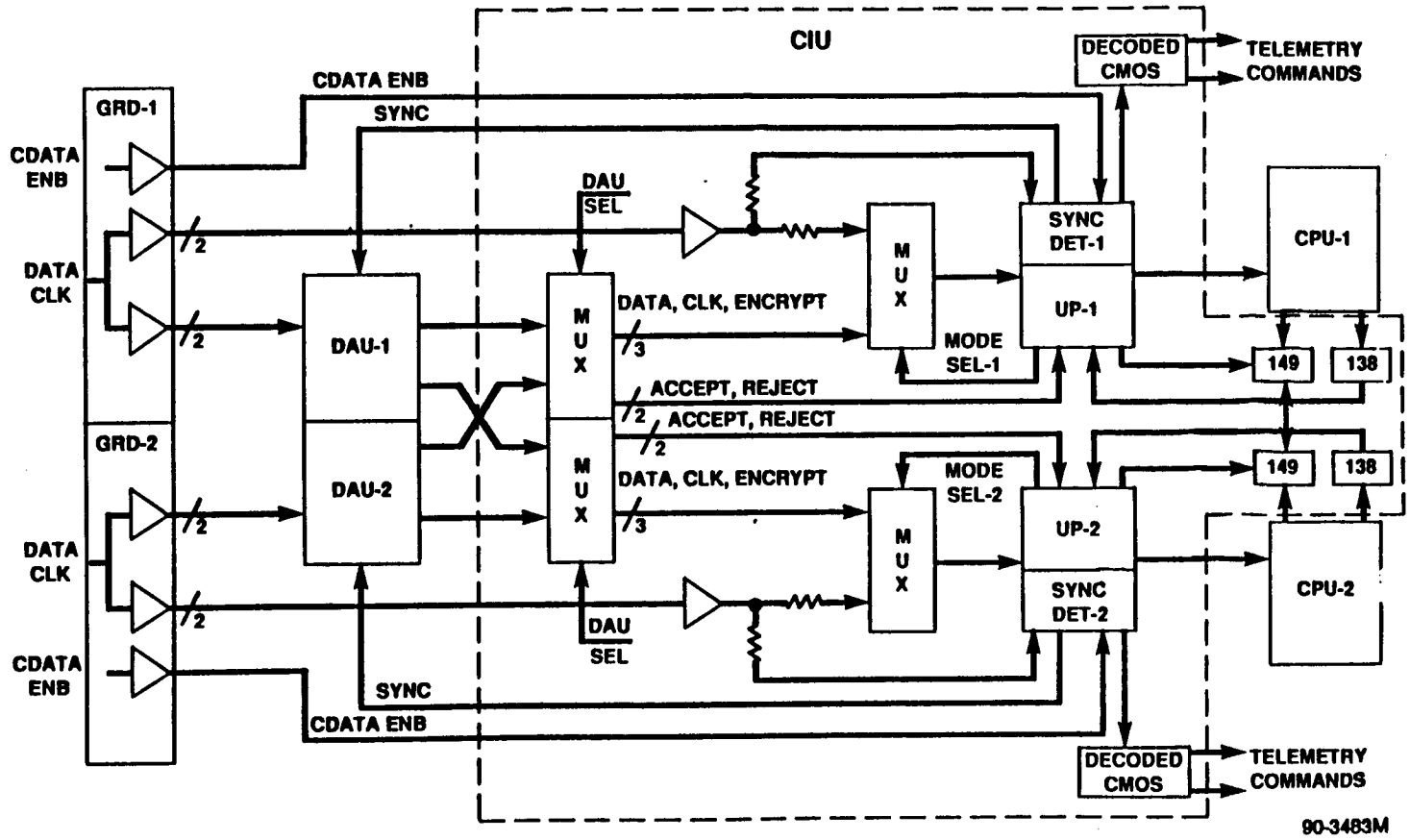


Figure 4.9.2-9. Uplink Processor Interface Diagram

4.9.2.2.2.2.1 Command Formats. The GSTDN uplink format is shown in Figure 4.9.2-10a for both plain text uplink and cipher text uplink. Figure 4.9.2-10b shows how, in the plain text mode, each 32-bit "command" breaks down to a 7-bit address, a 2-bit CIC code, the 16-bit active field, and 7 check bits for error correction. Similarly, Figure 4.9.2-10c shows the breakdown in the encrypted mode. Figure 4.9.2-10d shows how the CIC field and the 16-bit active field are used.

4.9.2.2.2.2.2 UP Data Capture Functions. The Uplink Processor performs two functions: Data Capture and Data Processing, as shown in Figure 4.9.2-11. The capture/processing flow is shown in Figure 4.9.2-12. Table 4.9.2-5 summarizes the command uplink accept/reject criteria. These functions operate at the input data rate of 2 kHz. Each UP receives data from one of three possible data sources: DAU1, DAU2, or a GRD. Each DAU receives encrypted data from the GRDs. If GRD data is encrypted, the DAUs decode the data into plain text format. Both DAU1 and UP1 are synchronized to the GRD1 data frames by the sync detector located on UP1. Similarly, both DAU2 and UP2 are synchronized to the GRD2 data frames by the sync detector located on UP2. Each UP captures and stores the 32-bit data words it receives from the DAU or GRD data stream. The bit flow into the data buffer is shown in Figure 4.9.2-13.

Sync detector logic, located on each UP, distinguishes sync from the GRD data path and synchronizes the UPs and DAUs to the beginning of each data frame. When sync is detected, the uplink processor is configured so that the next received bit is the first bit of the 32-bit data word. Once sync has been detected, any future sync signals are ignored until a double-bit error occurs, a Reject pulse is received, or POR (Power On Reset) occurs. When sync is detected, a sync pulse signal is sent to the DAU. The sync code is transmitted in plain text NRZ-M format using an 8-bit Barker sync pattern (11110010 NRZ-L format).

Sync detection is enabled at any time if:

1) The Data Enable n 1(2) signal from the GRD goes on, meaning that the carrier signal was removed.

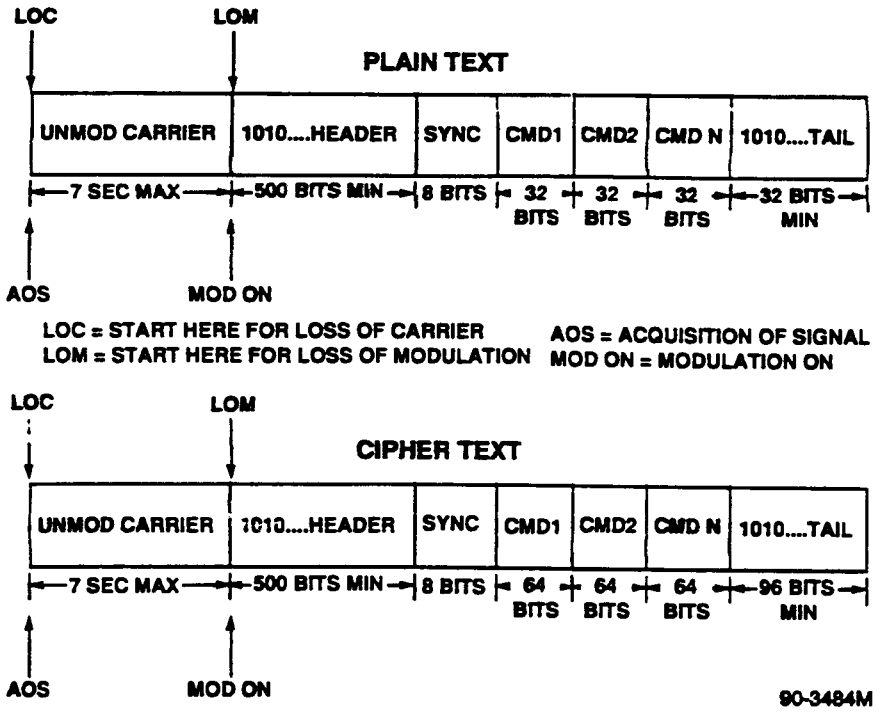
2) A double-bit error is detected by a hamming decoder.

3) Nine sequential DAU "Rejects" are counted (cipher text mode only)

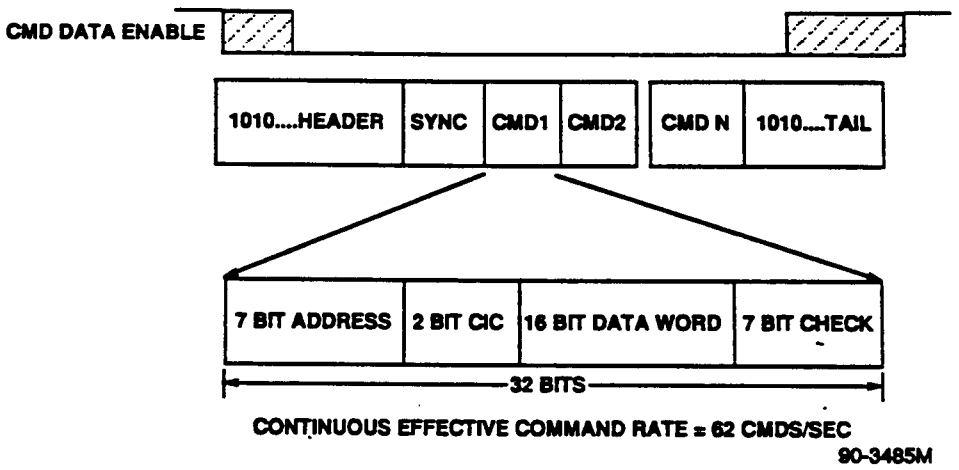
4) Power On Reset occurs.

Sync detection may be enabled from the ground using the 1010...10 signal (1111...11 NRZ-L format) sent at the beginning of each ground station transmission. This signal can cause either nine "Rejects" from the DAU (if in cipher text mode) or a double-bit hamming code error (if in plain text mode). Sync detection is also enabled at the beginning of a transmission when the carrier signal is removed at the end of the previous transmission.

Prior to receiving sync, several unsynchronized, therefore invalid, data words can pass through the UPs to the CPU if those data words contain double-bit errors. The UP does not pass a data word with an invalid CPU address unless that word contains a double-bit error.

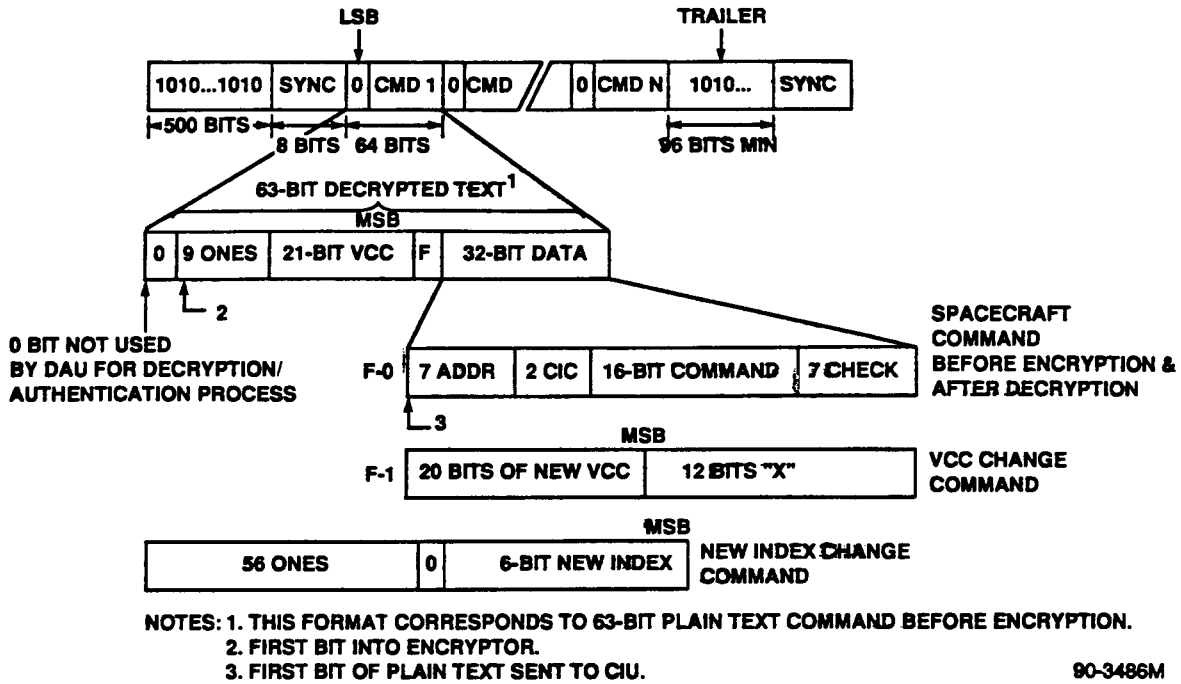


a. GSTDN Uplink Format



b. Uplink Format: Plain Text

Figure 4.9.2-10. Command Formats (Sheet 1 of 2)



NOTES: 1. THIS FORMAT CORRESPONDS TO 63-BIT PLAIN TEXT COMMAND BEFORE ENCRYPTION.
2. FIRST BIT INTO ENCRYPTOR.
3. FIRST BIT OF PLAIN TEXT SENT TO CIU.

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c. Uplink Format: Cipher Text

0 0 CIC CODE NOT USED/ASSIGNED

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
SATELLITE ADDRESS							01		16 BITS/CIU DECODED COMMAND																HAMMING CODE						

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
SATELLITE ADDRESS							10		16 BITS/CPU COMMAND																HAMMING CODE						

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
SATELLITE ADDRESS							11		16 BITS/CPU DATA WORD																HAMMING CODE						

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d. Uplink Command/Data Formats

Figure 4.9.2-10. Command Formats (Sheet 2 of 2)

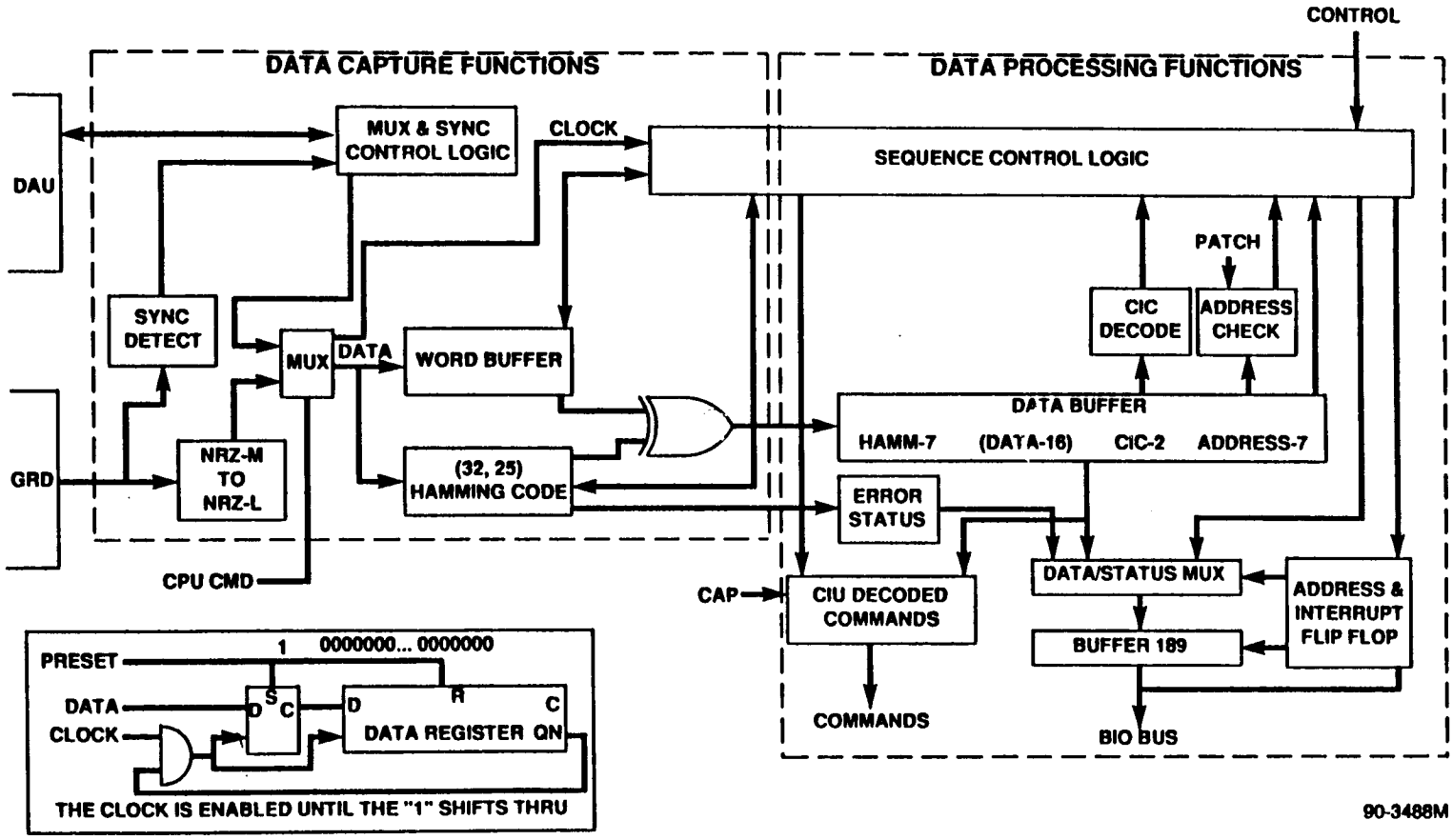

Figure 4.9.2-11. UP Block Diagram

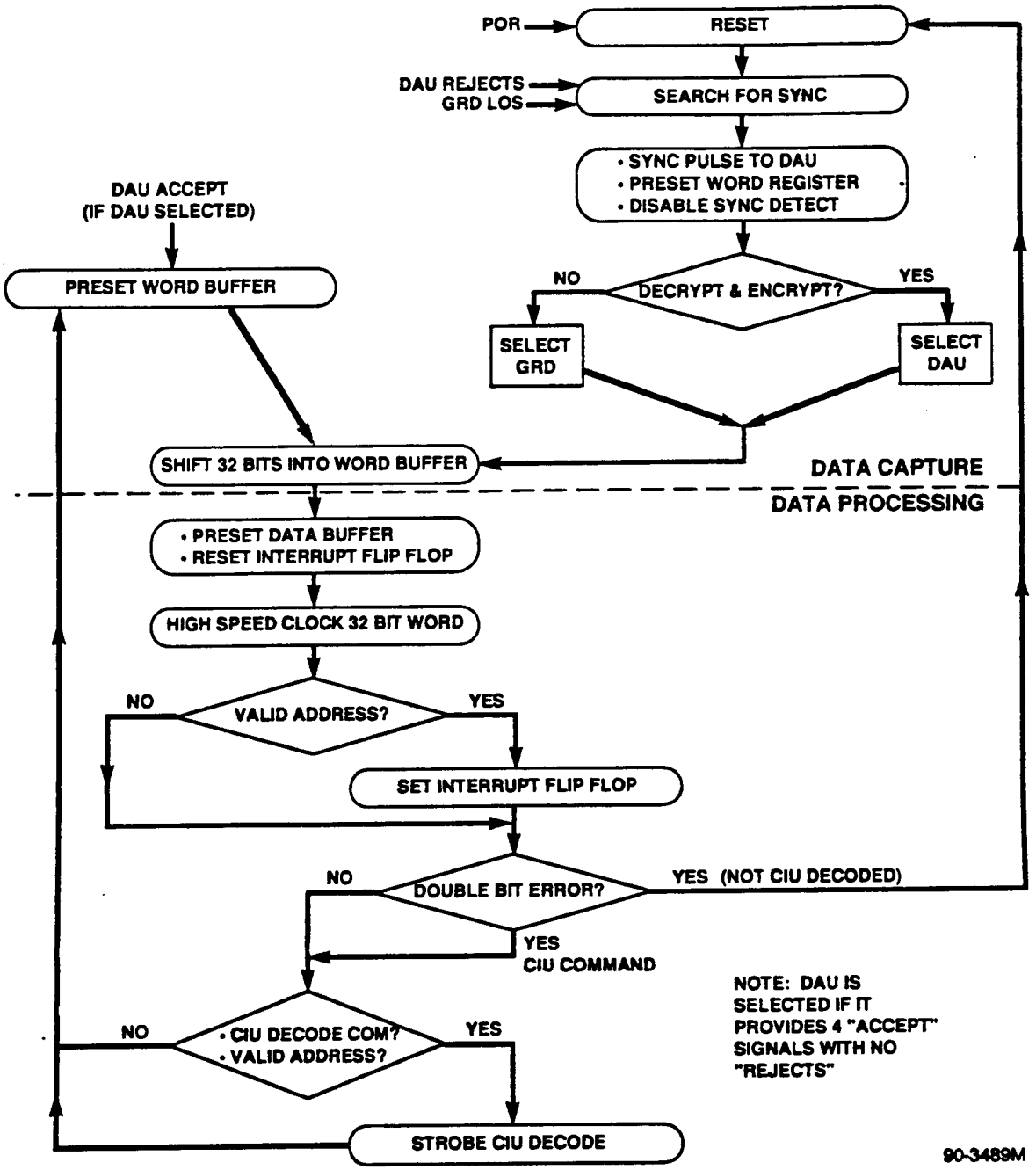

Figure 4.9.2-12. UP Flow Chart

WORD and DATA REGISTER CONTENTS

TIME	RECEIVED BIT	WORD BUFFER 32	31	30	29		3	2	1	1	DATA BUFFER 32	31	30	29		3	2	1	1	
T0	B32	1	0	0	0	·····	0	0	0	0	x	x	x	x	·····	x	x	x	x	Waiting for next bit.
T1	B1	B1	1	0	0	·····	0	0	0	0	x	x	x	x	·····	x	x	x	x	
T2	B2	B2	B1	1	0	·····	0	0	0	0	x	x	x	x	·····	x	x	x	x	
T3	B3	B3	B2	B1	1	·····	0	0	0	0	x	x	x	x	·····	x	x	x	x	
		⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	
T29	B29	B29	B28	B27	B26	·····	1	0	0	0	x	x	x	x	·····	x	x	x	x	
T30	B30	B30	B29	B28	B27	·····	B1	1	0	0	x	x	x	x	·····	x	x	x	x	
T31	B31	B31	B30	B29	B28	·····	B2	B2	1	0	x	x	x	x	·····	x	x	x	x	
T32-0	B32	B32	B31	B30	B29	·····	B3	B2	B1	1	x	x	x	x	·····	x	x	x	x	
T32-1		B32	B32	B31	B30	·····	B3	B2	B1	1	1	0	0	0	·····	0	0	0	0	Data Buffer Preset & High Speed Clock Enabled
T32-2		B32	B32	B32	B31	·····	B4	B3	B2	1	B1	1	0	0	·····	0	0	0	0	
T32-3		B32	B32	B32	B32	·····	B5	B4	B3	1	B2	B1	1	0	·····	0	0	0	0	
T32-4		B32	B32	B32	B32	·····	B6	B5	B4	1	B3	B2	B1	1	·····	0	0	0	0	
DATA CLOCK	HIGH SPEED CLOCK	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	
T32-30		B32	B32	B32	B32	·····	B32	B31	B30	1	B29	B28	B27	B26	·····	1	0	0	0	
T32-31		B32	B32	B32	B32	·····	B32	B32	B31	1	B30	B29	B28	B27	·····	B1	1	0	0	
T32-32		B32	B32	B32	B32	·····	B32	B32	B32	1	B31	B30	B29	B28	·····	B2	B2	1	0	
T32-33		B32	B32	B32	B32	·····	B32	B32	B32	1	B32	B31	B30	B29	·····	B3	B2	B1	1	Data Buffer Clock Disabled CIC Strobe, Word Buffer Preset, Interrupt Flip Flop Set
T32-34		1	0	0	0	·····	0	0	0	0	B32	B31	B30	B29	·····	B3	B2	B1	1	
T32-35		1	0	0	0	·····	0	0	0	0	B32	B31	B30	B29	·····	B3	B2	B1	1	Strobe, Set & Preset Removed

90-3490

Figure 4.9.2-13. UP Data Register Flow

TABLE 4.9.2-5. UPLINK COMMAND REJECT/ACCEPT CRITERIA

Invalid Spacecraft Address	• CPU not interrupted
Double Bit Error Within Command Frame	• CPU interrupted • Error status provided • CIU decoded commands not accepted • Uplink processor enables sync detect logic
Reject Signals From Selector DAU	• Uplink processor enables sync detect logic if the uplink has the DAU selected
DAU Encrypt or Decrypt 138-bit 12 Signal Removed	• Switches to GRD data stream • If this happens while a data word is loading, the incorrect data word could fail the hamming code check and start the sync detect mode

After receiving sync, a synchronized data word with a valid address is passed through the UP to the CPU. The sync detection function is disabled when sync is detected. Status of the sync detection function is indicated in the UP status word on buffer 189.

The GRD data stream is input to the UP in a plain decoded NRZ-M format (plain text mode). Encrypted data is decoded by the DAUs and input to the UPs in plain decoded NRZ-L format (Cipher text mode). The GRD/DAU data path is selected by Decrypt Mode, a level signal from bit 12 of buffer 138. If the plain text mode is selected, the UP receives data from the GRD data stream. If the cipher text mode is selected, the UP receives data from the "accepting" DAU. The UP provides two signals for each buffer 149 indicating if the UP is in cipher text mode.

The "accepting" DAU is the DAU that receives synchronized data encrypted with a matching encryption key code. The DAUs are programmed with different encryption keys; therefore, only one DAU accepts data at a time. As a result, DAU selection is made by the encryption key used for the ground station transmission. In summary, a DAU only accepts GRD data if the encryption key matches and if the DAU is synchronized to the data stream.

The cross-strap selection is achieved by counting Accept and Reject signals. A DAU "accepting" data produces an Accept signal for each data word. A DAU rejecting data produces a Reject signal for each data word. Each UP selects the DAU that produces four Accept signals in a row (no Reject signals). If the selected DAU provides nine Reject signals in a row, sync detection is enabled. Both UPs select the same "accepting" DAU input stream; therefore, identical data is passed to both UPs at the same time. However, only one UP at a time passes data to the CPU because both CPUs have different addresses.

Three possible data path configurations exist:

1) GRD1 → DAU1 ↔ UP1 & UP2
   GRD2 & DAU2 = not used

2) GRD2 → DAU2 ↔ UP2 & UP1
   GRD1 & DAU1 = not used

3) GRD1 → UP1
   GRD2 → UP2
   DAU1 & DAU2 = not used

Invalid modes of operation: If both DAUs present four accepts with no rejects at the same time, both DAUs are selected at the same time for one data word. Under this condition, an UP will OR together the signals from both DAUs for one data word. This condition occurs again after four more accepts are generated by both DAUs at the same time. The DAU selected is random during these four accepts. This problem will not occur if the decryption keys in both DAUs are always different because the data would only be valid for one DAU at a time.

4.9.2.2.2.2.3 UP Data Processing Functions. Data processing operates at a fast clock rate of 180 kHz. Data processing begins after the UP receives a data word. Data processing corrects single-bit errors, detects double-bit errors, checks the data word for a matching CPU address, strobes a CIU decoded command, provides a status word, and sends a data word to the CPU.

Single-error correction/double-error detection are provided with a (32,25) hamming decoder. The status word bit 3 indicates if a single-bit error was corrected. The status word bit 4 indicates if a double-bit error was detected. The status word changes during high speed data processing as the error is detected. Whenever a word is received with a double-bit error, this word is passed through to the CPU via the BIO bus.

After processing a data word, the UP checks the address of the data word against the unique CPU address. This CPU address will be coded by a connector selectable address patch. If the address matches, data is passed through to the CPU.

Each UP is capable of issuing 16 different decoded commands. Two of these commands are not used. If the CIC code of the data word indicates that the data word is a CIU decoded command and the data word does not contain a double-bit error, the CIU decoded command is issued.

Buffer 189 passes data, commands, and status through the BIO bus to the CPU for any word with a valid address or a double-bit error. Information held in buffer 189 is only changed during high speed data processing and therefore is characterized as having a data hold time of 15.5 mS. The presence of data is indicated by a level-12 interrupt signal. This signal is removed during the high speed data processing and reissued when the data processing is complete. This signal is also removed when the access to buffer 189 is removed by the CPU.

4.9.2.2.2.2.4 Circuit Level Operational Description. The Uplink Processor is composed of circuits that implement five principle functions: power supply isolation, sync detection, data capture, data processing, and CIU decoded command execution. The following paragraphs describe the circuits required to operate each function.

Sync detection circuits, data capture/processing circuits, and CIU decoded command circuits are power-, resistor-, and chip-isolated from one another. This isolation of circuit functions localizes the impact of single-point failures. The DAU cross-strap data capture circuits, located on the A12 board, are power-supply-isolated from the A5/A8 boards. However, these circuits are resistor-isolated from the A5/A8 boards because they interface with other data capture circuits.

Each of the power supply isolation circuits uses 1.0 μF and 0.1 μF bypass capacitors to filter out noise from the power supply. Additional 0.1 μF capacitors are positioned on the boards to buffer the transient current required by CMOS driver chips. These capacitors store enough energy to provide power for the high speed data processing which occurs at a clock speed of 180 kHz for durations of less than 40 clock cycles.

The sync detector logic, located on the A5/A8 boards, consists of an NRZ-M to NRZ-L conversion circuit, an 8-bit shift register circuit, a sync enable flip-flop circuit, and a sync pulse generator circuit. The sync detector logic is enabled by clocking the sync enable flip-flop circuit to the "on" state. The NRZ-M to NRZ-L conversion circuit converts the data as the data is clocked into the 8-bit shift register circuit. The 8-bit shift register circuit checks the data stream for a Barker sync code. When the shifted data bits represent the sync code, sync is detected and the sync pulse will be issued. The sync pulse will turn "off" the sync enable flip-flop circuit on the edge of the falling clock signal. The sync pulse will be transmitted to the DAU via the A12 board.

The data capture logic consists of input selection logic and data word storage logic. This logic receives and captures each data word into a word buffer register. High speed data processing takes place before the start of the next data word and after a complete data word is received. The data capture logic is synchronized to the data stream by the sync detector logic.

The input selection logic consists of DAU cross-strap logic, NRZ-M to NRZ-L conversion logic, and GRD/DAU mux logic. The DAU cross-strap logic is located on the A12 board. The NRZ-M to NRZ-L conversion logic and GRD/DAU mux logic is located on the A5/A8 boards.

The DAU signals are isolated from each other by redundant output drivers located on each DAU. The Data, Clock, Encrypt, Accept, and Reject signals are received from the selected DAU using the cross-strap mux logic. The accept and reject signals are used to control counters that implement the following functionality. The "accepting" DAU is the last DAU to send four Accept signals. If the selected DAU sends nine Reject signals before the other DAU sends four Accept signals and the UP is in the cipher text mode, the sync detector logic will become enabled.

The GRD data stream will be translated from NRZ-M to NRZ-L format. This conversion will take place by driving a D-flip-flop/exclusive OR circuit with the GRD NRZ-M data stream. After this conversion takes place an additional flip-flop circuit is used to hold the data thus allowing for clock skew caused by the clock control circuit delays.

The GRD data stream is selected if logic level signal Decrypt Mode 1/(2) or Encrypt 1(2) is low. The Encrypt 1(2) signal comes from the selected DAU. The Decrypt Mode 1/(2) signal comes from buffer 138.

The input data will be selected by the GRD/DAU Mux and piped into the word buffer logic and (32,25) hamming decoder. The word buffer will be initialized by being preset to 10000...0 to count in the 32-bits. The preset "1" will be used to indicate when 32-bits are received and therefore signal that a fully loaded word is ready. The hamming code syndrome generator is initialized as this data is loaded. The word buffer inverts the seven hamming code bits because these bits are inverted as they are transmitted from the ground station. The clock signal for the word buffer logic comes through the clock control circuits. After receiving a 32-bit data word, the clock control circuits high speed clocks the data word out of the word buffer, through the hamming decoder, and into the data buffer.

The word buffer and hamming decoder are preset when:

1) In the cipher text mode, the selected DAU sends an accept signal.
2) Power On Reset occurs.
3) Sync is detected.
4) The data processing strobe pulse logic sends a strobe pulse to initialize for the next data word.

The data processing functions are implemented by those logic circuits driven by a high speed data processing clock. The word buffer logic and (32,25) hamming decoder logic operates at both the slow data capture rate of 2 Kbs and the high speed data processing rate of 180 Kbs. The high speed data processing circuitry will start working when a full 32-bit data word is loaded into the word buffer logic as indicated by the preset "1" signal. Data processing circuits include clock control circuits, hamming decoder, data buffer logic, CIC decode logic, address check logic, error status logic, strobe pulse logic, buffer 189 interface logic.

The clock control circuits drive at the slow speed input data clock rate after the word buffer and hamming decoder are preset. After the full data word is captured, the clock control circuits enable a high speed clock (180 kHz) to clock the data through the word buffer and the (32,25) hamming decoder and into the data buffer.

High speed data processing starts the instant the data word is captured and will be completed before the next word starts loading (within 0.5 mS). The data buffer logic will be clocked one half clock cycle later than the word buffer logic to avoid race conditions. After the data buffer logic is loaded, the high speed clock will be disabled. When the strobe pulse is issued, the clock control circuits will be reset for the slow speed input data clock.

The hamming decoder syndrome generator logic is initialized while the word buffer is receiving the data word. The hamming decoder will then correct any single-bit errors and detect any double-bit errors as the data word is high speed processed. Single-bit errors are corrected using an exclusive OR. The hamming decoder circuit is implemented with the feed-forward equation: $G(X) = X^7 + X^6 + X^2 + 1$ and the feed-backward equation: $F(X) = X^6 + X^4 + X^3$. During the high speed data processing, the data input to the hamming decoder logic will be set to logic low. Refer to Figure 4.9.2-14.

The data buffer will be used to collect and hold a single-bit error corrected 32-bit word. The clock control circuits will disable the clock for the data buffer while the UP is receiving data into the word buffer. When a full 32-bit word is received, as indicated by the preset "1" of the word buffer, the data buffer will preset to 1000...0 and the interrupt flip-flop will be reset. The preset data buffer will enable a high speed clock to pipe the data word out of the word buffer, through the hamming decoder, and into the data buffer. This high speed clock will be disabled when the preset "1" has piped through to the end of the data buffer. This preset "1" therefore indicates that the 32-bit word is loaded and locked into position.

A Data Ready signal, derived from the preset "1", enables the CIC decode logic and address check logic to analyze the data. The data held in the data buffer will be inverted to compensate for the inverting buffer 189. In conclusion, data is held in the data buffer for at least 15.5 mS and data processing takes place in less than 0.5 mS.

The CIC decode logic identifies the CIC (CPU Interrupt Code) which determines how the data word is processed.

00 = unused 01 = CIU Command 10 = CPU Command 11 = Data Word

The CIC decode signals are passed to buffer 189 in the status word. The CIC bits also go to buffer 189. If the CIC decode logic indicates that the data is a CIU decoded command, the strobe pulse logic sends a CIU decoded command Strobe pulse signal.

The address check logic will be enabled when the data buffer is fully loaded. The address check logic compares the data word address to the connector selectable address patch. Each address patch is programmed in a patch plug connected to the J1 connectors of boards A5 and A8. Exclusive OR gates check each of the seven address bits. These seven bits and the Data Ready signal are passed into an AND gate structure to generate the Address OK signal. If the addresses match, the interrupt flip-flop are set by the strobe pulse logic.

Double-bit error detection and single-bit error correction signals are derived in the hamming decoder during the high speed data processing. These signals are stored in the error status flip-flops. These flip-flops get reset when the data buffer is preset and therefore indicate the error status of the word stored in the data buffer. The error status is presented in the status word of buffer 189. Detecting a double-bit error enables sync detector.

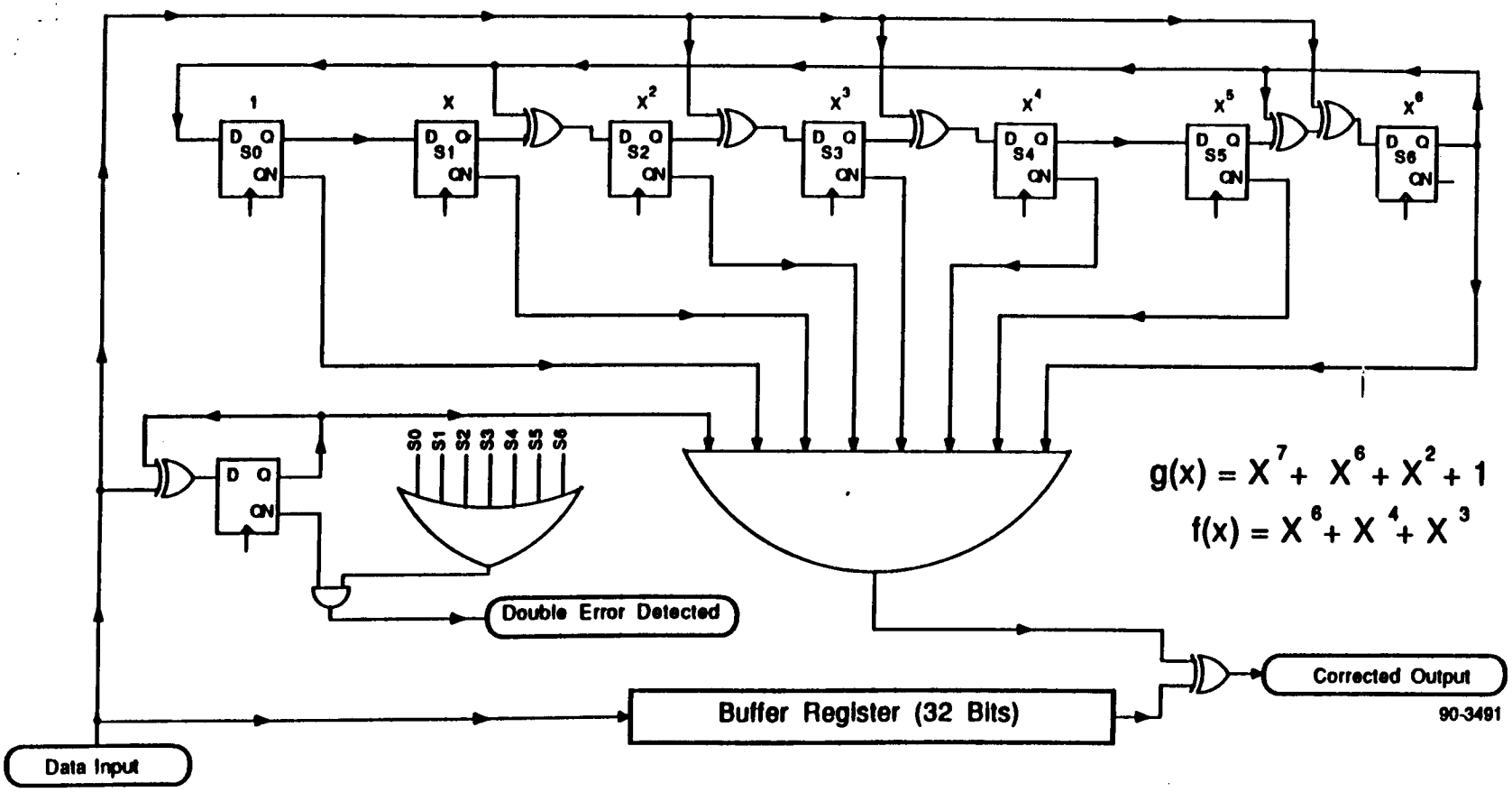

Figure 4.9.2-14. TIROS KLM Hamming Code Decoder (32,25) for the CIU Uplink Processor

The strobe pulse logic generates a 180 kHz logic pulse several clock cycles after the data buffer is loaded. This strobe pulse performs the following functions:

1) Preset the word buffer and hamming decoder
2) Reset the clock control circuits to the slow speed clock rate
3) Set the level-12 interrupt flip-flop of buffer 189 if the address is OK or the data contains a double-bit error
4) Strobe a CIU decoded command if the CIC code indicates that the data is a decoded command, the address matches, and the data does not contain a double-bit error.

4.9.2.2.2.2.5 Message Word Processing. The two CIC bits of a command word define the operation to be performed on the message word portion of the command word. When a single or multiple bit error occurs, an error message (one of the error status words) is transmitted to the CPU. All of the operations, except error-free unused CIC commands (OLS load data), will generate a CPU interrupt at level 12. This interrupt will be maintained until either:

a. The CPU performs an IPR data to the buffer with hex address 189, or

b. The next valid spacecraft address is decoded, and parity and CIC are received.

4.9.2.2.2.2.5.1 Status Word. An IPR status to hex address 189 is performed by the CPU whenever a level 12 interrupt is received or the level 16 POPS routine is initiated.

The CIU will respond to the IPR status at any time; the response is transfer of a 16 bit status word to the CPU. The format of the UP status word is shown in Figure 4.9.2-15. The CPU will examine the status word to determine the next sequence of events for the level 12 or 16 interrupt. Table 4.9.2-6 lists the status words which may result from an uplink command word.

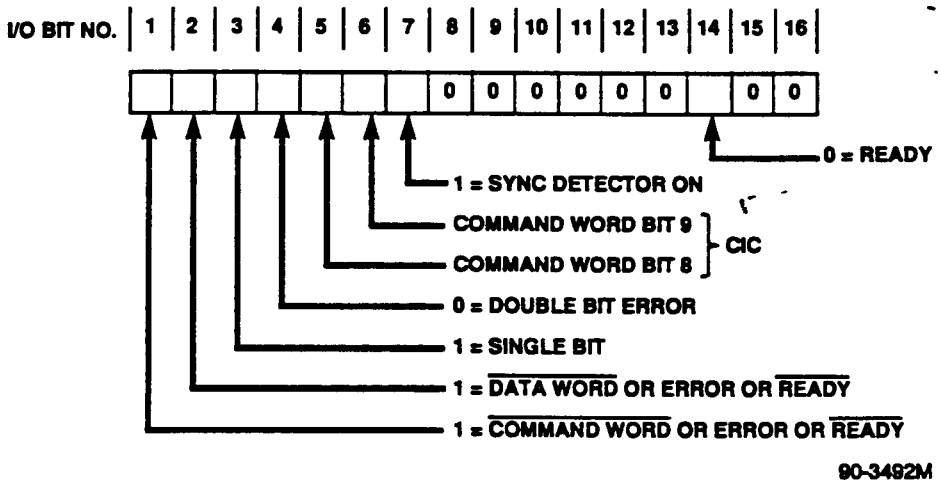

Figure 4.9.2-15. Uplink Processor Status Word Format

TABLE 4.9.2-6. UP PROCESSOR STATUS WORDS

State	I/O Bit No.															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Uplink Processor Not Ready	1	1	X	X	X	X	X	X	X	X	0	0	0	1	0	0
CPU Command Word Ready and No Errors	0	1	0	1	1	0	X	X	X	X	0	0	0	0	0	0
CPU Data Word Ready and No Errors	1	0	0	1	1	1	X	X	X	X	0	0	0	0	0	0
CIU Decoded Command Ready and No Errors	1	1	0	1	0	1	X	X	X	X	0	0	0	0	0	0
Word Ready, Single Bit Error	1	1	1	1	X	X	X	X	X	X	0	0	0	0	0	0
Word Ready, Multiple Bit Errors	1	1	1	0	X	X	X	X	X	X	0	0	0	0	0	0
X = Don't care																

4.9.2.2.2.2.5.2 CPU Commands. Any error-free command word with a CIC code of 10 (bits 8, 9) contains a real time CPU command in the message word. After verification, the UP will generate a level 12 interrupt and, in response to IPR status, generate the status word for "CPU Command Word Ready and no Errors".

The presence of a logic 0 in bit 14 of the status word indicates to the CPU that an IPR data operation is required. When the IPR data to hex address 189 is executed by the CPU, the UP will transfer the 16 bit message word to the CPU, then reset to the "not ready" state and remove the level 12 interrupt. Any subsequent IPR status requests would result in the "Uplink Data Word Not Ready" status word.

4.9.2.2.2.2.5.3 CPU Data Words. Any error-free command word with a CIC code of 11 contains CPU data in the message word. The UP operates in the same manner on the CPU data words as on the CPU commands except the "CPU Data Word Ready and No Errors" status word will be transferred to the CPU. The CPU detects this status word by the presence of a logic 0 in bit 2.

4.9.2.2.2.2.5.4 Unused CIC. Any error-free command word with a CIC code of 00 is an unused command word. This CIC code will not produce a level 12 interrupt to the CPU and no further processing of this command will be performed.

4.9.2.2.2.2.6 CIU Decoded Commands. Table 4.9.2-7 contains the list of CIU decoded commands. All CIU decoded commands can only be uplinked and executed in the hardware. Each CIU decoded command must be followed by a CIU execute command; thus, it takes two uplink messages before a CIU decoded command is carried out. The use of the execute command permits the ground to verify through telemetry that the proper CIU decoded command was received by the spacecraft. If the next uplink word after the receipt of a CIU decoded command is not execute, then the previously received message is erased.

All CIU decoded commands are real-time commands only; they cannot be executed via storage in and retrieval from the stored command table in the CPU.

TABLE 4.9.2-7. CIU DECODED COMMANDS

Command Function	Spacecraft Address		CPU Affected	
	UP-1	UP-2	CPU1	CPU2
Execute	X	X	X	X
Clock 1 Select	X	X	X	X
Clock 2 Select	X	X	X	X
CPU1 Select	X	X	X	X
CPU2 Select	X	X	X	X
Bus A Select	X	X	X	X
Bus B Select	X	X	X	X
CPU1 Memory Normal	X		X	
CPU1 Memory Swap	X		X	
CPU2 Memory Normal		X		X
CPU2 Memory Swap		X		X
CPU1 ON		X	X	
CPU1 OFF		X	X	
CPU2 ON	X			X
CPU2 OFF	X			X
RXO Primary Select	X	X	X	X
RXO Backup Select	X	X	X	X

4.9.2.2.2.2.7 Uplink Processor Operation. Figure 4.9.2-16 is a simplified schematic of the CIU command decoder. This figure shows the commands and the associated cross strapping. The UP-1 commands are decoded in a CD4028 BCD to decimal decoder and the decoded signals are then strobed out of an intermediate latch into a 2-input OR gate which cross straps the side 1 and side 2 commands through isolation buffers. These UP-1 commands are then OR'd with the single action CPU commands where the signal is latched, pulse stretched, and level shifted before it is transmitted to the external unit. The Power-On-Reset (PORS) sets each of the external units to the inactive state at initial turn on.

The uplink processor utilizes the 360 kHz clock signal from the phase locked loop oscillator circuit on the timing board. Use of this oscillator output will enable processing of the CIU decoded level commands with the absence of the RXO 5.12 MHz clock. In particular the CIU decoded command for RXO oscillator selection can be processed and executed by the uplink processor even in the absence of the 5.12 MHz RXO clock.

4.9.2.2.2.3 Clock and Timing Generation. The clock and timing generation logic comprises two separate but identical clock divider/time code counter chains and a clock selector. Each timing chain utilizes the 5.12 MHz input from the RXO to generate a full complement of clock and timing signals; the clock selector allows the use of either chain as the primary spacecraft timing source.

4.9.2.2.2.3.1 Clock Dividers. Each clock divider generates the outputs listed in Table 4.9.2-8; the divider logic is shown functionally in Figure 4.9.2-17. The 360 kHz output is not an integral submultiple of 5.12 MHz and therefore requires a frequency multiplication (X9) in its synthesis. This is provided by a phase locked oscillator circuit using a CD4046B Phase Locked Loop IC and a divide by 9 counter in the feedback path. The other output frequencies are generated by direct digital countdown from the 5.12 MHz input.

The 2.56 MHz IMU Clocks and the 1.706667 MHz CPU Clocks are provided separately (redundantly) from the 2 clock dividers. Other clocks are each gated in the clock select logic for output from redundant interfaces.

The clock dividers and time code counters also supply 1024 Hz, 32 Hz, 2 Hz, 1 Hz, 1/2 Hz, and 102.4 kHz for timing and synchronization within the CIU. The 102.4 kHz is used for data transfer clocking in the modular serial output and serial input data I/O buffers. It is generated by both clock dividers, and gated to the buffers via the I/O bus control logic.

4.9.2.2.2.3.2 Time Code Counters (TCC). Each time code counter is a 16 bit binary counter with an input clock frequency of 32 Hz. The contents of each time code counter are continuously available to the associated CPU as a 16 bit real time clock reference.

The time code counters are synchronized to each other and to the IMU 10 Hertz signals, depending on the state of the Select Clock 1 signal from the uplink processor as summarized in Table 4.9.2-9. The selected time code counter is synchronized to a 2 Hz signal derived by dividing the 10 Hz IMU Sync signal by 5, and the other counter is synchronized to the 2 Hz output of the selected counter.

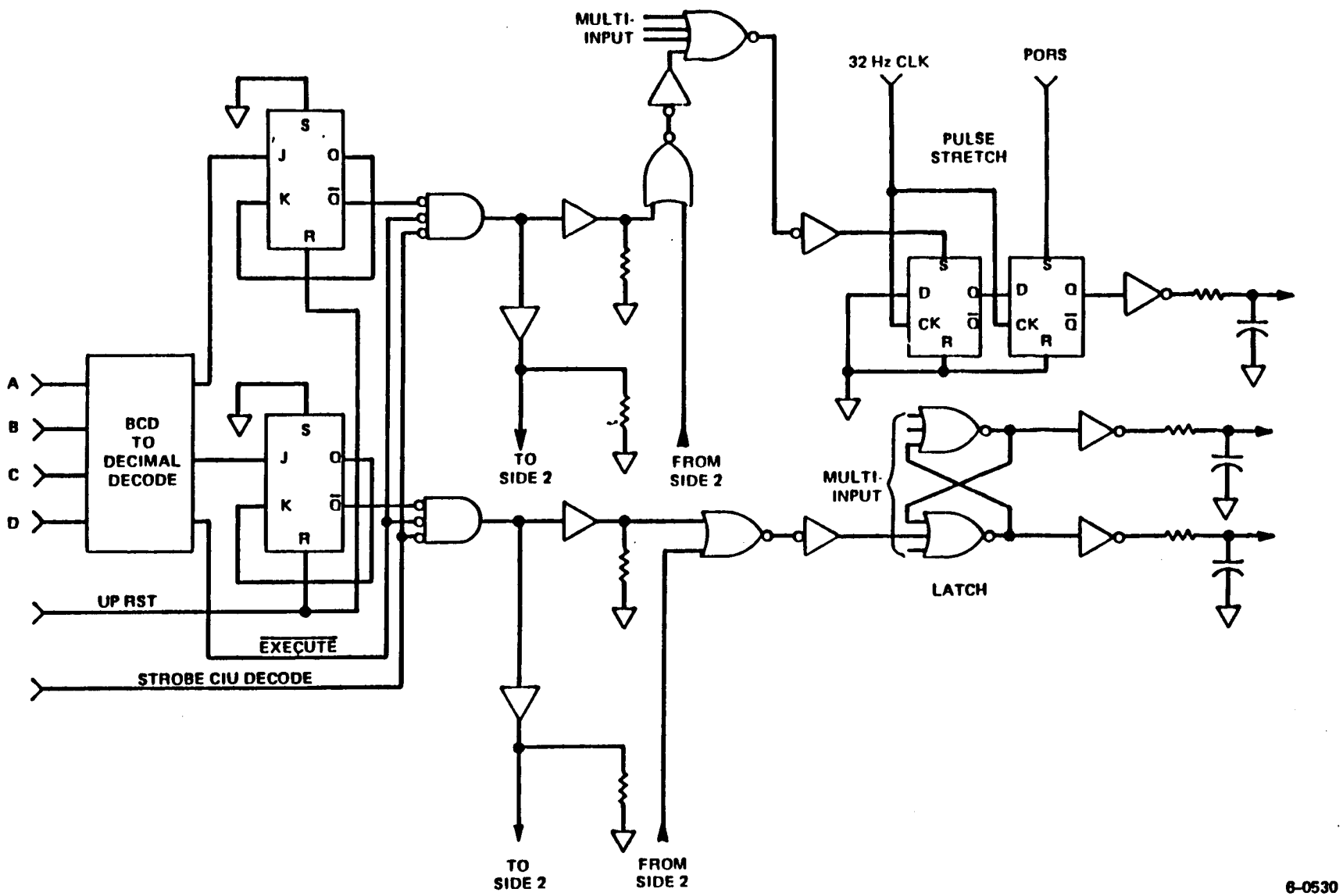

Figure 4.9.2-16. CIU Decoded Command Circuit

TABLE 4.9.2-8. CLOCK DIVIDER OUTPUTS

Output Designation	Frequency
IMU Clock	2.56 MHz
CPU Clock	1.706667 MHz
XSU Clock	1.024 MHz
*TMU Clock	1.024 MHz
*CXU Clock	1.024 kHz
*SSE Clock	640 kHz
*TIP Clock	360 kHz
*SAD Clock	102.4 kHz
*PSE Clock	2 Hz
*ESA Sync	2 Hz
*TIP Sync	1 Hz
*AIP Sync	1 Hz
*Subjected to clock selection function	

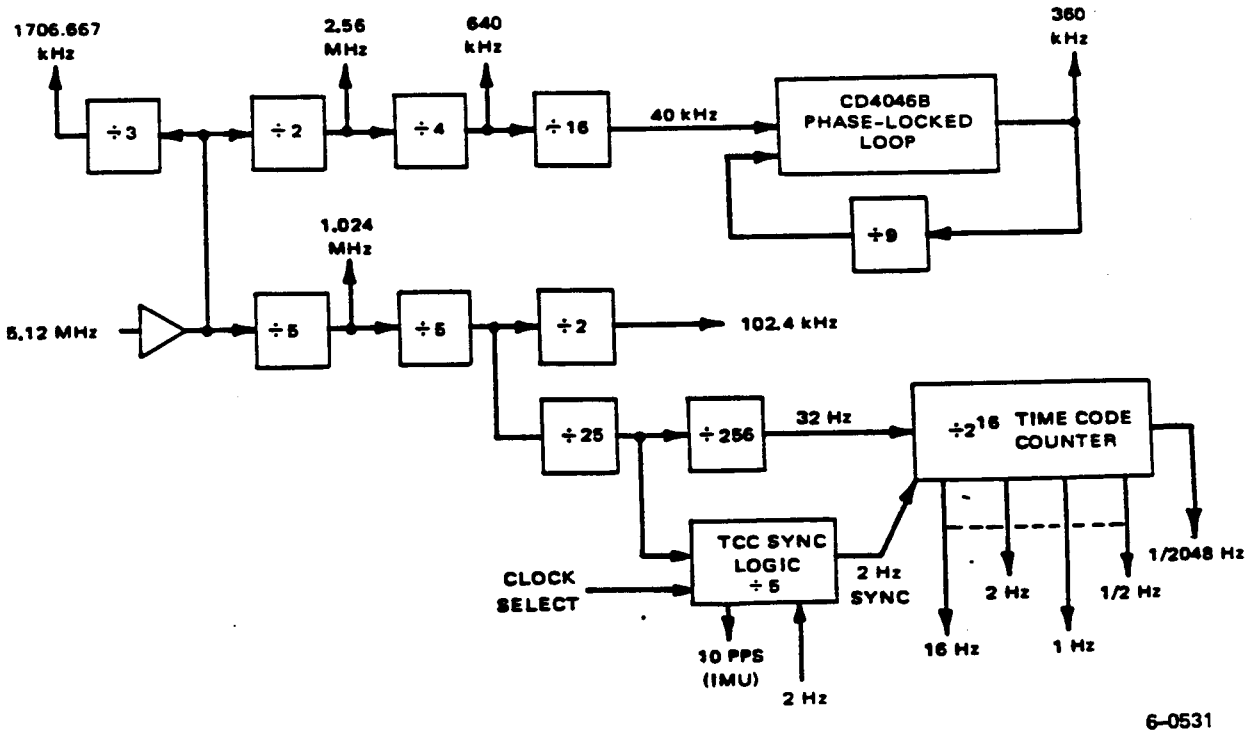

Figure 4.9.2-17. Clock Divider/Time Code Counter Block Diagram

TABLE 4.9.2-9. TIME CODE COUNTER SYNCHRONIZATION

Select Clock 1	TCC1 Sync From	TCC2 Sync From	
0	2 Hz-2	IMU 10 Hz After ÷ 5 Counter	
1	IMU 10 Hz After ÷ 5 Counter	2 Hz-1	←Spacecraft Power On Reset

A 2 Hz signal derived from the time code counter is gated to the level 9 interrupt of the non-control CPU in Boost mode and OR'd with the IMU Data Ready signal to the level 9 interrupt of both CPU's in Orbit mode. This 2 Hz signal pro- vides a backup initiation of the CPU processing cycles in the event of an IMU interface failure.

The time code counter provides a 2 Hz Flag signal to the CPU flag input buffers to allow software identification of the 10 Hz level 9 interrupt which coincides with the 2 Hz sync signal; the 2 Hz Flag is true for 62.5 milliseconds following each 2 Hz sync signal.

The 2 Hz Flag of TCC1 is input to CPU1's flag buffer and the flag of TCC2 is input to CPU2's flag buffer. These result in a data one in the flag bit if an IPR occurs while the flag is true.

The divide by 5 counters receive a 10 Hz Sync signal from the IMU in all combinations of CIU and IMU modes. When Clock 1 is selected, the output of the divide by 5 is used to trigger both negative edge-triggered pulse generators. This assures that both divider chains are reset simultaneously every 2 Hz.

Furthermore, the slave clock's negative edge triggered pulse generator is used to keep this divide by 5 counter in synchronism with the divide by 5 counter of the master clock. This prevents timing glitches when the clock select is changed by the user.

Rephasings will occur as a result of IMU switchovers, but each CPU will find its 2 Hz Flag whenever it is interrupted by its 2 Hz backup interrupt. Furthermore, since the rephasing will take place simultaneously, both CPU's will perceive things in the same way at the same time.

4.9.2.2.2.4 <u>CPU Interface Control</u>. The communicative interface between each CPU and the CIU comprises a bi-directional data transfer trunk and a uni-directional interrupt request trunk (CIU outputs); these 2 trunks are generically referred to herein as an "I/O bus". Because of the critical speed and timing requirements of these interfaces, the CIU contains special logic to buffer and re-clock all signals to assure reliable operation.

4.9.2.2.2.4.1 Data Trunk Buffers. The CIU transfers data to and from CPU1 via its I/O interface, designated I/O-1, and similarly transfers data to and from CPU2 via I/O-2. Each of these interfaces comprise a 16-line bi-directional I/O data and address trunk together with five control and clock signals.

A block diagram of the data trunk buffer and control logic is shown in Figure 4.9.2-18. As shown, each data trunk buffer comprises line switches (transmission gates), two parallel registers for data and address storage, and control logic required to transfer data bi-directionally between the CPU I/O interface and the BIO interface, which connects to the remainder of the CIU. The timing of trunk buffer operations is shown in Figure 4.9.2-19 for an IPR operation (data transfer from the CIU to the CPU), and in Figure 4.9.2-20 for an OPR operation (data transfer from the CPU to the CIU). CPU timing for these operations is discussed in Section 4.9.2.2.2.6.

IPR operations are controlled by a sequencer clocked by the CPU phase 1 clock. The two sequencer flip-flops are designated Q1 and Q2, and are "weighted" 1 and 2, respectively, in defining the four sequencer states. The standby condition of the sequencer is state 0. Presence of a high level on the I/O Alert line from the CPU at the time of phase 1 clock (negative edge) advances the sequencer to state 1. The next three negative edges of phase 1 clock successively step the sequencer to states 3, 2, and 0, respectively.

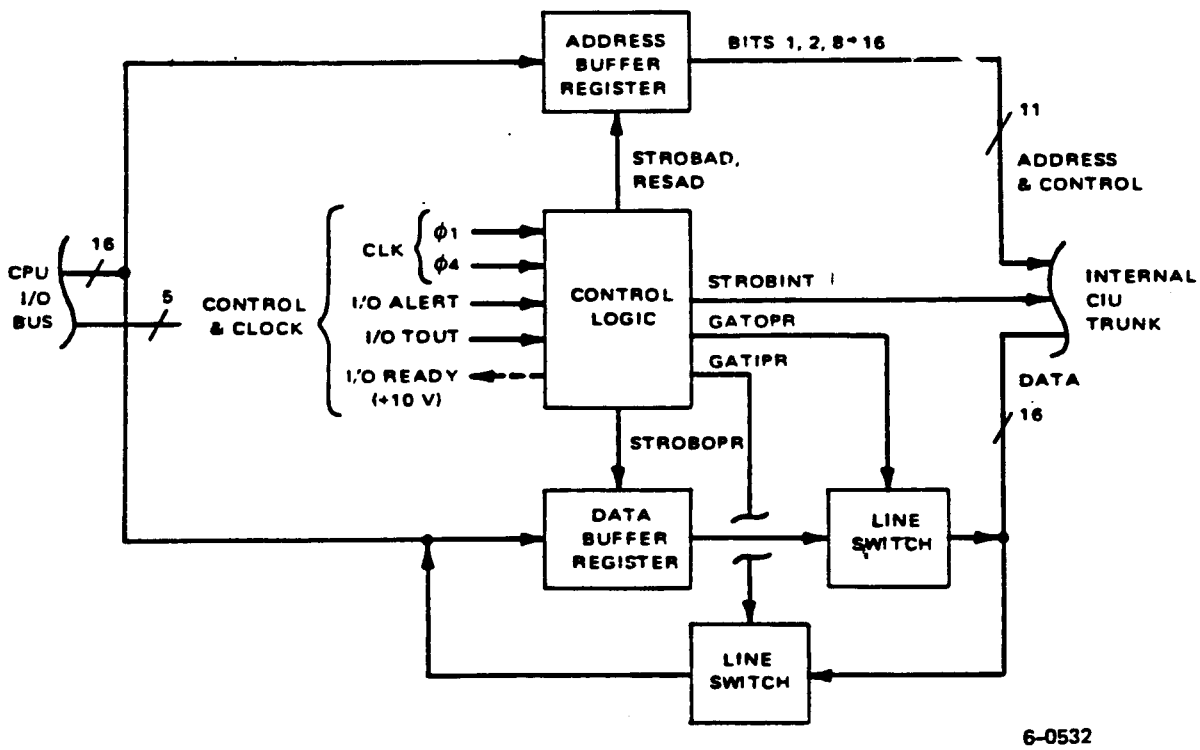

Figure 4.9.2-18. Data Trunk Buffer Block Diagram

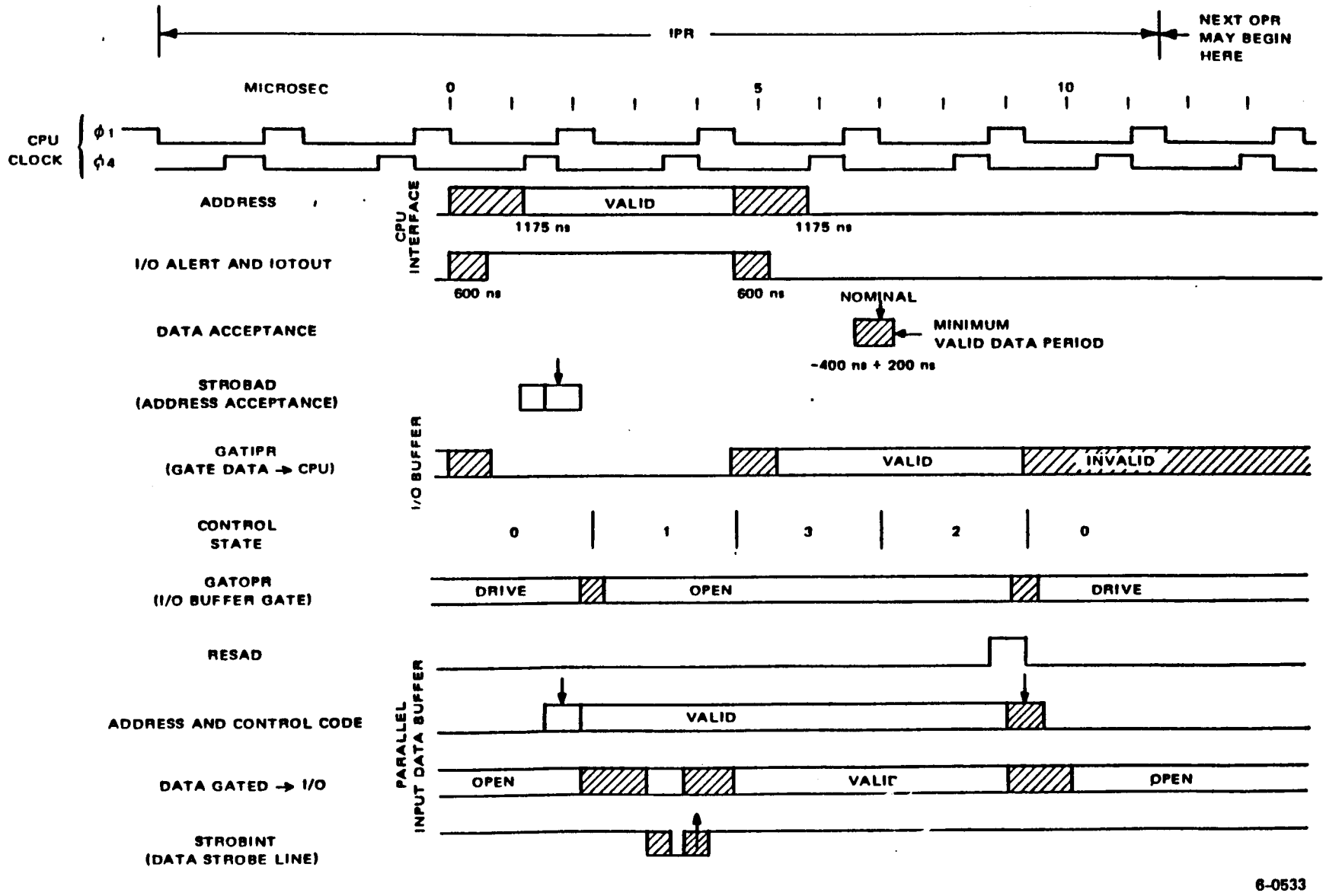

Figure 4.9.2-19. CIU Timing, IPR Data (To CPU)

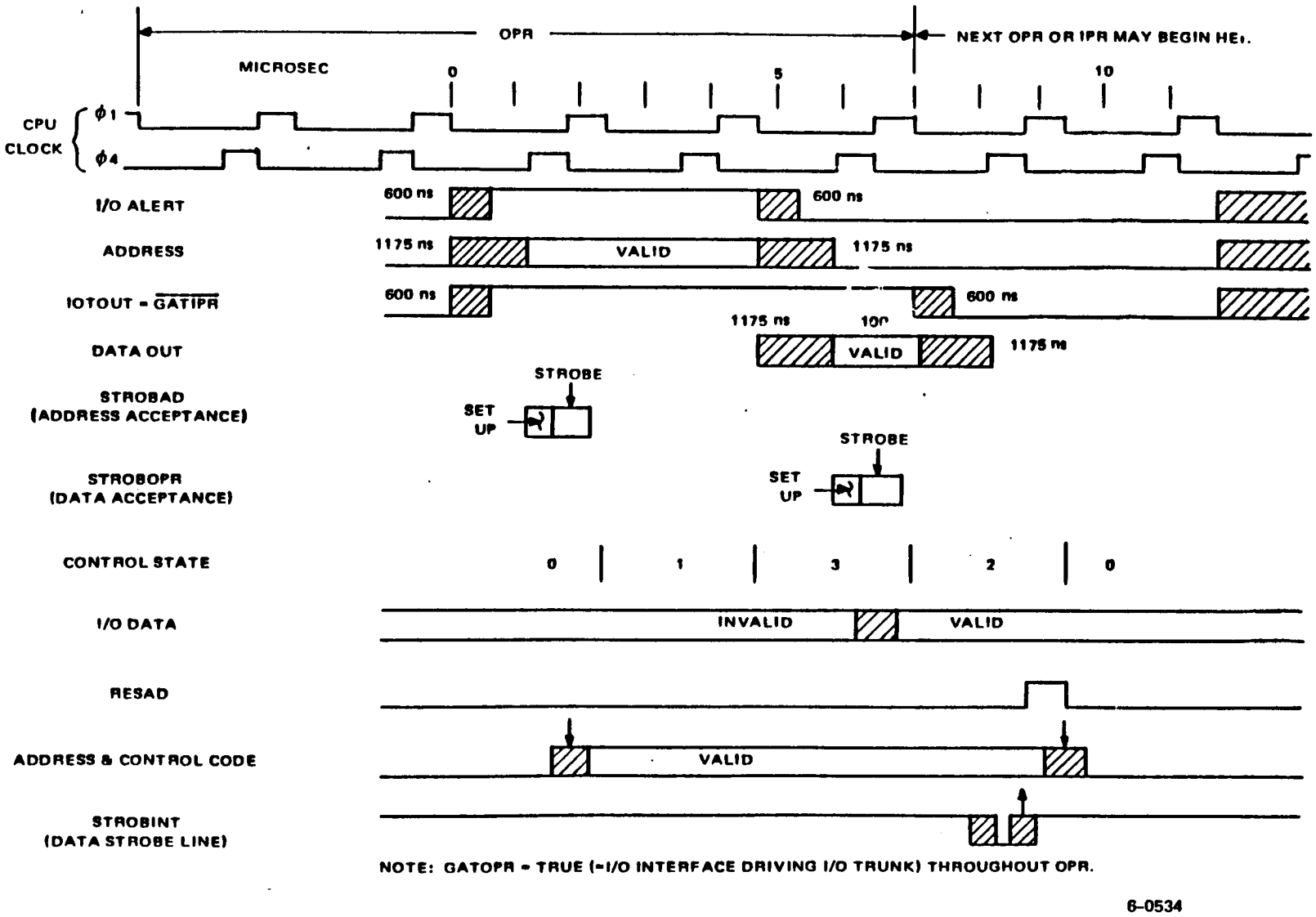

Figure 4.9.2-20. CIU Timing, OPR Data (From CPU)

The presence of I/O Alert in sequencer state 0 gates the next phase 4 clock (trailing edge) to strobe an address word from the CPU I/O interface into an address buffer register. The address buffer register is reset at the trailing edge of the next phase 1 clock, which terminates sequencer state 2.

The address buffer register contains a 4 bit control code A1-A4 (hex digit 1) and a 12 bit address code A5-A16 (hex digits 2, 3, and 4). Bits 3 and 4 of hexadecimal digit 1 are not used by CIU, these bits are reserved for software operations. The significance of these address bits is shown in Table 4.9.2-10. Address bits A5-A8 (hex digit 2) are used by the buffer control logic as follows. If A5, A6, A7, and A8 are all zeros, the STROBINT pulse is inhibited because address words containing all zeros in these bits (hex addresses X0XX) are reserved for CPU software ground test operations. Address bit A8 is used by the cross strap gating logic (see Paragraph 4.9.2.2.2.5.2) to determine whether the addressed data buffer is "local" (interfaced with the BIO bus) or "not local" (interfaced with the I/O-A or I/O-B bus, via the cross strap logic).

Address buffer register bits A1, A2, A5 and A8 through A16 are provided to the CIU internal buses.

The presence of three "ones" in bits A5 and A8 through A16 constitute a valid buffer address in the CIU. The CIU contains an invalid address detector to prevent any address containing more than 3 "ones" from being clocked into the address register. A functional block diagram of the detector is shown in Figure 4.9.2-21. The detector uses select speed CD4008 4 bit binary adders to sum the number of "ones" contained in the address and if an invalid address is detected, holds the address register reset during the attempt to clock the address into the register.

At the first phase 4 clock in sequencer state 1, a data strobe pulse (STROBINT) is output via the internal CIU buses to the data buffers. Following STROBINT, the addressed buffer will place data or a status word on the data lines D1-D16 as requested by address bits A1 and A2 (the control code).

At approximately the beginning of sequencer state 3 the CPU will terminate the high level on the I/O Transfer Out (IOTOUT) interface line. This will cause the I/O buffer to gate the data or status code (strobed from the internal bus) to the CPU I/O interface.

During an IPR Status operation with a standard serial buffer, the buffer places status code data on 4 internal trunk lines but leaves the other lines open-circuited. The buffer control "jams" zeros on the remaining lines by disabling the cross strap data selection gates for these unused data lines, so that no ambiguous or "floating" data lines appear at the I/O interface. For a standard serial I/O buffer, zeros are jammed on data lines 1 through 12; for the unique IMU data buffers, however, the status code appears on lines 1 through 4. The buffer control accommodates this special condition by decoding address $BXX3_{16}$, which identifies IPR Status from the IMU buffers, and jams zeros on data lines 5 through 16 when it is detected.

TABLE 4.9.2-10. I/O ADDRESS WORD FORMAT AND MODE CONTROL

Hexadecimal Digit 1	I/O Address Word Bit No. 1 2 3 4	Input/Output Mode Output Buffer (CPU to External)	(Buffer Operation) Input Buffer (External to CPU)
3	0 0 1 1	Output buffer (OPR) reset	Input (IPR) Data (Not Last Word)
B	1 0 1 1	Input (IPR) Status	Input (IPR) Status
F	1 1 1 1	Output (OPR) Data (Not Last Word)	Output (OPR) "Begin"
7	0 1 1 1	Output (OPR) Data (Last Word, or Single Word)	Input (IPR) Data (Last Word)

Hexadecimal Digit ?	Bit No. 5 6 7 8	Type of Buffer	Buffer Interface
1	x 0 0 1	Parallel	BIO1 or BIO2 Bus (Local)
2	0 0 1 0	Parallel	I/O-A or I/O-B Bus
A	1 0 1 0	Parallel	(Not Local)
4	0 1 0 0	Serial	I/O-A or I/O-B Bus
C	1 1 0 0	Serial	(Not Local)
0	0 0 0 0	Reserved for software debugging: CIU must ignore	

Hexadecimal Digits 3, 4	Bit Number 5 9 10 11 12 13 14 15 16	Address Format and Significance
xx	x x x x x x x x x	Must include 3 ones and 6 zeroes
x3	x x x x x 0 0 1 1	IMU Data Buffer - Status Code is gated via data lines 1-4, not 13-16
x8	x x x x x 1 x x 0	Special output status and control buffer
x9	x x x x x 1 x x 1	CRD Data Buffer (and several input status parallel buffers) Status Code gated via 16 data lines
xx (Even)	x x x x x x x x 0	Output Buffer (CIU to External Data Transfer)
xx (Odd)	x x x x x x x x 1	Input Buffer (External to CIU Data Transfer

For another special case, the uplink processor data buffers, the status code appears on all 16 data lines. The buffer control accommodates this case by decoding a "one" in address bit 13, and inhibiting the "jam zeros" logic when it is detected. (Several buffer addresses besides that of the uplink processor buffer have a "one" in bit 13, but they are all parallel buffers, for which the IPR Status operation is irrelevant.)

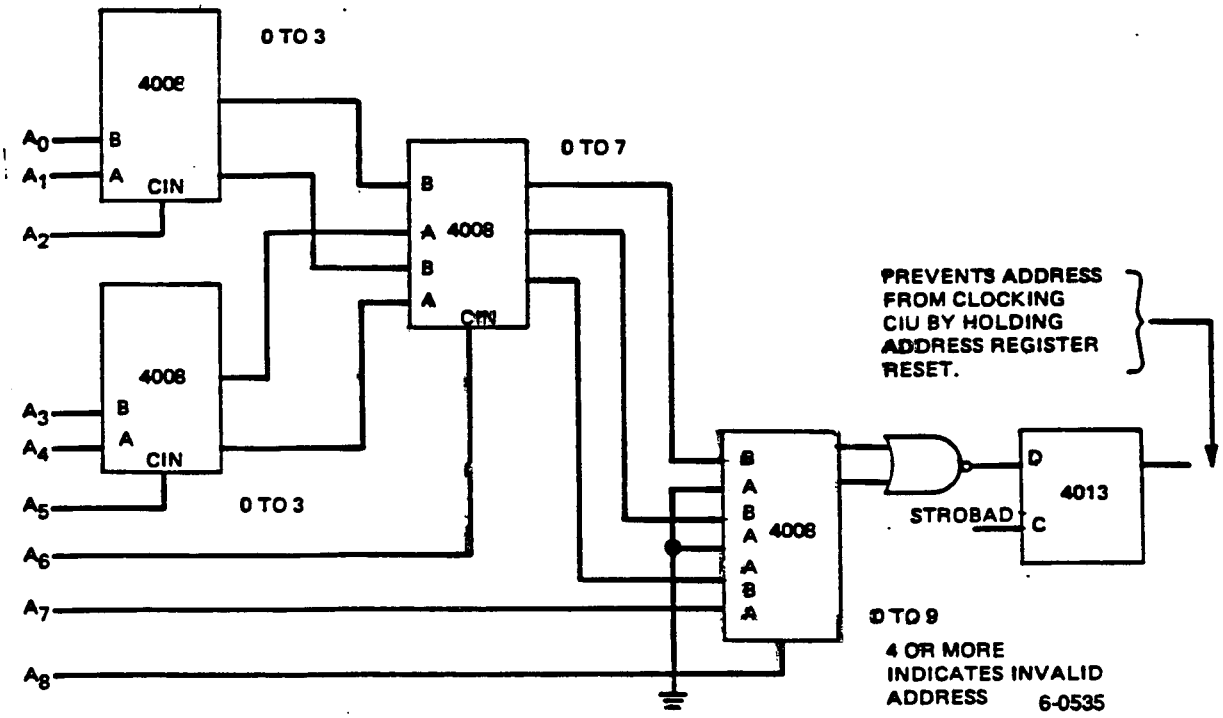

Figure 4.9.2-21. Invalid Address Detector Functional Diagram

Referring to Figure 4.3.2-20, buffer operation during states 0 and 1 of an OPR operation is as follows. The initiation, clocking, and state sequence of the sequencer flip-flops, and the strobing (and subsequent resetting) of an address word into the address buffer register are the same as for an IPR operation (Figure 4.3.2-19).

At the trailing edge of the first phase 4 clock pulse during sequencer state 3, data at the CPU I/O interface is strobed into a data register in the trunk buffer. The data is then gated out to the appropriate internal destination according to the cross strap control logic and the Local/Not Local information decoded from address bit 8.

At the first phase 4 clock in sequencer state 2, the CIU internal data strobe pulse (STROBINT) is output via the appropriate internal bus to the I/O buffers. This pulse strobes data into the addressed buffer.

4.9.2.2.2.4.2 Interrupt Controllers. In order to assure that each CPU responds once and only once to valid interrupts from all of its data interfaces, a centralized interrupt controller is provided for each CPU interface. The interrupt controller stores up to 1 interrupt at each valid priority level and outputs a "buffered interrupt" signal to the CPU, on the appropriate line, for each active level. The buffered interrupt for each level is maintained until acknowledged by the CPU via an IPR or OPR to the I/O buffer assigned to that level; this assures service to buffers which generate short-duration pulse interrupts and/or those to which the CPU response is delayed by higher

level processing. The interrupt controller also insures that a new buffered interrupt is not generated unless the corresponding interrupt is terminated and re-activated after being acknowledged; this assures that a CPU is not hounded by a confused or failed data buffer. Each interrupt controller comprises 6 separate interrupt sequencers; each interrupt sequencer provides control for one buffered interrupt as described above. The logic and state diagram for each interrupt sequencer is shown in Figure 4.9.2-22.

With the sequencer in state 0, a high level (true) on the Input Interrupt (INT) line sets FAn at the next 1.024 MHz clock negative edge and places a high level (true) on the output Buffered Interrupt (BINT) line; the INT line may go low (false) at any time after FAn has been set.

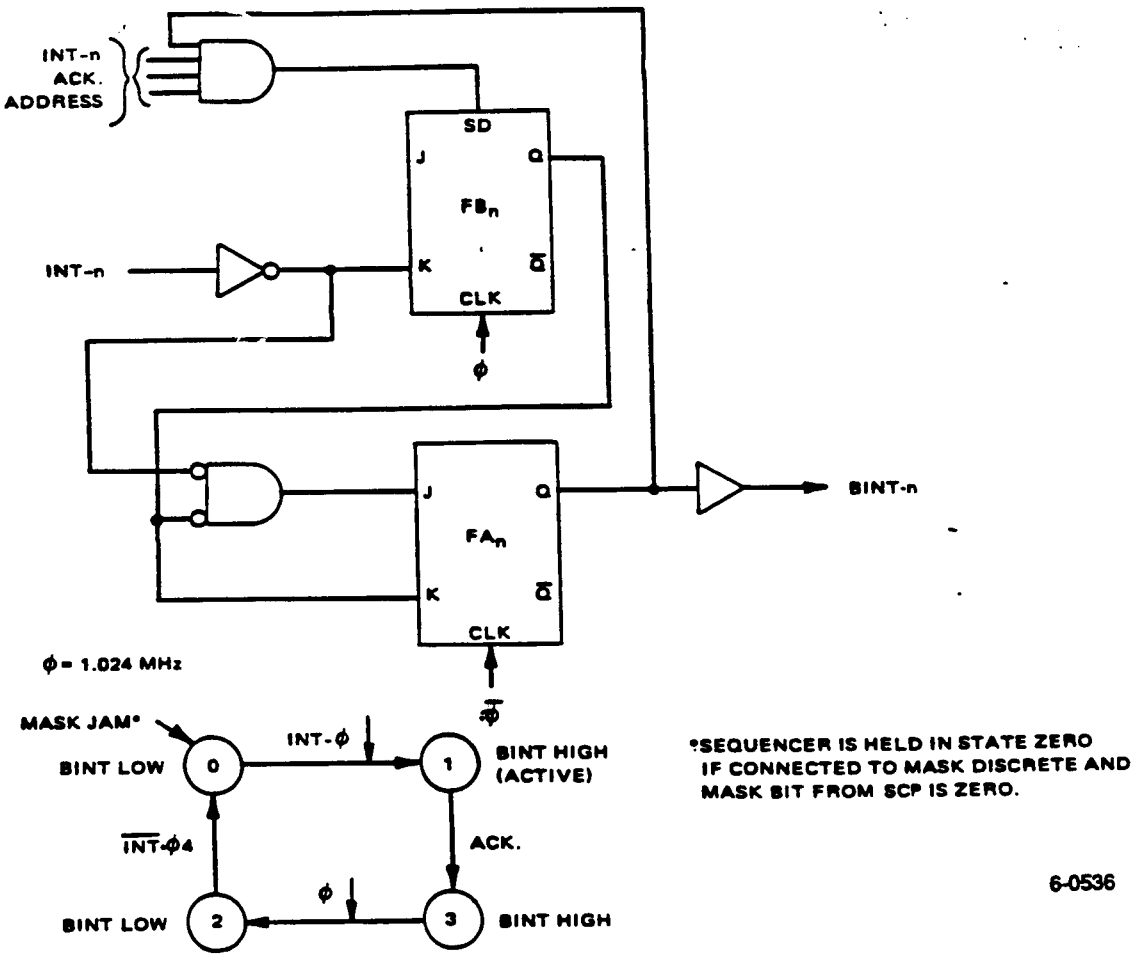

Figure 4.9.2-22. Interrupt Sequencer Logic and State Diagram

When the CPU responds to the BINT signal, the software will cause an OPR or IPR operation using a designated "acknowledge" (ACK) address as indicated in Table 4.9.2-11. This address is decoded by the controller as a pulse, approximately 7.6 microseconds in duration. FBn is set at the leading edge of this ACK address pulse (if the controller is in state 1). At the first 1.024 MHz clock negative edge after FBn is set (state 3), FAn is reset, placing the controller in state 2. The controller remains in state 2 until the first clock positive edge following the trailing edge of ACK address pulse or when the INT line goes high, whichever occurs later. This clock edge resets FBn, returning the controller to state 0.

The functional assignment of interrupting signals to the interrupt controller is given in Table 4.9.2-11. The interrupting signals for level 12 are specially generated and buffered by the uplink processor. The UP outputs a level 12 interrupt signal when the uplink data buffer is full. The other interrupts are each buffered by a standard sequencer in the interrupt controller.

The interrupt sequencers for levels 11, 10, 8, 7, and Y may be separately enabled or disabled by software in the associated CPU; each of the Interrupt Mask discretes is connected to the Direct Reset inputs of FAn and FBn of each maskable interrupt. A "zero" mask bit jams the sequencer in state 0, inhibiting, or "masking", that interrupt.

4.9.2.2.2.5 I/O Bus Control. The I/O bus control logic provides hardware and software interactive control of CPU and CIU redundancy; it includes CPU select logic and cross-strap steering logic.

The CPU select logic provides the capability to select either CPU to control I/O bus switching from software. It also provides continuous checks on the functional status of each CPU and, should one CPU fail to satisfy status checks, automatically selects the functional CPU regardless of previous commands. Bus switching discretes controlled by the selected CPU are gated onto the bus cross-strap lines.

TABLE 4.9.2-11. INTERRUPT ASSIGNMENTS

CIU Interrupt Input	Assigned Function	Maskable	ACK Address (HEX)
12	Uplink CPU Data	No	189
11	CPU Boost Telemetry	Yes	432
10	CPU Memory Dump	Yes	432
9	IMU Data	No	483
8	ESA Data	Yes	425
7	TIP Data	Yes	407
Y	Unassigned	Yes	-

The cross-strap steering logic is simply a multitude of and-or-select gates, transmission gates, and line drivers which interconnect the selected CPU with the I/O bus (A or B) of its choice and the non-selected CPU with the other I/O bus.

4.9.2.2.2.5.1 CPU Select Logic. The CPU select logic is shown functionally in Figure 4.9.2-23. CPU1 and CPU2 both attempt to control the CIU cross state. Each CPU outputs a control discrete designated MOB-1 (or MOB-2). The MOB discrete set to 1 signifies, "This CPU requests that the cross strap gating connect this CPU with the I/O-B bus" and vice-versa.

At any given time, only one of the two CPUs is selected to generate the Cross (cross strap select) control discretes. The selected CPU is defined by the level of a discrete signal designated Control, which is high when CPU1 is selected. Normally CPU1 may be selected by a Select CPU1 command decoded by either of the CIU uplink processor sections; similarly, CPU2 may be selected by a Select CPU2 command. Both CPU's are, however, continually monitored by the CPU select logic. Each CPU is assumed to be "OK" if it performs an OPR operation to address 168 (hexadecimal) at least once per 1.5 seconds. If CPU1 fails to perform the MEOK OPR operation for a period during which the CIU logic counts four successive 2 Hz pulses, the monitor logic switches to a CPU1 NOT OK state, which may be subsequently returned to the CPU1 OK state only by a Select CPU1 command pulse or a Select CPU2 command pulse decoded by either uplink processor. Identical logic determines CPU2 OK/CPU2 Not OK states.

When the logic is in the CPU1 OK/CPU2 OK state, or in the CPU1 Not OK/CPU2 NOT OK state, control is determined solely by the CIU decoded CPU Select commands.

When the logic is in the CPU1 OK/CPU2 Not OK state, CPU1 is automatically selected regardless of the commanded CPU selection. Similarly, when the CIU logic is in the CPU1 Not OK/CPU2 OK state, CPU2 is automatically selected.

If CPU1 is selected, Control is high and Cross is true (CPU1 on I/O-B) when the MOB-1 discrete is set to 1, and Cross NOT is true when that bit is set to 0.

If CPU2 is selected, Control is low and Cross NOT is true (CPU2 on I/O-B) when the MOB-2 discrete is set to 1, and Cross is true when that bit is set to 0.

Several other control signals used within the CIU are similarly determined in accordance with level discretes set (by software) by the selected CPU. If CPU1 is selected, the discrete is derived from a bit in CPU 1's buffer and if CPU2 is selected, the discrete is derived from a bit in CPU 2's buffer. Veto Bus Selection, which allows the control CPU to override ground selection of the bus, is one such signal.

4.9.2.2.2.5.2 Cross Strap Steering. A functional schematic diagram of the data/interrupt cross strap steering logic is shown in Figure 4.9.2-24. As shown, the CPU I/O bus is connected to either its associated BIO bus, I/O-A, or I/O-B each time an IPR or OPR operation is performed. The status of the Local bit in the I/O operation control code and its logical inverse determine whether the CPU is connected to its BIO bus (Local) or to I/O-A/B (Local Not). If the control bit is Local Not, the status of the Cross/Cross Not signals from the CPU select logic is used to connect the CPU with either I/O-A or I/O-B. The possible CPU-CIU I/O interconnects are summarized in Table 4.9.2-12.

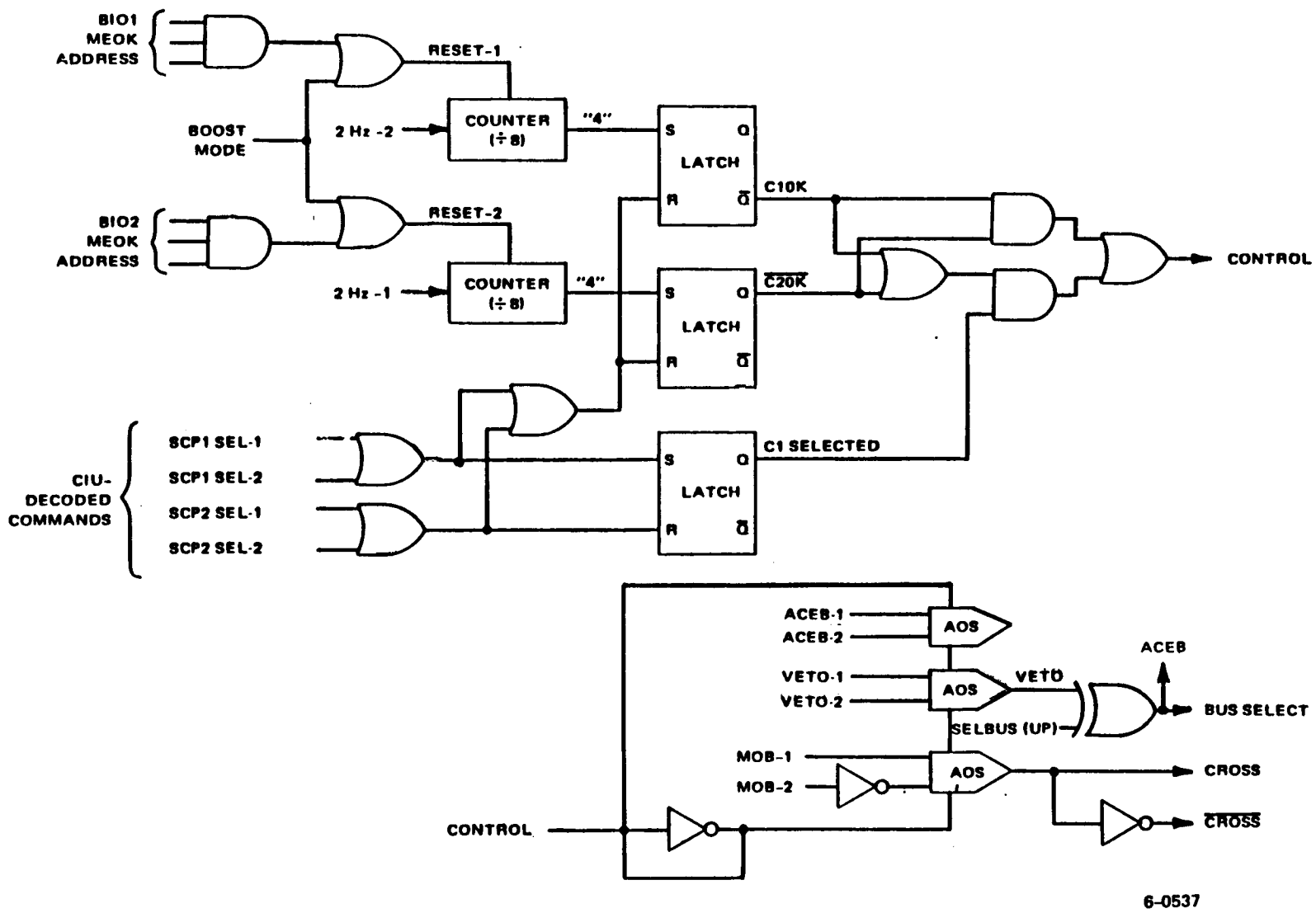

Figure 4.9.2-23. Simplified CPU Select and Bus Switch Logic

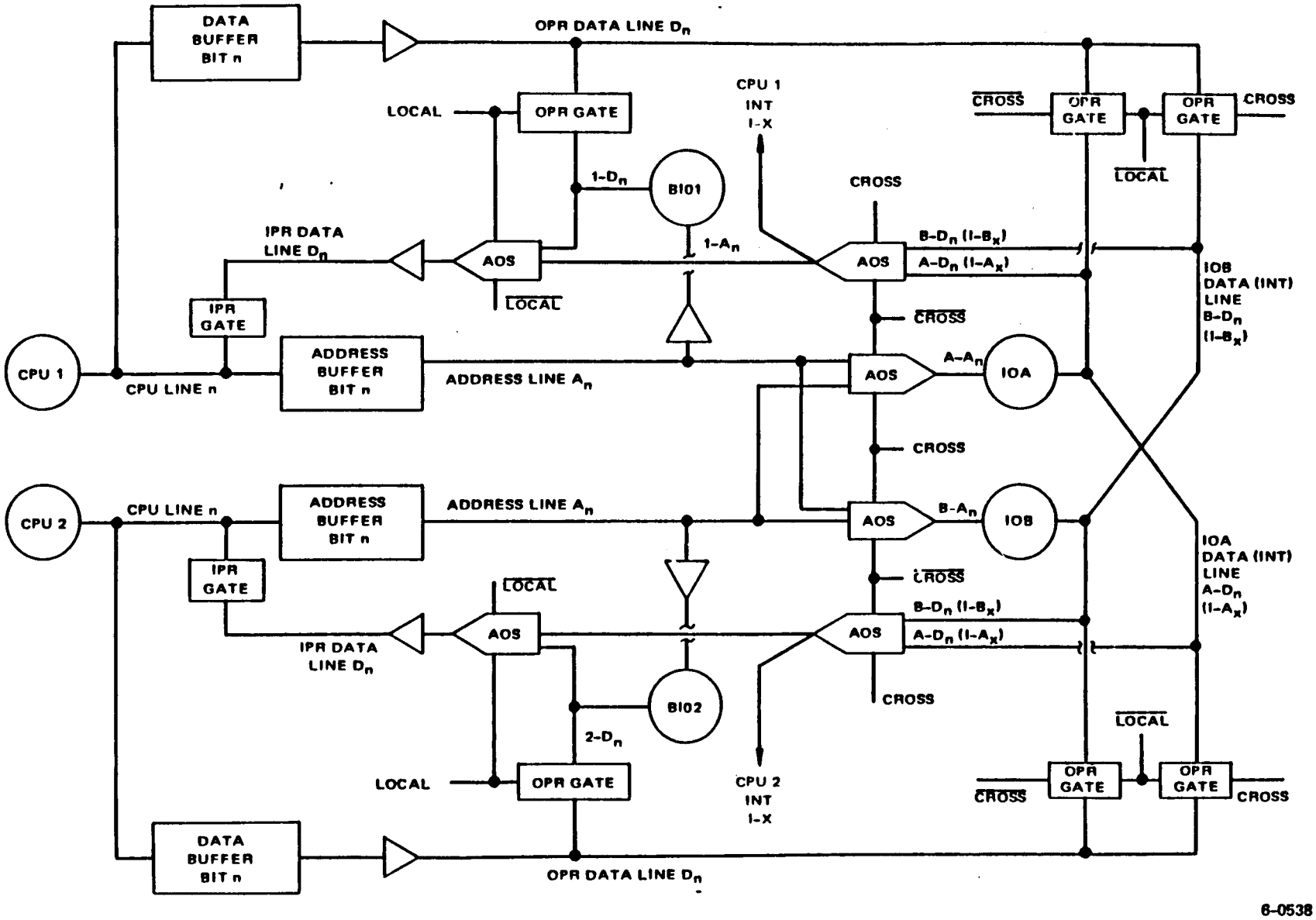

Figure 4.9.2-24. Data/Interrupt Steering Logic Functional Schematic

TABLE 4.9.2-12. DATA/INTERRUPT CROSS STRAP STEERING SUMMARY

CPU1 Power Status	I/O Address (CPU1)	Cross State	I/O Operation (CPU1)	Gate Data From CPU1 to	Gate Data to CPU1 From	Gate Interrupts to CPU1 From
Power Off	None	NOT Cross	None	I/O-A Bus (Dummy Zeros)	None (Jammed Zeros)	None (Jammed Zeros)
		Cross	None	I/O-B Bus (Dummy Zeros)	None (Jammed Zeros)	None (Jammed Zeros)
Power On	NOT Local	NOT Cross	OPR IPR	I/O-A Bus None	I/O-A Bus* I/O-A Bus	I/O-A Interrupts
		Cross	OPR IPR	I/O-B Bus None	I/O-B Bus* I/O-B Bus	IOB Interrupts
	Local	NOT Cross	OPR IPR	BIO1 Bus None	BIO1 Bus* BIO1 Bus	I/O-A Interrupts
		Cross	OPR IPR	BIO1 Bus None	BIO1 Bus* BIO1 Bus	I/O-B Interrupts

*Data from cross strap logic is gated off by I/O buffer

Identical conditions apply to CPU2 except that BIO2, I/O-B, and I/O-A bus replace BIO1, I/O-A, and I/O-B bus, respectively.

The cross strap steering logic also includes selection gates to assure that the 102.4 kHz basic I/O clock is supplied to I/O-A or I/O-B from the clock divider associated with the CPU connected to each bus; e.g., 102.4 kHz-1 is gated to I/O-A logic when the buses are uncrossed (Cross is false) to optimize data transfer timing. In the event that one CPU is determined to be non-functional (OK Not in the CPU select logic), the clock divider associated with the other CPU is automatically gated to both I/O-A and I/O-B to assure full I/O capability in the event that a divider chain failure or power shutdown was the cause of the CPU's plight. Table 4.9.2-13 shows a summary of the 102.4 kHz source selection as a function of the CPU status and cross strap state.

4.9.2.2.2.6 I/O Buffer Logic. To accomplish the required tasks, the CPUs must be fed timely information from other boxes and they must be able to output their answers, in the form of control levels (discretes) or data, to other boxes so things get done as a result. Since a CPU has a lot of things to do and must be fast and efficient to accomplish them, it can't be kept waiting very long for input data, and likes to transmit each answer when ready, but only once. In addition, all external communication is conducted via a single data trunk, or I/O bus, which is just big enough to get 1 word (16 bits) in or out at a time. Something "out there" must funnel data from various sources into the I/O bus and also grab the answers as they appear, sort them out, and send them where they're supposed to go.

TABLE 4.9.2-13. SERIAL TRANSFER CLOCK (102.4 kHz) SOURCE SELECTION

I/O Crossed State	Uncrossed		Don't Care		Crossed	
CPU1 Status	Not OK	OK	OK	Not OK	Not OK	OK
CPU2 Status	Not OK	OK	Not OK	OK	Not OK	OK
102.4 kHz Clock Source for Serial Buffers in CPU Section A	CD 1	CD 1	CD 1	CD 2	CD 2	CD 2
102.4 kHz Clock Source for Serial Buffers in CPU Section B	CD 2	CD 2	CD 1	CD 2	CD 1	CD 1

The thing "out there" is a set of hardware registers called I/O buffers, each of which is expected to supply or accept one word via the I/O bus when required. To avoid complete chaos, each I/O buffer has a unique address and always supplies or accepts a word or series of words unique to its address. Each I/O buffer connects itself to the I/O bus if and only if it has been addressed by the CPU.

There are four kinds of I/O buffers:

1. A Serial Input Buffer (SIB) fetches data serially, one word at a time, from an external unit and puts it on the I/O bus when addressed;

2. A Serial Output Buffer (SOB) does the same thing in the other direction;

3. A Parallel Input Buffer (PIB) stores one bit of data from each of 16 external units and puts all 16 bits onto the I/O bus when addressed; and,

4. A Parallel Output Buffer (POB) grabs and stores 16 bits from the I/O bus when addressed and then continues to output each bit as a control level (discrete) to an external unit.

In a few cases, SIBs and SOBs must transfer data when the units are ready, which is unhandy for the busy CPU; in these cases, the I/O buffer works somewhat on its own and signals the CPU by means of an interrupt via the interrupt controller when data is ready (SIB) or needed (SOB).

Table 4.9.2-14 identifies assigned buffer functions, hexadecimal addresses, and bus connections. The control code HEX digit which defines the type of operation - OPR, IPR, etc. is not included but is in reality the most significant digit of a complete 4 digit address. Redundant buffers (which reside on two buses) have identical addresses and each bus (I/O-A, I/O-B, BIO-1, BIO-2) has a separate address bus and internal strobe timing pulses.

TABLE 4.9.2-14. BUFFER ADDRESS ASSIGNMENT

Buffer Address (hex)	Buffer Image Table Index No.		Buffer Type	Bus	Functions/Subsystem	CIU Perf. Spec. Buffer Reference Number
	Dec	Hex				
119			PIB	1/2	CPU1 TCC/CPU2 TCC	5/6
138	0	0	POB	1/2	CPU1 Interrupt Cont./ CPU2 Interrupt Cont.	1/2
149			PIB	1/2	CPU1 Flag Inputs/CPU2 Flag Inputs	11/12
168			Spec.	1/2	CPU1 Status Monitor/ CPU2 Status Monitor (MEOK)	3/4
189			PIB	1/2	CPU1 Uplink Data/CPU2 Uplink Data	44/45
20E	12	C	POB	A/B	AVHRR Discretes	48/53
216	1	1	POB	B	RYC 1B/PTC 2B/X Gyro Test-Discretes	14
21A	2	2	POB	A/B	AIP/ESA/TIP/XSU/SSE Discretes	35/65
21C	11	B	POB	B	SCU EED Discretes	38
226			POB	A/B	CPU on A RWA Control/ CPU on B RWA Control	15/16
22A	3	3	POB	A/B	IMU/RWA/SAD Discretes	36/66
22C	4	4	POB	B	RYC 2B/PTC 1B/IMU/SCU Discretes	40
231			PIB	A/B	RWA Speed and Flags	17/18
246	5	5	POB	A/B	IMU/RWA Discretes	33/63
24A			POB	B	SCU Thruster Discretes	37
24C	6	6	POB	A/B	PSE/DTR/TCE Discretes	51/61
258	13	D	POB	A/B	TCE Discretes	8/58
286	7	7	POB	A	RYC 1A/PTC 2A Discretes	34

TABLE 4.9.2-14. BUFFER ADDRESS ASSIGNMENT (Continued)

Buffer Address (hex)	Buffer Image Table Index No.		Buffer Type	Bus	Functions/Subsystem	CIU Perf. Spec. Buffer Reference Number
	Dec	Hex				
28A	8	8	POB	B	SCU EED Discretes	39
28C	9	9	POB	B	Growth	52
298	14	E	POB	A/B	AVHRR Discretes	49/54
2A4	15	F	POB	A/B	SCU/DAU Discretes	9/59
2A8	16	10	POB	A/B	HIRS Discretes	55/75
2C2	17	11	POB	A/B	TCE Discretes	56/68
2C4	10	A	POB	A	PTC 1A/RYC 2A Discretes	13
2C8	18	12	POB	A/B	DCS Discretes	7/57
407			SIB	A/B	TIP Subcom Telemetry	79/80
(1) 413			SIB	B	IMU Buffer Extender (Boost Mode)	28
415			SIB	A/B	Sun Sensor Data	42/72
(1) 423			SIB	B	IMU Buffer Extender (Boost Mode)	29
425			SIB	A/B	ESA Data	43/73
(2) 432			SOB	A/B	CPU A Telemetry Dump Data/CPU B Telemetry Dump Data	19/20
(1) 443			SIB	B	IMU Buffer Extender (Boost Mode)	30
445			SIB	A/B	SAD Data	46/76

(1) These buffers are used during Boost Mode to extend capacity for transferring IMU data.

(2) Buffer 432 is normally used for CPU Telemetry. In boost mode the buffers with note (2) are used to extend CPU Telemetry data transfer

TABLE 4.9.2-14. BUFFER ADDRESS ASSIGNMENT (Continued)

Buffer Address (hex)	Buffer Image Table Index No.	Buffer Type	Bus	Functions/Subsystem	CIU Perf. Spec. Buffer Reference Number
(2) 452		SOB	B	CPU on B Telemetry Dump Data Extender (Boost Mode)	21
454		SOB	A/B	PSE Mode Command	82/83
(2) 462		SOB	B	CPU on B Telemetry Dump Data Extender (Boost Mode)	22
464		SOB	A/B	CXU Command Data	84/85
470		SOB	A/B	CPU A Command Verify/CPU B Command Verify	25/26
(1) 483		SIB	A/B	IMU Data	31/32
(2) 492		SOB	B	CPU on B Telemetry Dump Data Extender (Boost Mode)	23
494		SOB	A/B	Growth	86/87
(2) 4A2		SOB	B	CPU on B Telemetry Dump Data Extender (Boost Mode)	24
4B0		SOB	A/B	TIP Mode Command	27/77
4D0		SOB	A/B	MIRP Mode Command	47/78
4E0		SOB	A/B	XSU Mode Command	50/70
A30	19	POB	A	Growth	67
A50	20	POB	A	Growth	69
A88	21	POB	A/B	TX/MIRP/AIP/SATCU Discretes	10/60

(1) IMU extension buffers for boost mode.

(2) CPU telemetry extension buffers for boost mode.

TABLE 4.9.2-14. BUFFER ADDRESS LIST (Continued)

Buffer Address (hex)	Buffer Image Table Index No.	Buffer Type	Bus	Functions/Subsystem	CIU Perf. Spec. Buffer Reference Number
AA0	22	POB	A/B	HIRS/SAD/CXU/SARR/SCU Discretes	62/74
AC0	23	POB	A/B	DCS Discretes	64/81
C60		SOB	A	Growth	41
C90		SOB	A	Growth	71

4.9.2.2.2.6.1 Standard Buffer Operation

4.9.2.2.2.6.1.1 Parallel Output Buffer. A Parallel Output Buffer (POB) includes a 16 bit register to which data can be uniquely transferred via the BIO1/2 or IOA/B interface by a CPU OPR operation. Each register retains its contents statically until another OPR operation occurs to that specific register. Each stage of the register is coupled through a buffer amplifier to an output line.

Data appearing on the I/O bus data lines is parallel-strobed into the register at the leading edge of the STROBINT pulse from the data trunk buffer control logic (Section 4.9.2.2.2.4.1) if, and only if, the buffer address is also present from the same logic; the buffer contents remain static at all other times. If the buffer resides on the selected bus as determined by the bus select control, then only the CPU which is in control may cause data to be strobed into the buffer.

4.9.2.2.2.6.1.2 Parallel Input Buffer. A Parallel Input Buffer (PIB) includes a 16 bit register from which data can be uniquely transferred via the BIO1/2 or I/O-A/B interface by a CPU IPR operation. The input to each stage of the register of all input lines is parallel strobed into the register at the leading edge of each STROBINT pulse from the data trunk buffer control logic (Section 4.9.2.2.2.4.1) and the contents of the register are gated onto the I/O bus on receipt of the buffer address from the same logic.These operations assure static but current data in the register for CPU read in.

4.9.2.2.2.6.1.3 Serial Output Buffer. A Serial Output Buffer (SOB) includes a 16 bit register to which a data word can be transferred via the BIO1/2 or IOA/B interfaces by a CPU OPR operation. The register subsequently presents the data serially via a buffer amplifier to an output line (to an external unit). The data word is output most significant bit (bit 1 of a CPU data word) first.

The serial transfer is controlled by a sequencer, which functions as described below and as shown in Figure 4.9.2-25. The sequence and timing of interface signals is shown in Figure 4.9.2-26.

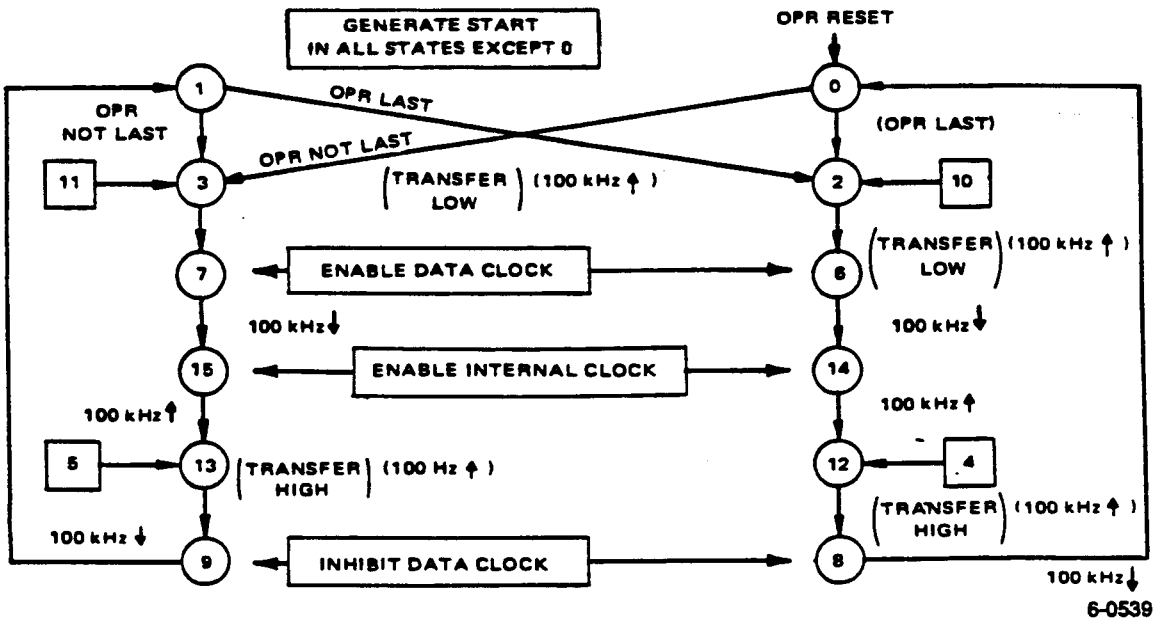

Figure 4.9.2-25. Serial Output Buffer State Diagram

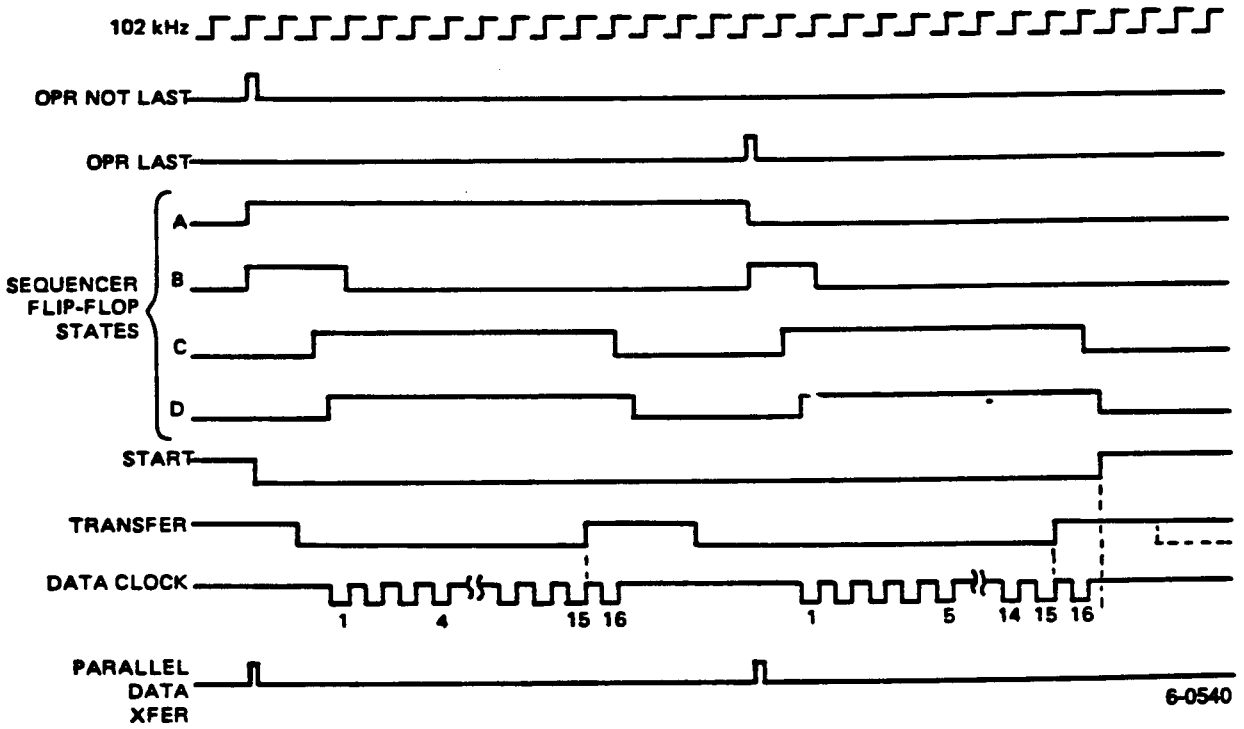

Figure 4.9.2-26. Serial Output Buffer Signal Timing

The sequencer (and/or address decoding logic) recognizes four types of CPU operation, as specified by the I/O address word control code (see Table 4.9.2-10):

1. In response to an IPR Status operation, the sequencer gates a 4 bit status code onto the I/O bus data lines 13 through 16; this status code identifies, for the software, the current sequencer state (i.e., readiness to accept a new word for transfer) in accordance with Table 4.9.2-15. The sequencer will not accept a new word for transfer unless its status is ready (sequencer state 0 or 1).

2. In response to an OPR Not Last operation, the sequencer accepts and transfers the data word but does not terminate the interactive interface with the external unit when the transfer is complete. This operation implies that this is not the last word of a multi-word transfer.

3. In response to an OPR Last operation, the sequencer accepts and transfers the data word, and terminates the interactive interface when the transfer is complete. This operation implies a single word transfer or the last word of a multi-word transfer.

4. In response to an OPR reset operation, the sequencer is unconditionally placed into the standby state (State 0).

The first OPR operation after an OPR reset causes the Start line to go low within 5 microseconds after the negative going edge of the I/O Alert signal; OPR Not Last causes the sequencer to advance to state 2.

TABLE 4.9.2-15. SERIAL OUTPUT BUFFER STATUS CODES

			Status Code			
State	Status	Bit 1-12	13	14	15	16
0	Standby (Ready for OPR)	No output from serial buffer	0	0	0	0
2	Waiting for Transfer		0	0	1	0
4			0	0	0	1
12	Shifting Serial Data	I/O Buffer jams zeros	0	0	0	1
8			0	0	0	1
1	Standby (Ready for OPR)		0	1	0	0
3	Waiting for Transfer		0	1	1	0
5			0	1	0	1
13	Shifting Serial Data		0	1	0	1
9			0	1	0	1

The external unit responds to the low Start line by causing the Transfer line to go low (after a variable delay), indicating readiness to accept data. Transfer low causes the sequencer to advance from state 3 to state 5 (or state 2 to state 4).

The sequencer is supplied with an ungated 102.4 kHz square wave clock from the timing section of the CIU. The sequencer advances from state 3 to state 7 (or from state 3 to state 6) only when the ungated clock goes high, to prevent the generation of partial Gated Clock pulses.

In state 6 or state 7, the serial data buffer initiates a burst of Gated Clock pulses to the external interface at a frequency of 102.4 kHz $\pm$1 kHz; the Gated Clock pulse (low) duration is 4.88 $\pm$0.2 microseconds.

At the next negative transition of the ungated clock, the sequencer advances from state 7 to state 15 (or from state 6 to state 14) and initiates internal clock pulses to shift the data register. The register shifts synchronously with the negative going edges of the external clock. On the next positive transition of the clock, a transition is made from state 15 to state 13 or from state 14 to state 12.

The external unit shifts in Serial Data at the positive going edges of the Gated Clock signal and places a high level on the Transfer line within 3.0 microseconds after the 15th Gated Clock pulse. The high Transfer level causes the sequencer to advance from state 13 to state 9 (or from state 12 to state 8), disabling the Gated Clock line (forced high) at the first positive going edge of the Gated Clock pulse after the positive going edge of the Transfer signal.

The next negative going edge of the ungated clock advances the sequencer from state 9 to state 1 (or from state 8 to state 0), terminating the internal register shift clock pulses. At sequencer state 0, the Start signal is terminated.

The external unit holds the Transfer line high for a minimum duration of 15 microseconds, and then may place a low level on the Transfer line as soon as the external unit is again ready to accept additional data.

If the buffer resides on the selected bus as determined by the bus select control signal, then only the CPU which is in control may cause data to be strobed into the buffer or alter the state of the sequencer.

4.9.2.2.2.6.1.4 <u>Serial Input Buffer</u>. A Serial Input Buffer (SIB) includes a 16 bit register which can transfer data to the BIO1/2 or I/O-A/B interface during a CPU IPR operation. The register is loaded by serial transfer from an external unit via a Serial Data In line. The data is transferred most significant bit (bit 1 of a CPU data word) first, with one exception - data from the IMU is transferred least significant bit first. The MSB-LSB interchange is performed in the CIU harness board.

The serial transfer is controlled by a sequencer, which functions as described below and as shown in Figure 4.9.2-27. The sequence and timing of interface signals is as shown in Figure 4.9.2-28.

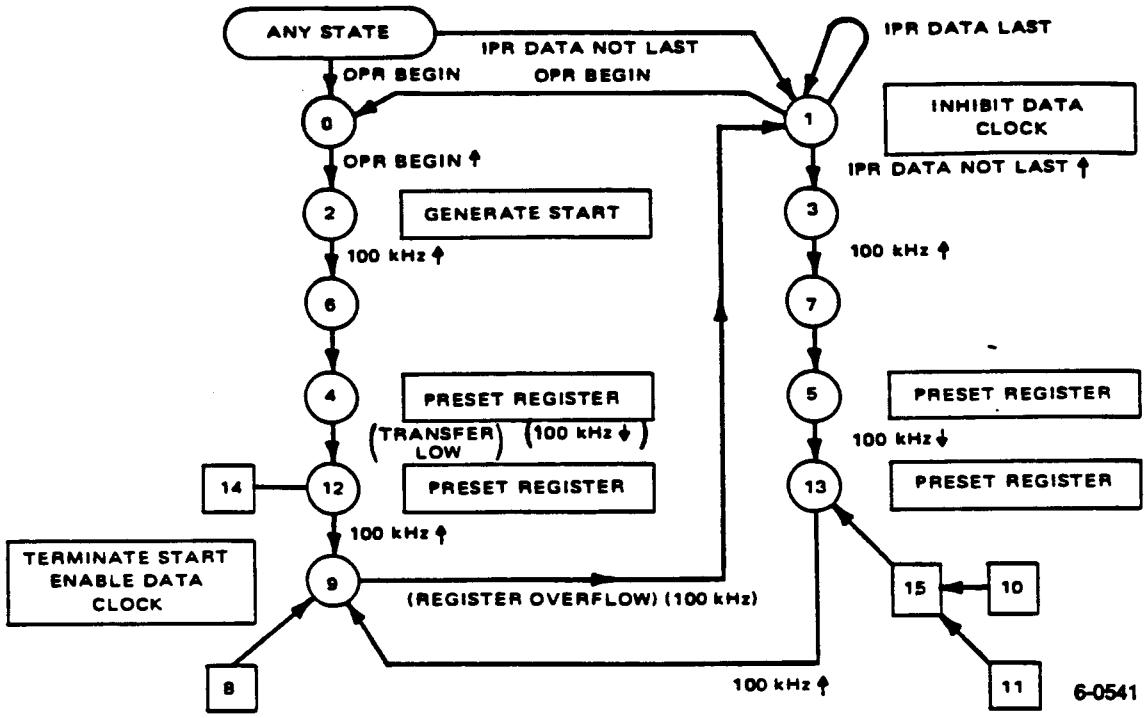

Figure 4.9.2-27. Serial Input Buffer State Diagram

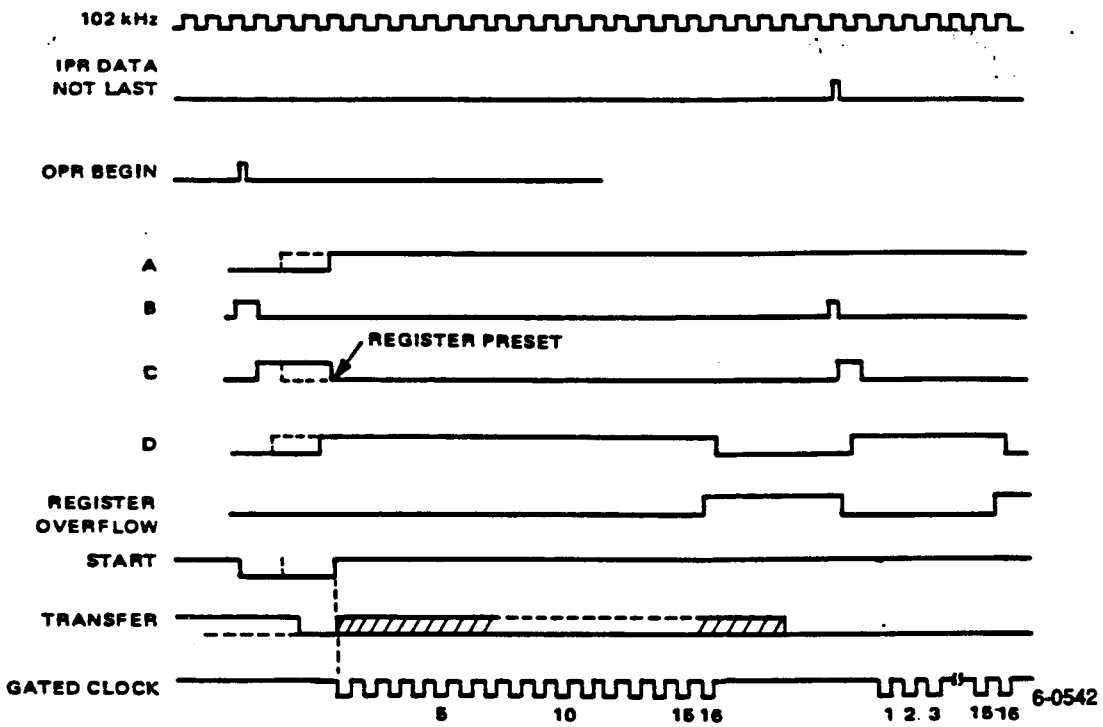

Figure 4.9.2-28. Serial Input Buffer Signal Timing

The sequencer recognizes four types of CPU operations, as specified by the I/O address word control code (see Table 4.9.2-3):

1. In response to an IPR Status operation, the sequencer gates a four bit status code onto the I/O bus data lines 13 through 16 (1 through 4 in the case of the IMU buffers); this status code identifies, for the software, the current sequencer state (i.e., the availability of data for input) in accordance with Table 4.9.2-16.

2. An OPR Begin operation resets the sequencer to state 0 from any other state. This operation causes a re-initiation of the interactive interface with an external unit to restart the data transfer process.

3. In response to an IPR Not Last operation, the sequencer gates the current buffer contents onto the I/O bus and then proceeds to input a new word from the external unit; this operation implies that this is not the last word of a multi-word transfer.

4. In response to an IPR Last operation, the sequencer gates the current buffer contents onto the I/O bus, but does not input a new word from the external unit. This operation implies that this is a single word transfer or the last word of a multi-word transfer.

TABLE 4.9.2-16. SERIAL INPUT BUFFER STATUS CODES

		IMU Buffers 483					All Serial Buffers Except 483, 189*				
State	Status	Bit 1	2	3	4	5-16	1-12	13	14	15	16
0, 1	Full (Ready for IPR Data)	0	0	0	0	**	**	0	0	0	0
2, 3		0	0	1	0	**	**	0	1	0	0
4	Waiting for Transfer	0	1	0	0	**	**	0	0	1	0
5		0	1	0	0	**	**	0	0	1	0
12, 13	Presetting Register	1	1	0	0	**	**	0	0	1	1
9	Shifting Serial Data	1	0	0	0	**	**	0	0	0	1

*Buffers 189 are special uplink processor buffers described in Section 4.9.2.2.2.2.

**No output from serial buffer. I/O buffer jams zeros.

The trailing edge of the decoded OPR Begin pulse advances the sequencer from state 0 to state 2, causing the Start line to go low (true). The next positive edge of 102.4 kHz clock advances the sequencer to state 4, where the buffer data register is preset with a 1 in the first stage and zeros in the remaining stages. The external unit places a low (true) level on the Transfer line to signify readiness to output data to the CIU. Transfer low causes the sequencer to advance from state 4 to state 12 at the next negative going clock edge.

At the next positive clock edge the sequencer advances from state 12 to state 9 and begins to output a burst of Gated Clock pulses (102.4 kHz) to the external interface, and to shift data into the buffer register at the negative going (leading) edge of each Gated Clock pulse. The transition to state 9 also terminates Start (line goes high).

After the 16th clock pulse has been gated out, the preset "one" has been shifted through the data register and appears at the last stage output. When the ungated clock goes high, this "overflow" signal causes the sequencer to advance from state 9 to state 1. The buffer content may be transferred to the CPU by an IPR operation at any time, but the data will be invalid if the buffer was not in state 1 prior to the IPR (the CPU may ascertain buffer state by an IPR Status operation).

An IPR Not Last places the sequencer in state 1, regardless of prior state, and the trailing edge of the decoded IPR pulse advances the sequencer from state 1 to state 3. The sequencer then advances in succession from state 3 to states 5, 13, 9, and 1 in a similar manner to the advance from state 2 to states 4, 12, 9, and 1 respectively, but with the following differences.

1. The Start line remains high;

2. The transition to state 13 does not depend on the Transfer line; and

3. An IPR Last operation may be performed by the CPU at any time, and has no effect on the SIB sequencer; bit if it is performed at any time other than sequencer states 0 or 1, will yield incorrect data.

4.9.2.2.2.6.2 Special I/O Buffers. Several CIU data buffers require unique designs and are not implemented by the modular buffer circuit boards.

4.9.2.2.2.6.2.1 Uplink Processor Buffers. Buffers with hex address 189 are highly specialized SIBs which are part of the uplink processors. Sequencer operation, serial transfer, and status codes are described in Section 4.9.2.2.2.2.

4.9.2.2.2.6.2.2 IMU Extension Buffers. Buffers with hex address 413, 423, and 443 are specialized "slave" SIBs. They are used to increase the capacity of buffer address 483 in Boost mode, and the shifting of data into them is controlled by the SIB 483 sequencer. These buffers respond to any IPR operation as a standard SIB responds to IPR Data Last.

4.9.2.2.3.6.2.3 RWA Speed Buffers. Buffers with hex address 231 are PIBs which interact with the Attitude Control Electronics (ACE) as discussed in Section 4.9.2.2.2.7.

4.9.2.2.2.6.2.4 MEOK Buffers. Buffers with hex address 168 exist only as addresses to which the CPUs must continually perform OPR and/or IPR operations to signal valid operation; the MEOK address decodes are part of the CPU select logic discussed in Section 4.9.2.2.2.5.1.

4.9.2.2.2.6.2.5 CPU Boost Telemetry Extension Buffers. Buffers with hex addresses 452, 462, 492, and 4A2 are specialized "slave" SOBs. They are used to increase the capacity of the CPUB telemetry buffer address 432 in boost mode only and the shifting of data into them is controlled by the buffer 432 sequencer. See Section 4.9.2.2.2.8.4 for details of operation.

4.9.2.2.2.7 Attitude Control Electronics. The Attitude Control Electronics (ACE) includes both digital and analog circuits which cross-interface the functionally redundant I/O buffers and CPU's with the numerically redundant RWAs. RWA Torque data from the I/O bus enabled by Bus Selection (Section 4.9.2.2.1.2.4) is converted to analog torque level outputs for each of the four RWAs; tachometer and flag signal inputs from all RWAs are sequentially converted to RWA Speed inputs to both I/O buses to allow parallel processing in the two CPUs.

4.9.2.2.2.7.1 RWA Torque Data Processing. The ACE processes RWA Torque data after it has been transferred to buffers with hex address 226 from the I/O-A or I/O-B interface respectively. The buffer data format is as follows:

1. Buffer bit 1 is a level discrete torque sign bit, with data 1 = +10V out = Negative Torque.

2. Buffer bits 2 through 9 are an 8 bit torque magnitude signal with a scale factor of 0.02 volt per count. Bit 2 is most significant and bit 9 is least significant.

3. Buffer bits 10 through 12 are unused and are nominally data 0's.

4. Buffer bits 13, 14, 15 and 16 contain a single "one" bit to signify that the torque magnitude data and torque sign apply to the Z, Y, X, or S (Skew) RWA, respectively.

A block diagram of the RWA torque output logic and analog circuitry is shown in Figure 4.9.2-29. As shown, there is a D/A converter, reference supply, and sequencer associated with each RWA Torque buffer, and there is a separate holding capacitor, operational amplifier, and sign flip-flop for each RWA output interface.

The 8 torque magnitude bits in each buffer are continuously converted to an analog level by the associated D/A converter. Each time a new word is strobed from the I/O bus into the buffer register, the data strobe pulse is output from the buffer as a Start pulse to the sequencer.

After a delay of 1 to 2 milliseconds (one to two 1024 Hz clock cycles) to allow D/A converter settling time, the sequencer internally generates a 4.9 millisecond (5 clock cycles) sample gate. This sample gate is logically AND'd with Bus Select A or Bus Select B and with each of the four RWA identification bits from the buffer. If its Bus signal is true (enabled), the sequencer thus generates a 4.9 millisecond pulse output on one of the four RWA interface strobe lines

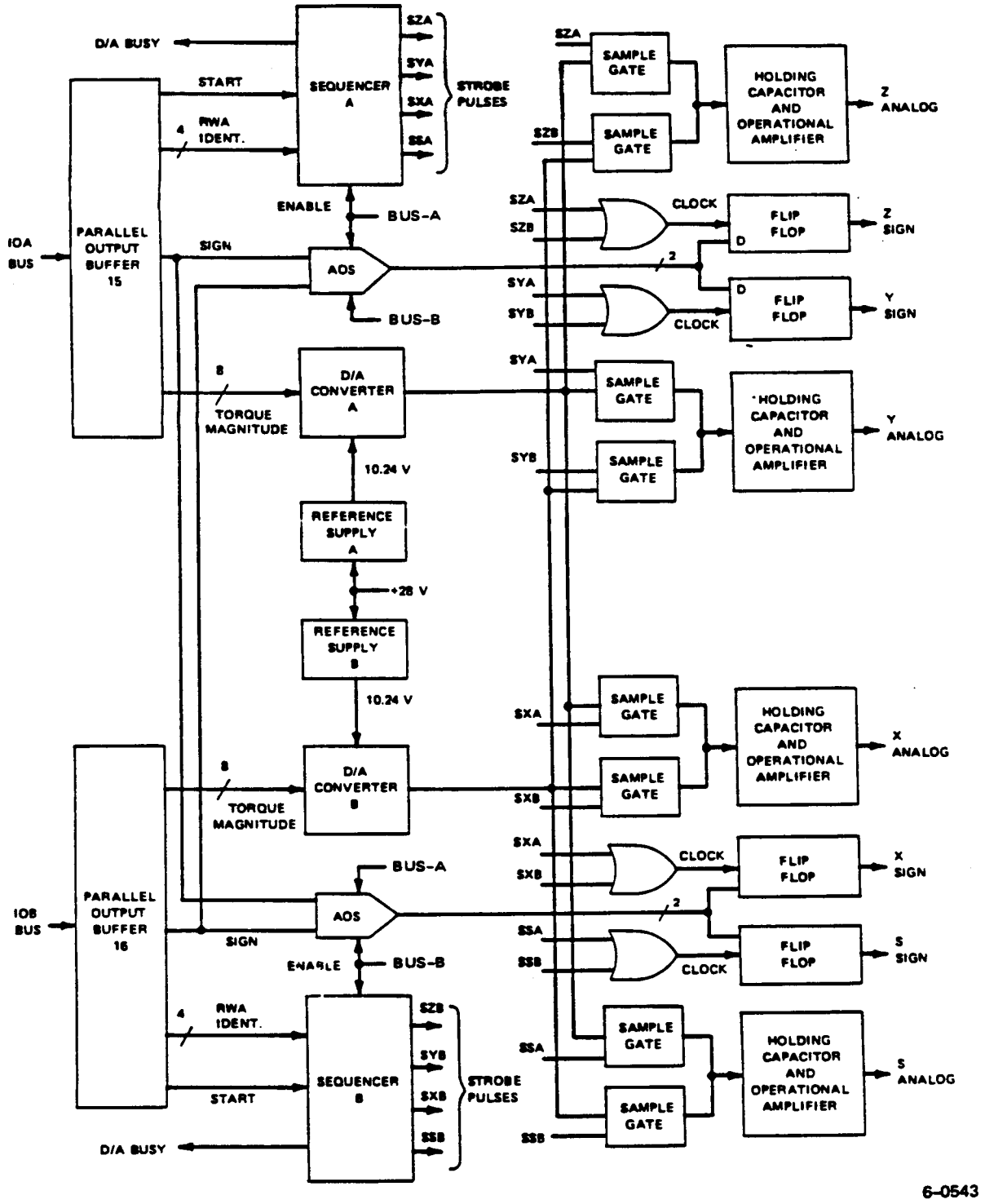

Figure 4.9.2-29. RWA Torque Output Logic and Circuitry

associated with its buffer/converter. This strobe pulse opens the sample gate connecting the D/A converter output to the interface holding capacitor and clocks the buffer sign bit, which is also gated by Bus Select state into the interface flip-flop.

When a new data word is output to the buffer which is not selected, the sequencer operates as above but no data is transferred to interface circuits.

The sequencer for each D/A converter also generates a D/A Busy flag. This signal is low (true) from the leading edge of the Start pulse until the trailing edge of the sequencer's internal gate. Each D/A Busy flag is steered by the cross strap logic and input to bit 10 of the Flag buffer (149) associated with the same CPU as the RWA torque buffer. The CPU should not output new data to the buffer until the associated D/A Busy flag is high.

The combination of each D/A converter and sample/hold circuit has the following characteristics:

- Output voltage range, 0.00 to +5.10 volts nominal
- Source resistance, 10 ohms or less
- Overall conversion error, ±1% of full scale (excluding droop)
- D/A quantizing error, ±1/2 LSB = ±0.01 volt maximum
- Settling time (within +0.005V of final value), 10 msec maximum relative to the transfer of data to the buffer
- Droop <0.3% of full scale in 500 msec

4.9.2.2.2.7.2 RWA Tachometer and Status Flag Signal Processing. The ACE includes circuitry for sequentially processing tachometer and status flag signals from each RWA to generate inputs to both RWA Speed buffers (231) for transmission to the I/O-A and I/O-B interfaces. The tachometer signals for each RWA are presented on three lines designated A, B, and C. Each input is an approximately square wave signal at a frequency proportional to wheel speed; for positive wheel rotation, B lags A by approximately 60 degrees and C lags B by approximately 60 degrees while for negative rotation A lags B and B lags C. There are also two discrete status flag inputs from each RWA, designated Power Limit Flag and Power On Flag.

The three tachometer signals for each RWA are each digitally differentiated to generate a pulse at each positive and negative transition, and these pulses are OR'd together into a single continuous speed signal with six signal pulses per cycle of the three tachometer waveforms.

The ACE sequentially gates each of the four speed signals into the clock inputs of two redundant binary counters; the duration of the signal gates is accurately fixed so that the count accumulated during each gate is a direct scaled measurement of wheel speed. The four speed measurements are made during successive 500 ms periods so that each RWA wheel speed is measured once every two seconds in accordance with the timing diagram shown in Figure 4.9.2-30.

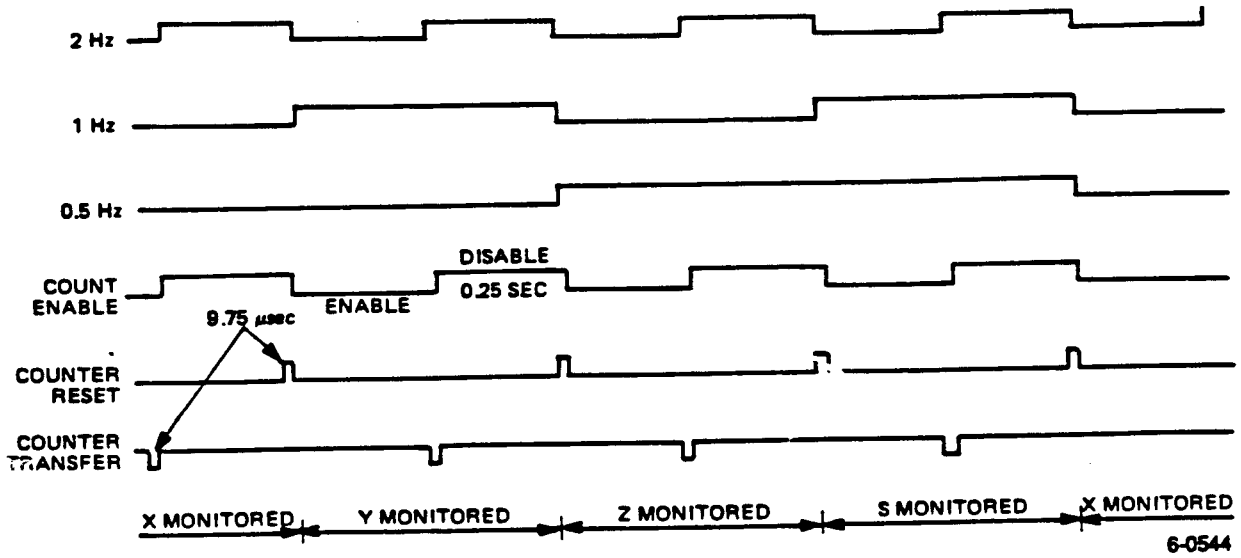

Figure 4.9.2-30. RWA Speed Measurement Timing Diagram

Each measurement gate has a duration of 250 ±0.1 milliseconds and its leading edge is synchronized within ±50 microseconds to the 2 Hz sync output of the time code counter. During the measurement gate, the logic detects tachometer signal phase by redundantly storing the logical value (1 or 0) of ØA at the positive transitions of ØB while counting the number of speed signal pulses to generate an 11 bit binary count.

In the event the wheel is rotating faster than 10,240 rpm, the maximum capacity of the counter, the CIU inhibits the clock from advancing the counter beyond the all 1's state. This prevents a wheel which is actually rotating very fast from indicating a speed near zero, since the counter would recycle back to zero after reaching the all 1's state.

At the trailing edge of the measurement gate, the detected rotation sense and the accumulated speed count are parallel transferred into the RWA Speed buffers (231), along with the logical value of each status flag and a 2 bit code identifying the RWA to which they apply. Data are transferred to each buffer in the following format:

1. Rotation sense is input to buffer bit 1, with data 1 = negative sense.

2. The RWA identification code is input to buffer bits 2 and 3; 00 = X, 01 = Y, 10 = Z, and 11 = S.

3. The Power On flag is input to buffer bit 4, with data 1 = true (power is on).

4. The Power Limit flag is input to buffer bit 5, with data 1 = true (RWA is power limited).

5. The speed count is input to buffer bits 6 through 16; bit 6 is the MSB and the LSB (bit 16) weight is 5 rpm per count.

4.9.2.2.2.8 Special Gating

4.9.2.2.2.8.1 CIU Boost/Orbit Switching. CIU Boost/Orbit switching is controlled by two level discretes, one on I/O-A, called Boost A, and one on I/O-B, called Boost B. The CIU will cause Boost Mode to be activated only if Boost Mode-A and Boost Mode-B discretes are true. Otherwise, the orbit mode will be activated.

4.9.2.2.2.8.2 IMU Data Special Processing. The processing logic associated with IMU Data buffers and the priority level 9 interrupt are augmented and modified to meet the different requirements for Boost mode and Orbit mode operation as shown in Figure 4.9.2-31.

The IMU 10 Hz Sync, IMU Data Clock, IMU Data Ready, and IMU Data signals each have two redundant interface lines between the IMU and the CIU. These interfaces are designated A and B (but this designation is not related to the A and B suffixes on signal names within the CIU, which relates them to the I/O-A and I/O-B buses). An IMU Interface Select signal from the IMU is used to gate the active interface lines for the IMU Data and IMU Data Ready signals. IMU Data A and IMU Data Ready A are gated whenever the IMU Interface Select line is low (0 volts), and the IMU Data B and IMU Data Ready B are gated whenever the line is high (+10 volts). The gated IMU Data is fed to both IMU buffers (483). The CIU drives both the inactive and the active interface lines for the IMU Data Clock signals.

In order to provide both CPUs with coherent IMU Data, only one of the buffers is allowed to input data at a time. The buffer on the enabled I/O bus (as determined by Bus Select B) is given priority and allowed to input data first. This priority control is exercised by the signal designated IMU Select A and its logical complement, generated by the priority logic. When the priority buffer has completed its read in, as determined by an IPR Last from its associated CPU, the other bus is enabled to read. When IMU Select A is false, the IMU Data Clock signals originate at the sequencer/controller for the buffer on I/O-B. When IMU Select A is true, those signals originate at the sequencer/controller for the buffer on I/O-A.

4.9.2.2.2.8.2.1 Boost Mode. In Boost mode, IMU Select A is always false and the serial transfer of data to the boost IMU buffers is enabled in the buffer 483 sequencer/controller logic section. IMU data is shifted into the serial input of buffer 443, the serial output of buffer 483 is shifted into the serial input of buffer 443, and so forth, until all four buffers have been serially loaded. The timing of IMU Data input to buffers in Boost mode is shown in Figure 4.9.2-32.

The buffer 483 sequencer is initially advanced to state 4 by a software OPR Begin. The IMU Data Ready signal is gated to buffer 483 sequencer as its Transfer signal, allowing the sequencer to proceed with serial data transfer.

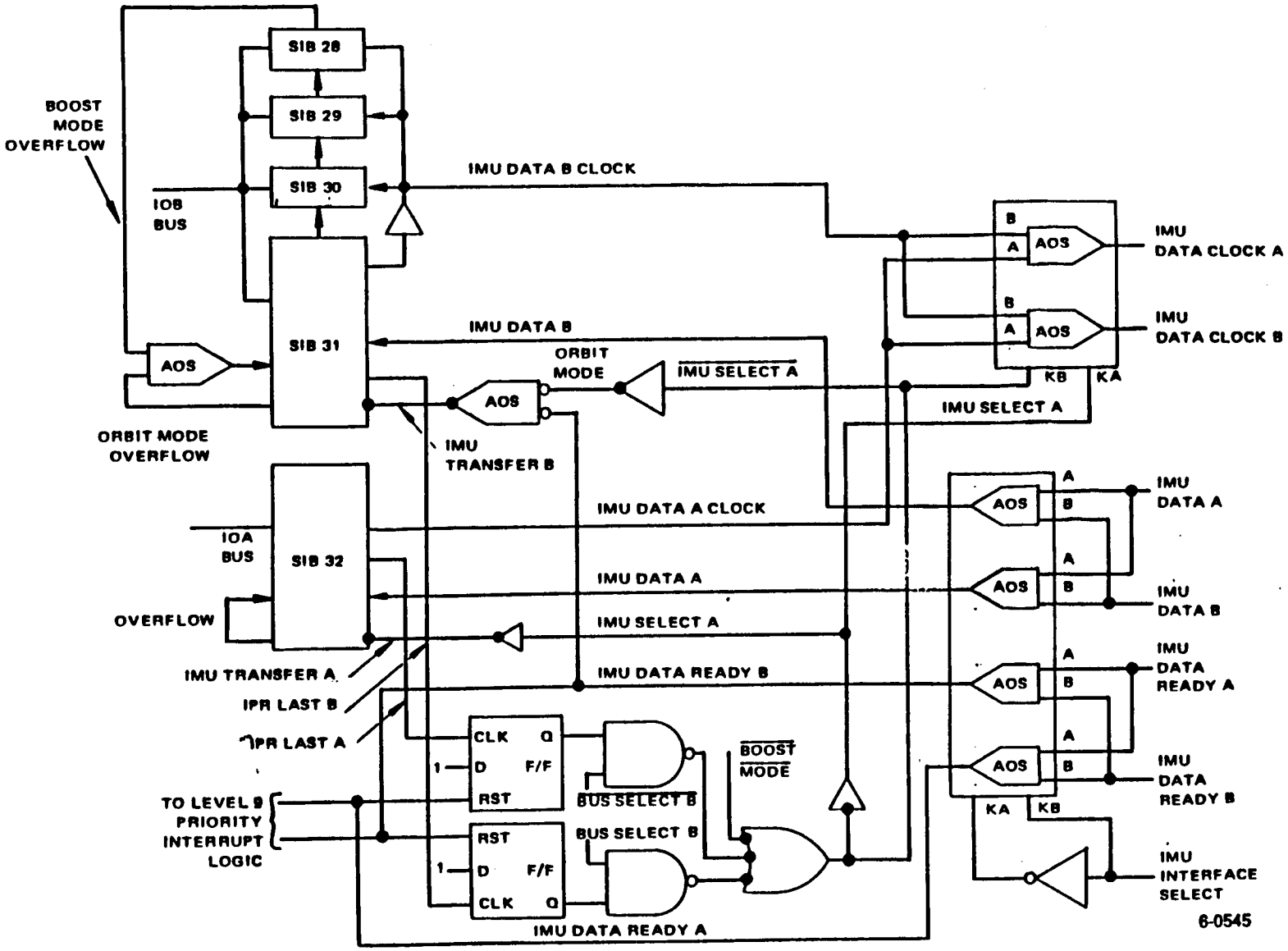

Figure 4.9.2-31. IMU Data Special Processing

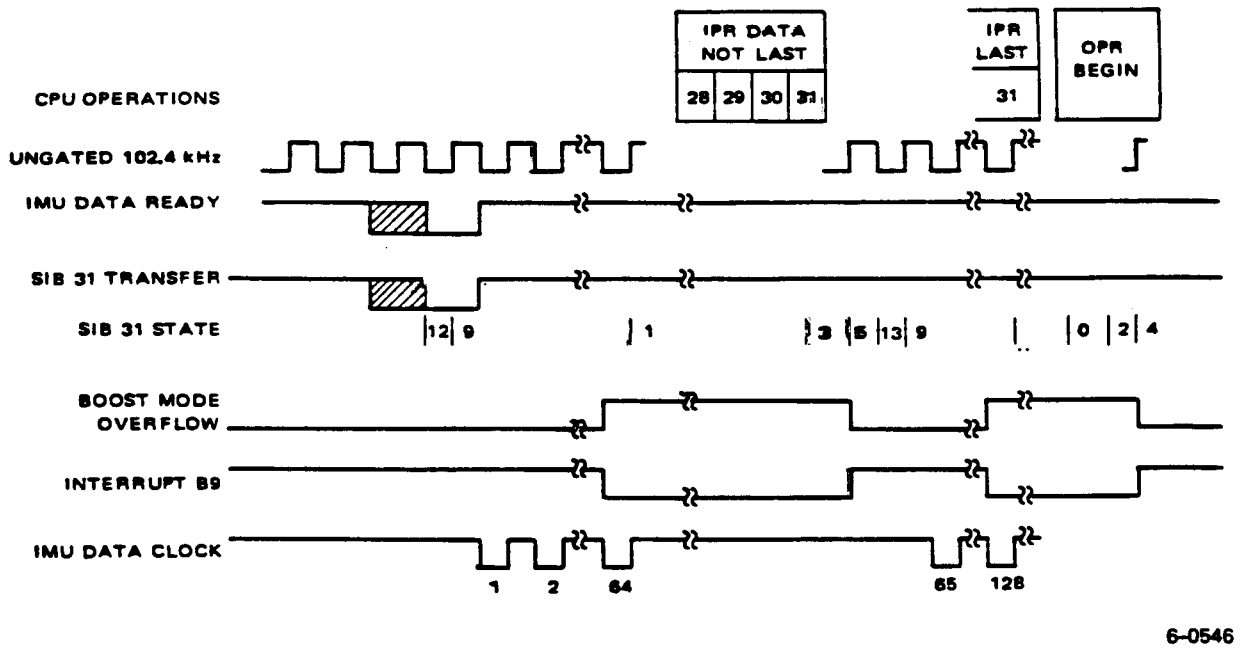

Figure 4.9.2-32. IMU Data Input Timing, Boost Mode

The "overflow" which causes the sequencer to advance from state 9 to state 1 (see Paragraph 4.9.2.2.2.6.1.4) is gated to the buffer 483 sequencer from buffer 413 and does not occur until the 64th data bit has been shifted. The overflow also activates Interrupt B9 to the CPU.

The CPU then performs IPR Not Last in succession from buffers 413, 423, 443, and 483. The last IPR causes the buffer 483 sequencer to initiate serial transfer of the next 64 bits (second half) of the IMU data. The overflow will again activate Interrupt B9 to the CPU. When the software is ready for the second half of the IMU and an IPR Last from buffer 483. The CPU finally performs an OPR Begin to buffer 483 to enable it for the next cycle.

4.9.2.2.2.8.2.2 Orbit Mode. The timing of IMU data input to buffer 483 in Orbit mode is shown in Figure 4.9.2-33. In Orbit mode, the IMU Select A signal allows successive control of the interface signals by the A or B bus sequencer, with the "first" sequencer selected according to the Bus Select function as previously described. Immediately following the IMU Data Ready signal, the IMU Select A function is set allow IMU data to be read into the buffer on the selected bus. Immediately following an IPR Last operation at the priority buffer sequencer, the IMU Select A function is set to allow IMU data to be read into the buffer on the unselected bus. When the CIU is in Orbit mode, the IMU Data Ready signal is gated to both interrupt A9 and interrupt B9.

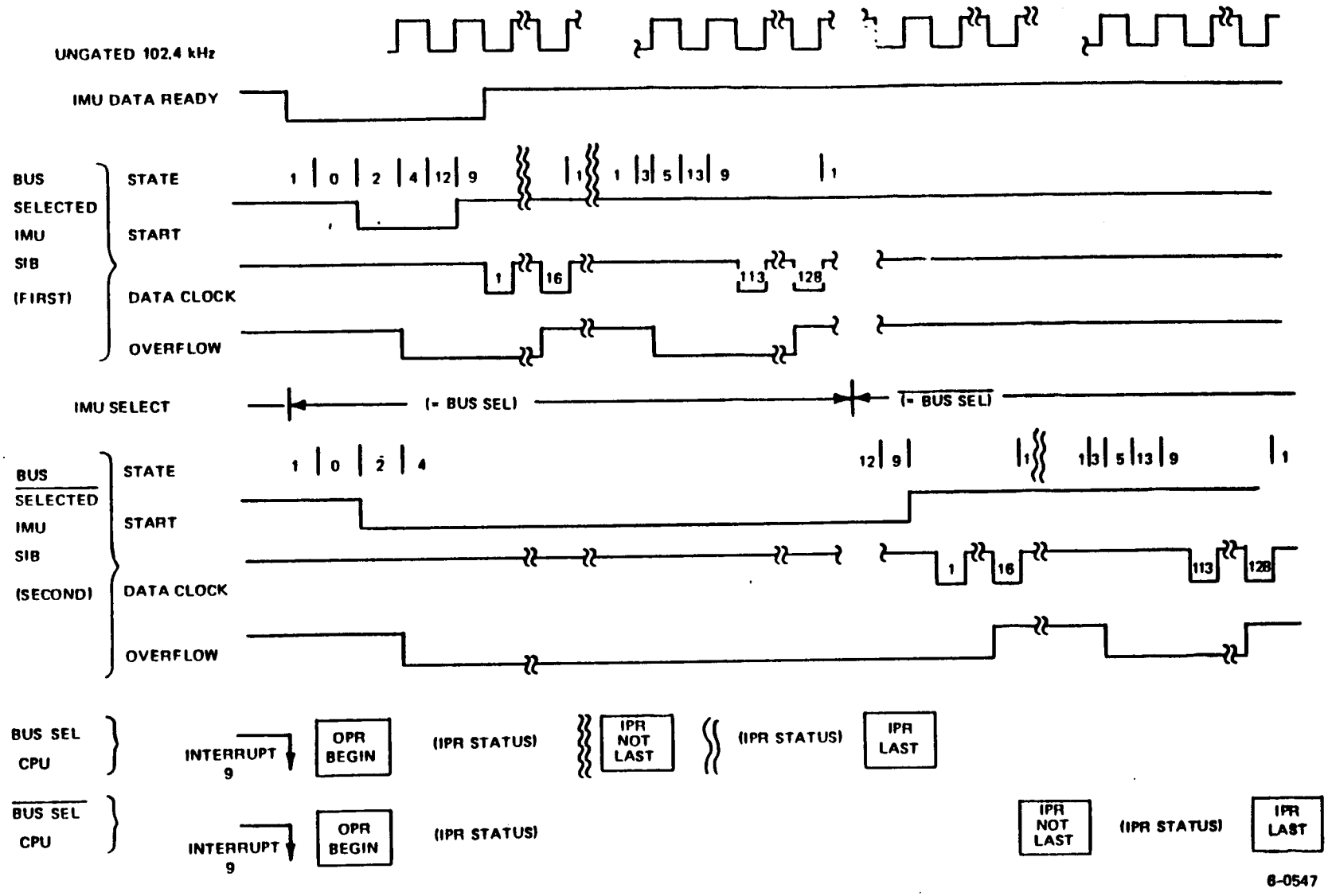

Figure 4.9.2-33. IMU Data Input Timing, Orbit Mode

In Boost mode, the software issues five consecutive OPR Last instructions to load data to buffers 4A2, 492, 462, 452, and 432 in that order. The OPR instruction to buffer 432 initiates the data transfer sequence. The Enable Boost Telemetry input signal is gated to buffer 432 as its Transfer signal so that the sequencer will remain in state 12 while 80 bits are serially transferred. The CPU Data Transfer input from the TIP, however, will go false after the 15th CPU Data Clock pulse, and remain false for 15 to 25 microseconds. During this period, the TIP will accept the 16th clock pulse but no additional pulses. To avoid loss of data, the CIU delays the CPU Data Transfer signal by 1 clock pulse and uses it to enable the data shift pulses to all the CPU telemetry buffers. Otherwise, the interface is standard as described in Paragraph 4.9.2.2.2.6.1.3. Figure 4.9.2-34 gives the timing details of the Boost mode data transfer.

4.9.2.2.2.8.4 Subcom Telemetry Data Processing. The CIU provides a standard redundant serial input buffer pair for this data, except that the Start signal is not used. The CIU provides the Subcom TLM Data Clock to each of the TIP sides and receives the Subcom TLM Data and Subcom TLM Transfer signals from each of the TIP sides. The Interface Enable signals are used to select the input signals from the powered TIP side.

An interrupt is initiated on Level 7 when the buffer overflow signal is activated. In response to this, the CPU (under software control) will process a four word transfer using the IPR Data Not Last instruction for the first three words and IPR Data Last Word instruction for the fourth word. The Transfer signal (and therefore interrupts also) occur at a 10 PPS rate during Orbit Mode operations. Subcom telemetry is not read in boost mode.

4.9.2.2.2.8.5 CV Data Special Processing. Command Verification data transmitted from the CIU to the TIP is selected from 1 of 2 sources. These sources are a CIU SOB on the I/O A bus and a CIU SOB on the I/O B bus. The CIU provides priority logic to select data from either one of the CIU SOBs.

The interfaces consist of the CV Start, CV Data, and CV Data Clock signals from each source. Priority is established on a "first come, first served" basis. Whichever source first initiates a Start signal causes its signals to be switched to the TIP and maintains control until the Start signal is terminated. At that time control is relinquished and a new source is free to take control by generation of its Start signal.

The priority logic is designed so that a failure of the Start signal in the active state from either of the CIU SOBs will not lockout the capability of access from the other source. A timer senses the fact that a Start signal has not terminated by the expected time and control of the priority logic is relinquished.

The CV Transfer signal is received from redundant TIP circuits and one of the two is selected under control of interface enable signals provided by the TIP indicating which signal should be used. Based on the status of the priority logic, the Transfer signal is appropriately routed to the I/O-A bus SOB or the I/O-B SOB.

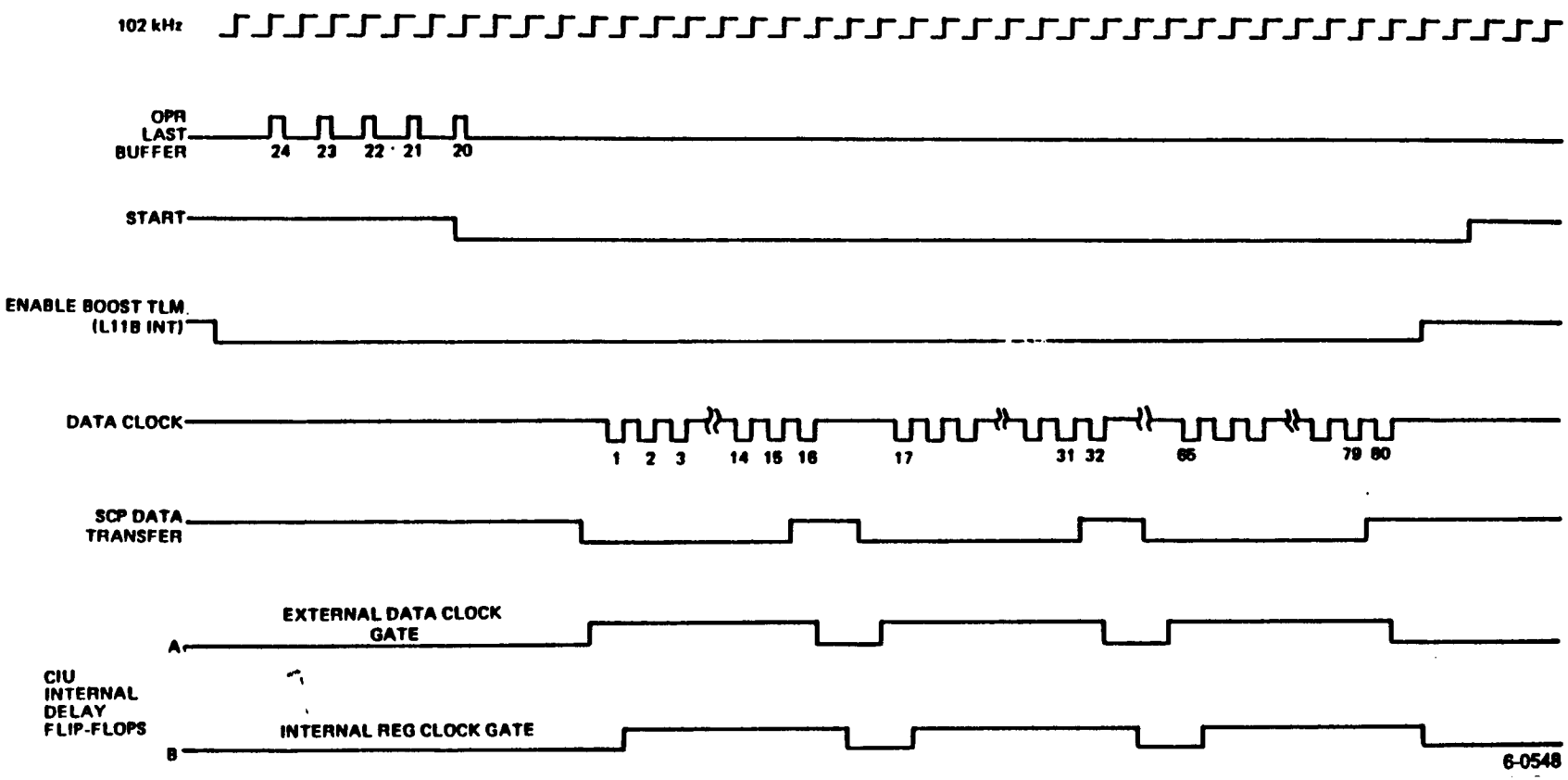

Figure 4.9.2-34. Boost Mode CPU Telemetry SOB Timing Diagram

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Contract No. F04701-75-C-0182
Contractor: GE Astro
Explanation of Limited Rights Data Identification Method Used
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4.9.2.3 Standard Controls Processor

The Standard Controls Processor (CPU) is a miniature, general purpose data processor operating in fractional, fixed point, 2's complement arithmetic. The CPU provides the computational capabilities required for real time, "hands-off" attitude control and for other data processing as required for satellite monitoring and control. Each CPU contains 32K words of read/write memory; the instruction set provided in microprogram control ROM provides facilities for addressing memory, fetching instructions and data, performing arithmetic and logical operations, and loading and storing data. The CPU used for ATN-HIJ is more specifically known as the SCP-234FT. The SCP-234FT read/write memory uses single error detection and correction with double error detection to maintain a highly-reliable data and program storage.

An interface diagram for the CPU is shown in Figure 4.9.2-35. The CPU interfaces with the rest of the spacecraft only through the Controls Interface Unit (CIU). The CIU provides the power and the various control and timing signals required by the CPU, and transfers all data and control signals from the CPU to other spacecraft units.

4.9.2.3.1 Organization

4.9.2.3.1.1 System Aspects. The CPU contains five logic boards which are interconnected as shown in Figure 4.9.2-36. The processing portion consists of two logic boards identified as the Memory Address Generator-I/O (MAG-I/O) and Arithmetic and Logic Unit (ALU). The memory section is composed of two identical boards each containing 16,384 words of read/write memory (RAM). The memory size for the ATN-HIJ SCP-234FT is 32K, and is expandable to 64K.

Interfaces between the CPU and the CIU, power converter, and ground support equipment are shown in Figure 4.9.2-35. Input and output data transfers between the CPU and CIU are performed via the bi-directional input/output bus and associated word markers. External interrupt requests generated by the CIU are stored in the CPU prior to servicing. Clock signals and power are supplied from oscillators and dc to dc converters shared with the CIU. The Reset input, when activated, forces the CPU to enter interrupt level 16 and to execute an initialization routine stored in the bootstrap Read Only Memory (ROM). The 9 line Ext/Int bus is used to direct the internal Control ROMs (CROMs) which contain the microprogram for any desired microinstruction. The memory protect override, when active, enables the CPU to modify contents of protected memory locations while operating on any interrupt level.

The Run/Stop input, in conjunction with the Ext/Int control lines, is only used for ground checkout operations.

4.9.2.3.1.2 CPU Hardware. The CPU and memory are partitioned into several boards which are described below.

The MAG-I/O board contains the following functions:

- Microprogram control logic
- Clock generator logic
- Interrupt logic
- Error control logic

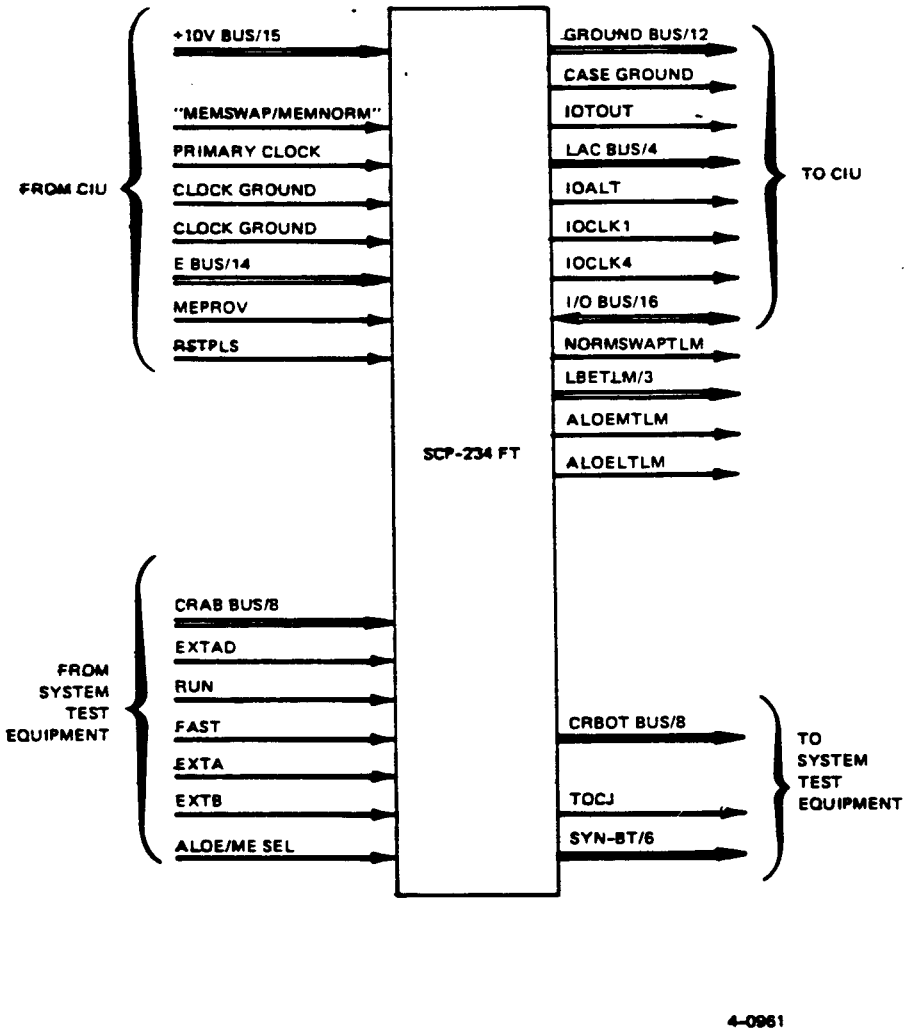


Figure 4.9.2-35. SCP-234FT Interface Diagram

- Input/output logic
- Memory interface logic
- Program counter
- Index registers X, Y, Z
- Instruction register
- Booststrap Rom
- Miscellaneous logic

The Arithmetic and Logic Unit (ALU) board contains the following functions:

- Adder and logical operations logic
- Accumulator, multiply-quotient, and memory data registers
- Multiply, divide, and miscellaneous special logic

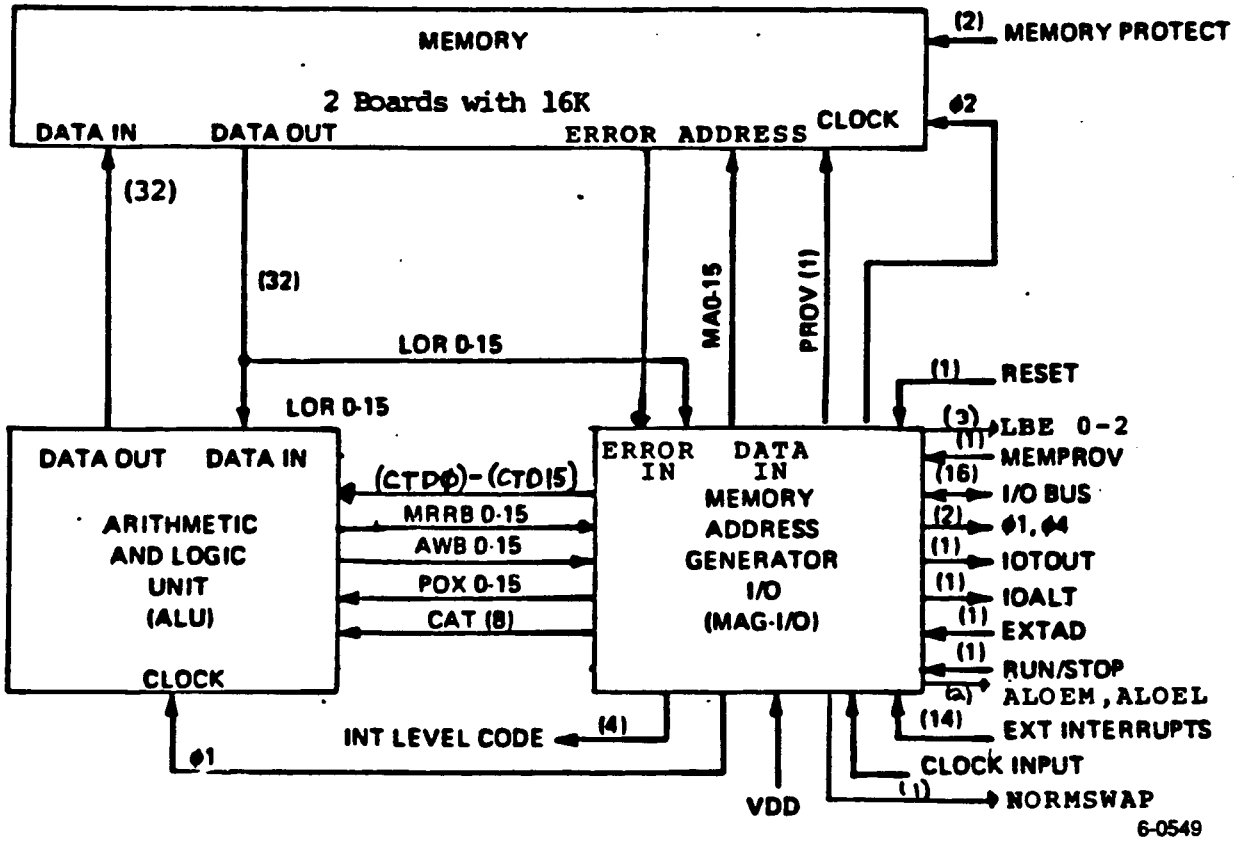


Figure 4.9.2-36. CPU Configuration

The 16K memory boards contain the following functions:

- Addressing logic
- Random Access Memory (RAM) (4096 x 1 bit ICs)
- Data output select logic
- Miscellaneous logic
- Memory Error Detection and Correction Logic (SEL/DED)

4.9.2.3.2 Control

4.9.2.3.2.1 Microprogram Control. Most operations within the processor and some memory functions are accomplished by a central microprogrammed control system, which operates as described below.

The processor control system includes a Control Read Only Memory (CROM) which is entirely independent of the main memory. The execution of instructions and other routines by the processor requires a series of sequential steps, each

The CAT itself is driven by one of two registers designated ROMAR 1 and ROMAR 2. These registers (8 bits wide), which contain addresses in CROM of the subsequent microinstruction, are selectively enabled to seize the CAT and thus generate the address code.

ROMAR 1, in general, is used for addressing all microinstructions which do not initiate the execution of a new instruction. ROMAR 2, in general, is used to point the CROM to the first EO of any instruction and, in addition, to initiate execution of the interrupt routine, to initiate the power initialization routine, to provide access for external address codes (test mode only), and to perform microprogram branches associated with the XFR instruction.

Actual address codes which are stored in ROMAR 1 and ROMAR 2 are obtained from any one of the sources shown in Figure 4.9.2-37 and listed below.

- Next Address ROM
- Branch Address ROM
- Instruction Start Address ROM
- Control Instruction Register (CIR)
- External Address Input

The next address code to enter ROMAR 1 is a function of the microinstruction being executed. Under normal conditions, the contents of the Next Address ROM are selected. When the current microinstruction specifies a test which involves a conditional branch, the modifier under the control of the Conditional Branch logic selects between the Next Address ROM and the Branch Address ROM codes to enter ROMAR 1. If the specified test is met, the contents of Branch Address ROM are selected and a microprogram branch takes place. If, however, the specified test is not met, the Next Address ROM contents are used and no branch takes place.

To initiate the execution of the next instruction, ROMAR 2 is loaded from the Instruction Start Address ROM which contains all the starting locations in CROM for all the instructions. The next instruction data and its addressing mode is contained in the OP code and X field of each instruction fetched from memory. These two fields (8 bits total) are supplied as an address code to the Instruction Start Address ROM directly from the Memory Read Register (MRR) located on the MAG board. The Instruction Start Address ROM serves as a translator which converts the OP code and X fields of each instruction into a corresponding microprogram address. The Control Instruction Register (CIR) also receives the instruction code from the MRR and is selected to load the source and destination fields of the XFR instruction into ROMAR 2.

External control of the microprogram is achieved by gating these codes into ROMAR 2 during ground testing. Interrupt and start microroutines are initiated by forcing ROMAR 2 to octal 000 or octal 377 and then relinquishing control to ROMAR 1.

4.9.2.3.2.2 Conditional Branching. Extensive conditional branching capability in microprogram enables fast execution of instructions and adds microprogramming flexibility. Complicated algorithms can be performed in hardware (i.e., microprogram) rather than software without the usual penalties of higher utilization rates and larger main memory requirements.

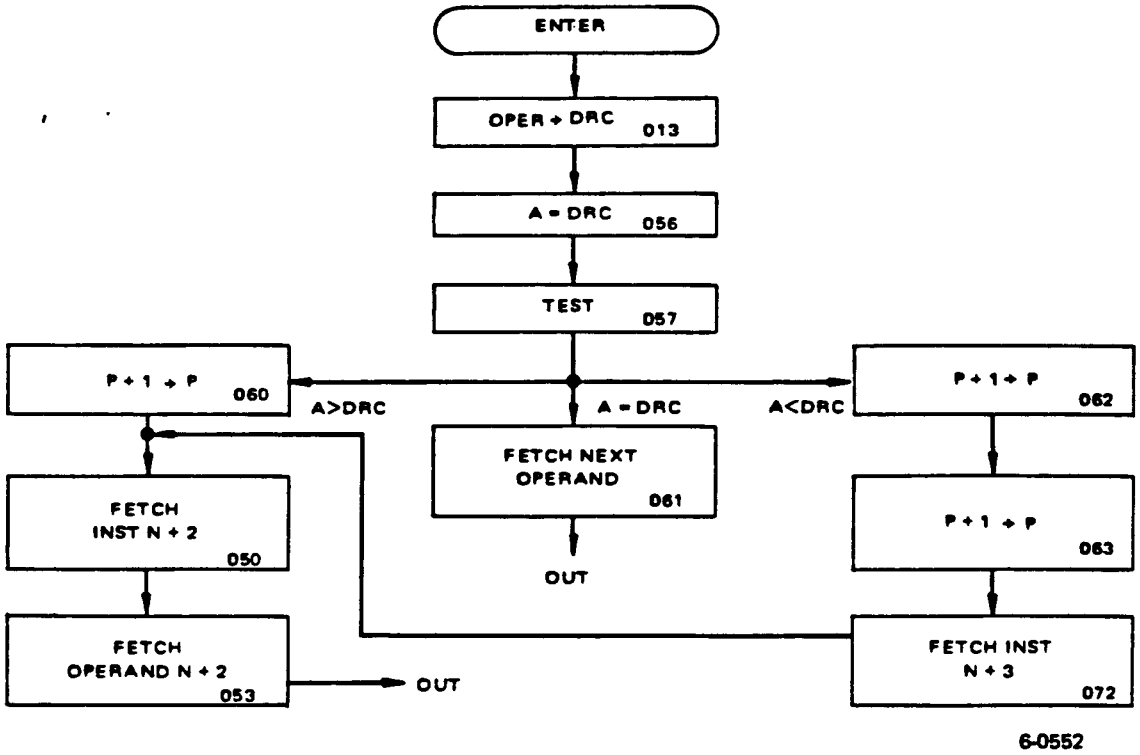


Figure 4.9.2-39. Microprogram Flow, CMA Instruction

4.9.2.3.2.3 Iteration Counter. To conserve microprogram store, an iteration counter as shown in Figure 4.9.2-40 is used to count down machine cycles. During the iterative operations associated with the execution of multiply, divide, and shift instructions, the microprogram is halted at the appropriate EO and the counter is used to time out the desired number of iterations. When the counter overflows, a conditional branch test is made and the microprogram leaves by selecting the next address from the Branch Address ROM.

The counter is initialized, as a function of the operation to be performed, with either fixed hardwired codes or with variable codes derived from the shift instruction N field. After loading, the counter is directed to count down until the all-zero decode gate comes true. This output is continuously monitored by the microprogram branch logic to determine the end of iteration.

4.9.2.3.2.4 Clock Generator. The externally supplied clock of 1.7 MHz from the CIU is further divided down within the CPU as shown in Figure 4.9.2-41.

A ring counter with states 1 through 6 is under the control of the Run/Stop signal and the start and self check circuit. Under normal operation and in flight, the Run signal is always true and the ring counter is running continuously. During ground testing, the Run/Stop signal is manipulated to perform step by step operations. This is accomplished by locking the counter at state 2 whenever the Run signal is false.

The counter can also operate in either of two modes. It can count by 4 or count by 6 as a function of the LEO/NEO signal from the CROM. Long EO (LEO) is required for special operations which demand more time than the basic Normal EO

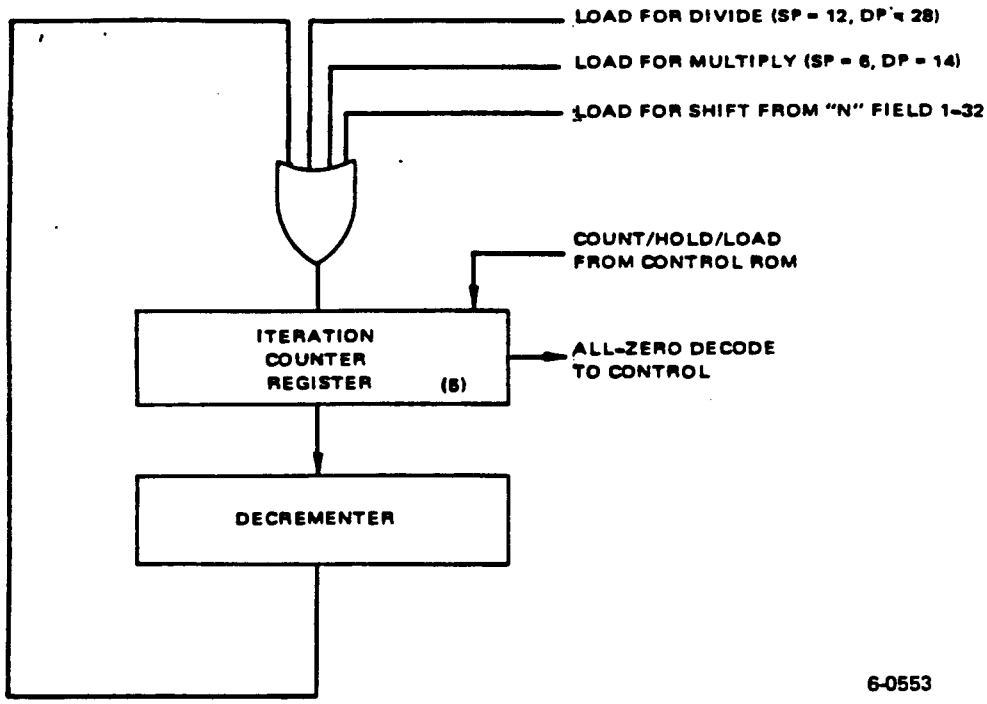


Figure 4.9.2-40. CPU Iteration Counter

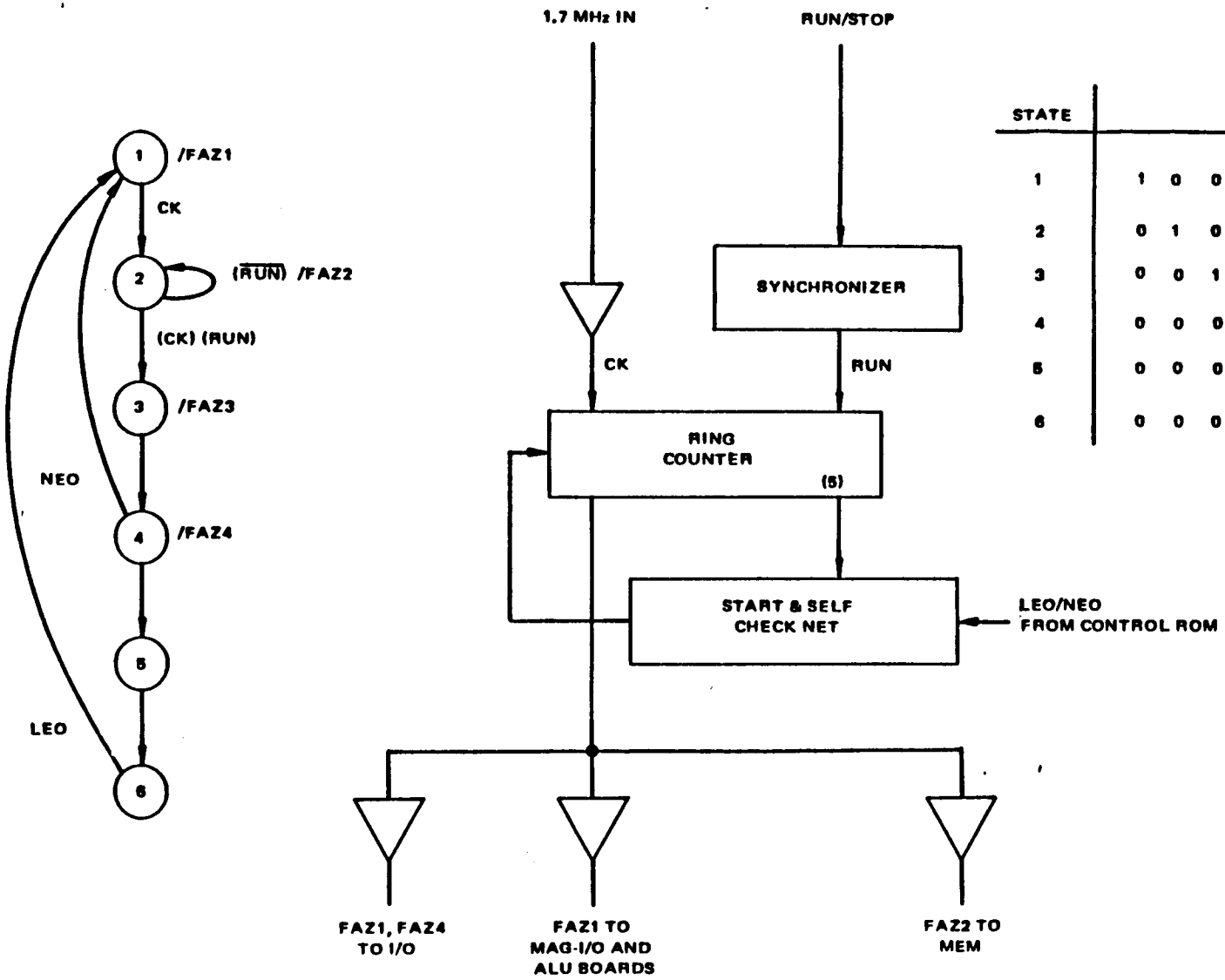
(NEO) of 2.34 microseconds provides. As shown in the flow chart, when in the NEO mode the counter advances through states 1, 2, 3 and 4 and recycles back to state 1. In the LEO mode, the additional states 5 and 6 are added after state 4 and then the counter recycles to state 1. Each additional state increases the period by 585 nanoseconds; a LEO is 50 percent longer than a NEO.

The self check circuit continuously monitors the counter to insure that an improper code is not circulated in the ring counter.

Four clock signal phases are generated for internal and external use. Special isolated and dedicated buffers are used for I/O operations. All internal operations are synchronous with FAZ1 clock with the exception of a special memory inhibit logic which operates during FAZ2. FAZ3 is not used internally and is considered as spare.

4.9.2.3.2.5 Input/Output. The bi-directional I/O bus shown in Figure 4.9.2-42 is used to transmit data and address words from the CPU to the CIU and to receive status and data words from the CIU. Data and address transfers are on a parallel 16 bit binary basis. CIU addresses are distinguished from CIU data by the I/O Alert signal, which is true only when the CPU is transmitting an address code.

The I/O Transfer Out (I/O TOUT) signal is active whenever the tristate drivers on the I/O bus are turned on by the CROM. This signal is used by the CIU to disconnect its own transmission gates from the I/O bus in order to prevent a conflict situation.



STATE						OUT
1	1	0	0	0	0	FAZ1
2	0	1	0	0	0	FAZ2
3	0	0	1	0	0	FAZ3
4	0	0	0	1	0	FAZ4
5	0	0	0	0	1	
6	0	0	0	0	0	

Figure 4.9.2-41. CPU Clock Generator

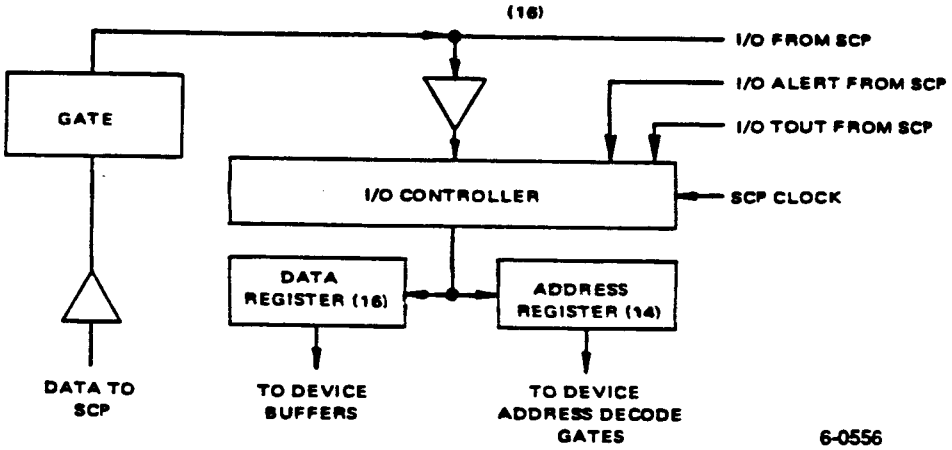


Figure 4.9.2-43. Interface Unit, CIU I/O Section

If the currently active program has the highest priority, the program proceeds without interruption. Otherwise, the system automatically transfers to the highest level demanding priority. When all of the higher demands are satisfied, control returns to the interrupted program, which is continued as before the interruption. In this manner the processor is able to interleave a number of different modules. The lowest priority level (Level 1) is known as the background level and is active only when no other level is interrupting. An external interrupt may not be generated on this level.

When a priority interrupt is honored, the machine logic ensures that the current Program Counter (PC), Status Register (SR), and Interrupt Requests (IQR) are stored in fixed locations in Read/Write (R/W) memory. The selection of the specific memory locations for each of the 16 words within each block is determined by the currently active interrupt level. When a level is re-entered after an interruption, the corresponding PC and SR are retrieved from the R/W memory locations where they had been stored.

During a level change, the hardware determines whether it is a new entry to the routine residing at the new level and the corresponding interrupt mask. There are sixteen 16-bit masks stored in ROM, each of which contains all zeros except for 1 set bit corresponding to a different one of the sixteen processing levels.

Example:	0000	0000	0001	0000	Mask for Level 5
	0000	0000	0001	0101	IQR for Level 5 (Hypothetical)
	0000	0000	0001	0000	Result of "AND" operation

The result is not equal to zero, indicating a return to a previously interrupted routine.

Whenever the level is changed to a new entry, the new PC is loaded from a reserved area in R/W memory and SR is cleared. Note that the clearing of SR initializes the machine to the Double-Precision Mode (DPM) of operation. The programmer is then responsible for establishing the desired mode and saving the contents of other working registers.

4.9.2.3.3.2 Internal Interrupts. Internal error alarms automatically request interrupt at the highest level (Level 16), which is reserved for a routine to deal with errors. These "alarm" interrupts are serviced upon the completion of the current instruction execution.

Apart from the hardware initiated interrupt request in the case of an error alarm, internal interrupts may be requested by the programmer by means of the Operating Mode Change (OMC) instruction, through which any desired combination of bits can be set in the Interrupt Queue Register (IQR). The OMC instruction can also be used to terminate interrupts by resetting the desired combination of bits in the IQR.

4.9.2.3.3.3 External Interrupts. There are 14 external interrupt input lines (E2 through E15), each uniquely associated with one of the CPU priority levels. E15 is the highest priority level which may be externally interrupted; level 16 is reserved for internal routines for error recovery. Requests are initiated by activating an input line to the logical 1 state (+10 V) until the CPU acknowledges it.

The CIU, being the source of the go-between for all external interrupts, contains interrupt enable-disable logic so that individual interrupt lines (E7, E8, E10, E11) can be "locked out" under software control.

The interrupt servicing rate varies as a function of the instruction being executed and is also dependent upon the existing operating mode. The external interrupt servicing delay time of the first instruction of the new priority level requested is 236.34 microseconds.

4.9.2.3.3.4 Interrupt Operation. Block diagrams of the interrupt sections in the CPU and CIU are shown in Figures 4.9.2-44 and 4.9.2-45.

The Interrupt Queue Register (IQR) is used to hold interrupt requests issued under program control via OMC or externally via the CIU. These requests are maintained until the CPU provides servicing.

The Current Level Code register (CLC) is a 4 bit register which holds a binary weighted (8421) code word specifying the priority level currently active (current level in control of the CPU). This code is brought out externally and is also used during microprogram-directed addressing of reserved memory for storing and fetching masks and data associated with the current interrupt level.

The comparator converts the 16 bit IQR word into a 4 bit binary code prior to comparing it with the CLC. When a mismatch occurs (CLC not equal to the Highest Level Requesting (HLR)), a signal is issued to the microprogram address generator logic requesting interrupt servicing immediately after completion of execution of the current instruction.

External requests coming in from the CIU are processed as shown in Figure 4.9.2-45. The interrupt sequencer, unique for each interrupt level, will issue a request to the CPU only if the interrupt mask register is under software control, which can modify its contents via the OPR instruction. Once a request is issued by the interrupt sequencer, it will remain active (state 2) until an acknowledging signal has been issued by the CPU (software). This arrangement protects against spurious external requests and dc type failures at the requesting source.

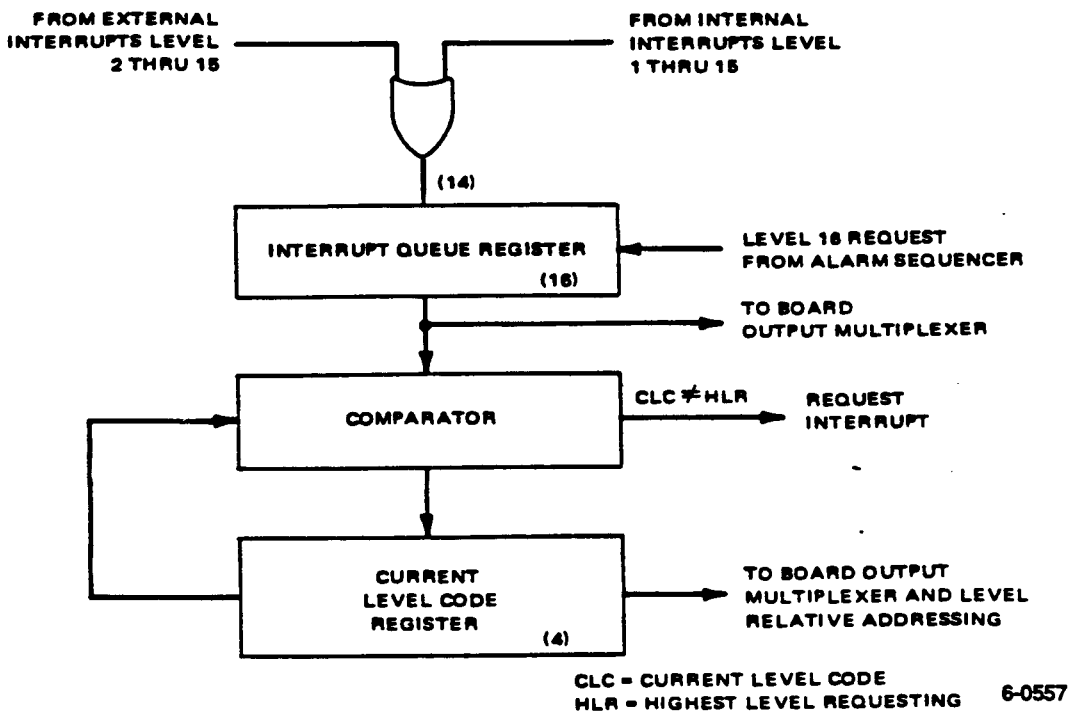


Figure 4.9.2-44. CPU Priority Interrupt Section

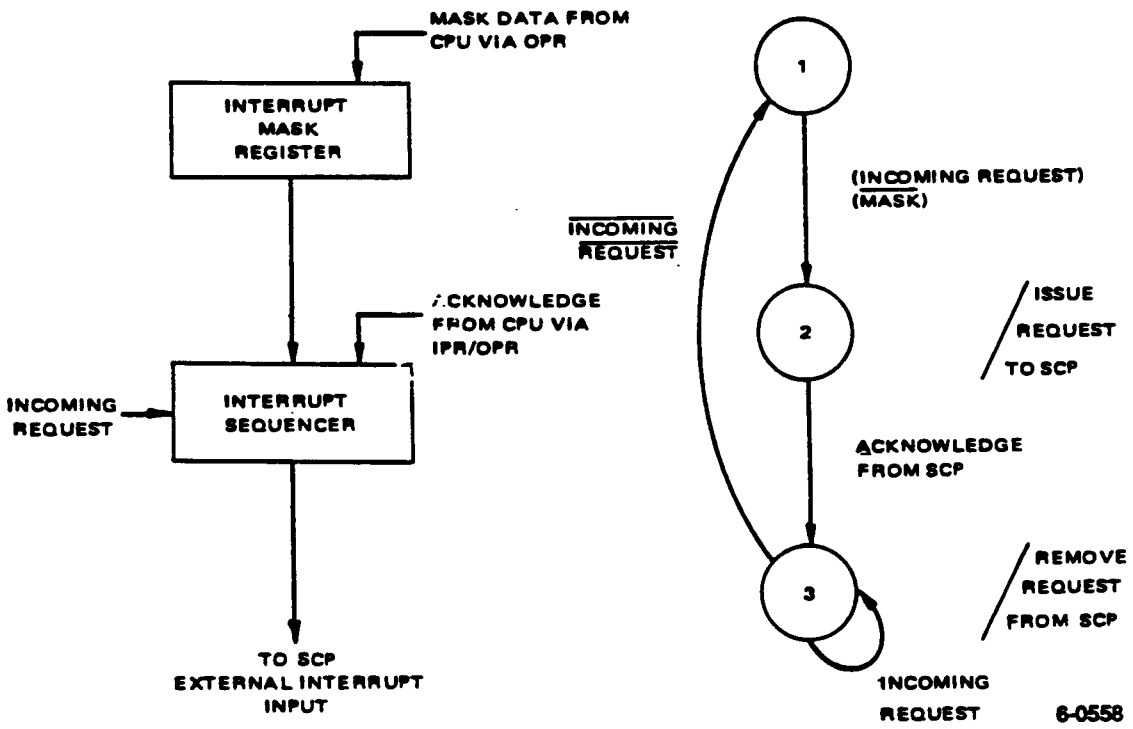


Figure 4.9.2-45. CIU Interrupt Logic

4.9.2.3.3.5 Interrupt Microprogram Routine. During interrupt servicing, the CPU enters reserved memory for the purpose of fetching masks and data and storing the PC, SR, and IQR for later retrieval. The address codes needed to access the memory are generated from two sources of data; a CROM field specifically dedicated to this function known as the EMIT field, and the CLC binary-weighted 4 bit number. Each 16 bit address code needed for main memory access is formed by concatenating bits from the EMIT and CLC. The CLC bits are in the 4 least significant positions so that the 16-bit address code is modulated by the CLC in accordance with the operating level (also known as Level Reference). This arrangement allows for using a common interrupt routine for servicing all interrupt levels (except Level 16).

The microprogram services interrupts after leaving normal program execution in accordance with the flow chart shown in Figure 4.9.2-46. The entry into this sequence, which occurs at the end of current instruction execution, may be due to an alarm condition or normal interrupt request processing. A test is performed to establish the reason for entry and to branch accordingly. In either case the IQR and corrected Program Counter (which has advanced due to instruction overlap) are stored in reserved memory.

Considering the normal interrupt case, the next step is to store the Status Register (SR) and update the current level store to the new operating level. At this point the microprogram is ready to fetch the corresponding IQR and test it for previous interruptions. If the bit associated with the new level is retrieved as a 1, it denotes that the CPU has been previously interrupted to go to a higher level before completing the required processing and therefore at this time it is returning to complete the task. On the other hand if the bit is a 0, it means that this is a new entry, there has not been a previous interruption while at this level, and therefore the CPU is to take its starting location from the block of reserved memory assigned to this function.

For the re-entry case, the SR is retrieved from memory and placed in the Status Register. For the new entry situation, the SR which has been previously cleared is left in the cleared state. The last block in the flow chart deals with setting up the pipeline for the instruction overlap system and finally the microprogram returns to normal programming. The flow for an alarm condition is discussed in the alarm section.

4.9.2.3.3.6 Interrupt Level 16 (Alarm Mode). This level is reserved for processing either error conditions or the initialization routine activated by the Reset pulse command.

4.9.2.3.3.7 Error Logic. A section of the SR shown in Figure 4.9.2-47 is used for accumulating error conditions and for signaling an alarm sequencer to request entry into Level 16.

Five types of error conditions will set corresponding bits in the SR. These are:

- Memory Double Error Detected
- Memory Address
- ALU Overflow
- Illegal XFR Source Code
- Illegal XFR Destination Code

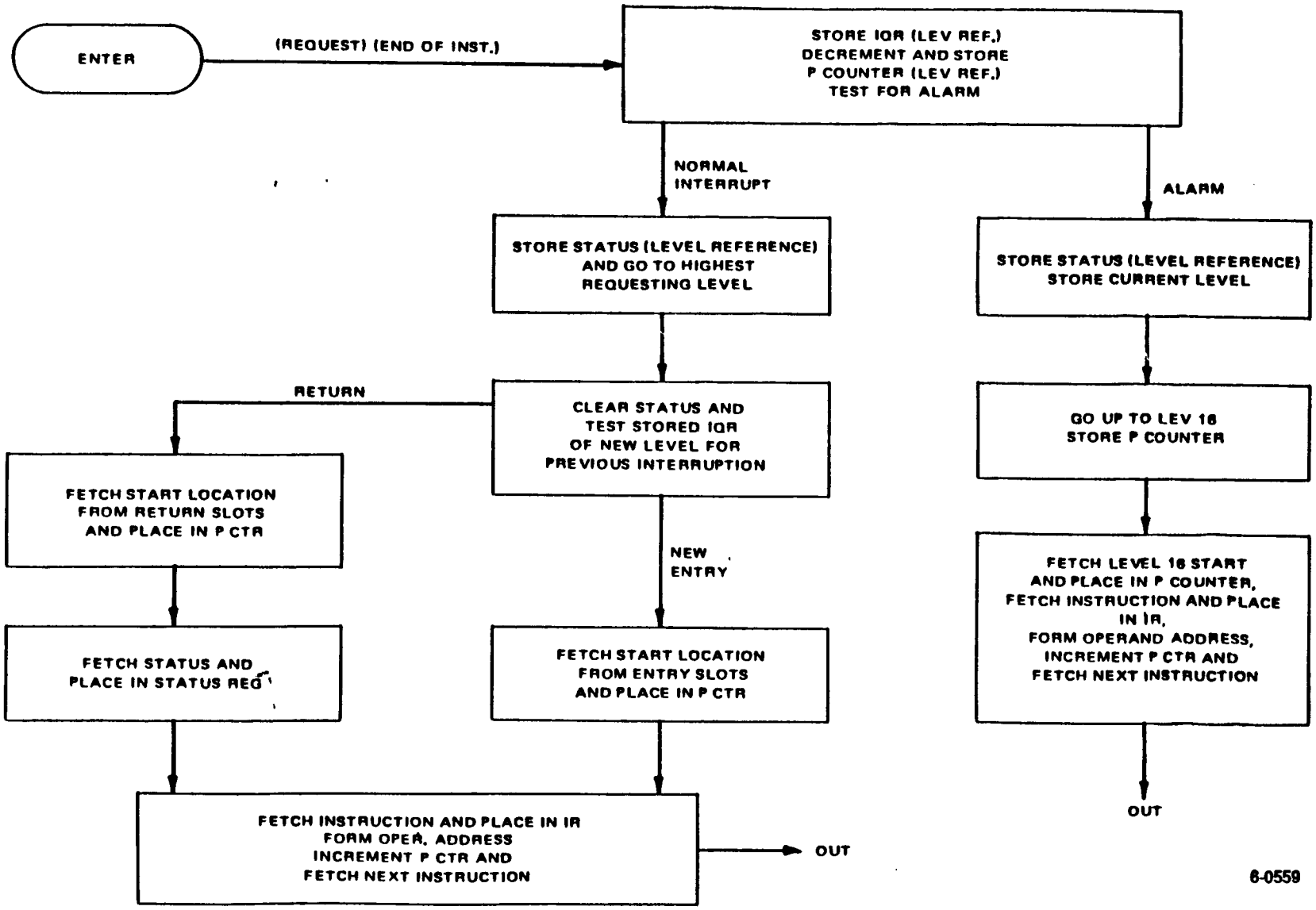


Figure 4.9.2-46. Alarm/Interrupt Routines

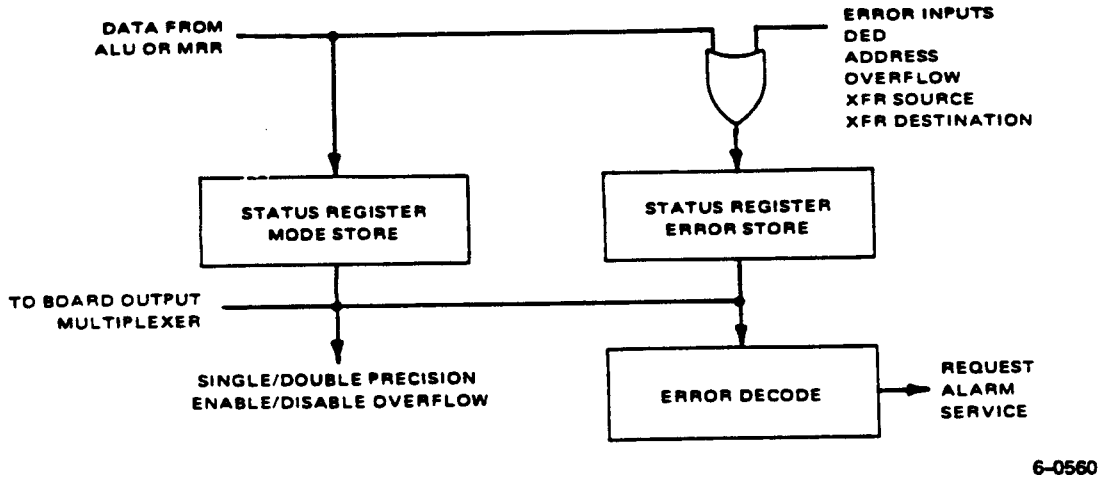


Figure 4.9.2-47. CPU Status Register

ALU overflow is conditioned by the existing mode (i.e., overflow error can be disabled or enabled by programming by setting the assigned bit in the mode store). Once any of the bits in the error store is set, the error decode logic generates an alarm request to the alarm sequencer.

4.9.2.3.3.8 Alarm Sequencer. The state diagram for this sequencer is shown in Figure 4.9.2-48. The normal inactive state is state 1. The sequencer will reside at this state as long as the system is not at Level 16.

Exit from state 1 into state 2 or state 3 occurs either as a response to an error condition or the Reset Pulse command (RST PLS).

In response to an error condition which has been stored in the SR, a request alarm signal is generated by the error decode logic and if the CPU is not at Level 16 already, the sequencer will travel from state 1 to state 2 where it will await the completion of execution of the current instruction. This insures that orderly transitions from the normal instruction sequencing into the interrupt routine takes place. While at state 2 the sequencer generates a Level 16 request to the microprogram address generator, which in turn will respond at the end of the current instruction cycle.

Once the microprogram shifts to the interrupt routine, shown in Figure 4.9.2-46, a test is performed to establish cause of entry which could be either normal interrupt or alarm.

After this test, the sequencer moves on to state 3 where it sets bit 8 in the SR to signify that the system is at Level 16. At Level 16, the memory protect feature is defeated and the CPU can execute the error routines stored in main memory. New error conditions accumulated at Level 16 will not initiate requests for alarm.

The sequencer will remain at state 3 until an OMC or XFR instruction clearing bit 8 of the SR is executed by the program. At that time the sequencer will return to state 1 via transient state 4 and the Level 16 bit in the IQR will be

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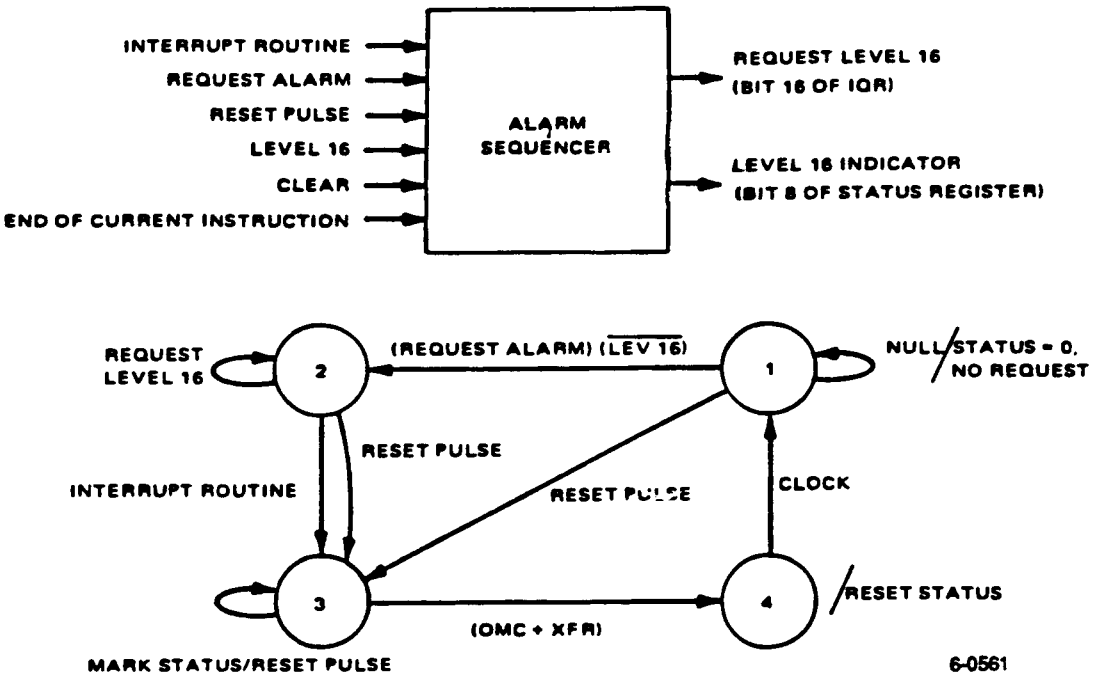

Figure 4.9.2-48. CPU Alarm Sequencer

cleared. This will cause an interrupt request which will be serviced by the interrupt routine and the CPU will drop to the next highest level requesting service.

As discussed above, this sequencer is also used for initiating entry to Level 16, in response to the Reset pulse. In this case, the sequencer proceeds to state 3 immediately, since an orderly transition is not important. Once at state 3 it marks the SR while the Reset pulse causes the microprogram to enter a special routine called START, shown in Figure 4.9.2-49.

The START routine causes the CPU to lock in place while deactivating the I/O bus and await the removal of the Reset pulse. Once this happens the system fetches the bootstrap program from ROM and proceeds to execute it.

4.9.2.3.3.9 Alarm Microprogram Routing. The alarm microprogram routine shown in Figure 4.9.2-46 was previously discussed with respect to interrupt processing. The alarm portion of the flow chart is entered after testing the reason for entry, storing the IQR, and updating the P counter and storing it as well. The next step calls for storing the SR and CLC. The storing of the CLC and the P counter is performed to provide analysis tools for the error handling routines of Level 16. These stored words provide information on the level and the instructions that caused the alarm condition.

The last step of the alarm routine includes all the operations necessary to "prime" the "pipeline" for the instruction overlapping.

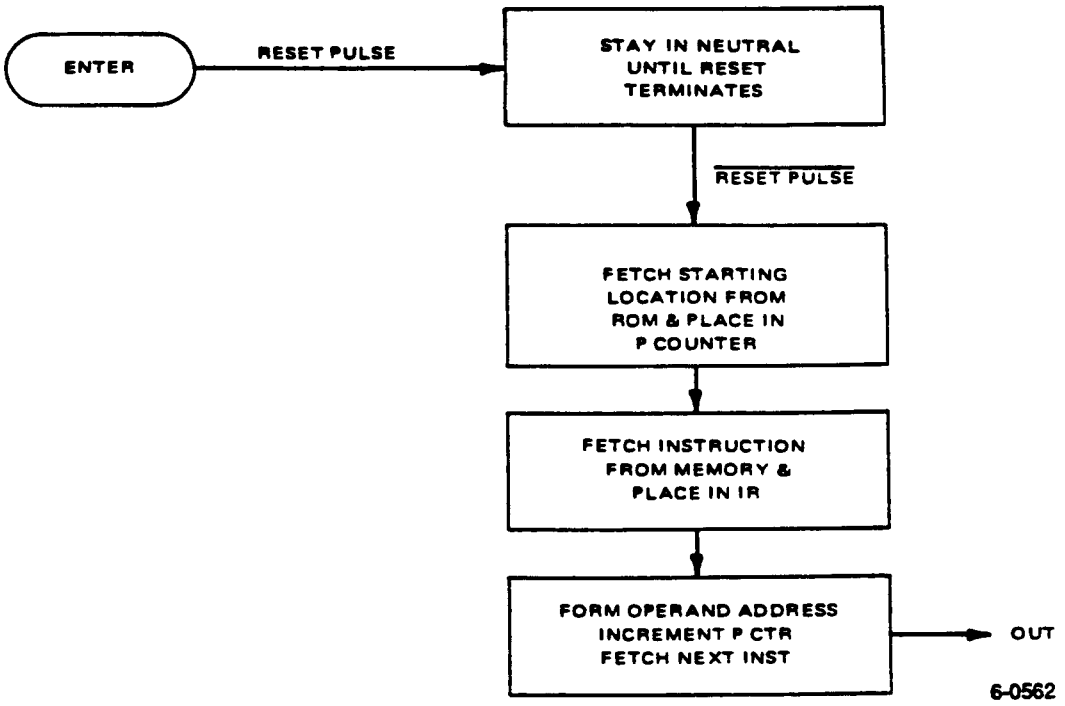

Figure 4.9.2-49. START Microprogram Routine

4.9.2.3.4 Memory Address Generator

This section of the CPU is charged with fetching instructions and operands from memory, loading of new programs and data into the memory, and performing various timing and control operations for the main memory. Figure 4.9.2-50 contains the main functional blocks, which are located on the MAG-I/O board. The remaining functional blocks associated with memory control are on the 16K R/W board and are described in Section 4.9.2.3.6.8.1.

4.9.2.3.4.1 <u>MAG Registers and Miscellaneous Logic</u>

4.9.2.3.4.1.1 <u>Instruction Register (IR)</u>. The Instruction Register is a 16 bit register used to store instructions. Each Instruction contains three fields:

1. Operation Code (OP Code) field (5 bits), which defines the operations to be performed by the CPU such as ADD, SUBTRACT, SHIFT, etc.

2. X field (3 bits), which in general defines operand addressing mode to be used in conjunction with this instruction.

3. D field (8 bits), which in general comprises a number to be added to one of 4 registers (specified by the X field) in order to form the address of the operand associated with this instruction.

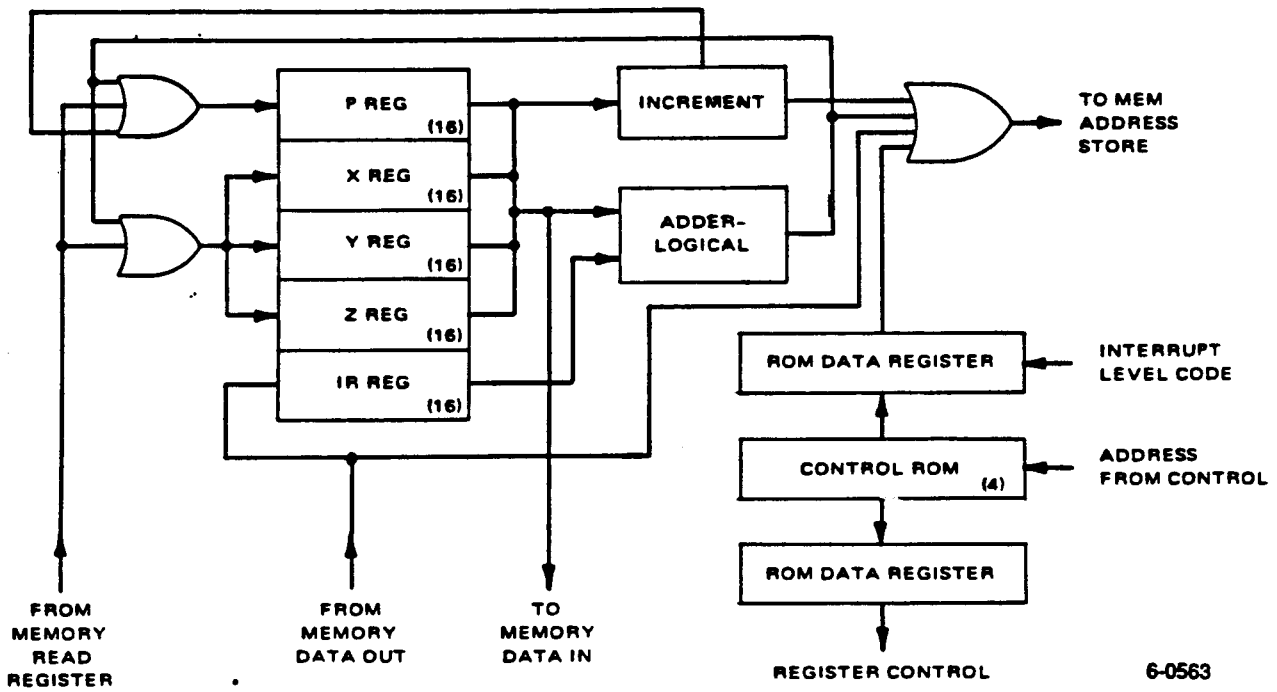

Figure 4.9.2-50. CPU Memory Address Generator

4.9.2.3.4.1.2 Index Registers (XX, XY, XZ). Three 16 bit Index Registers are available to the programmer for use in operand fetching or as software loop counters. Each of these registers can be loaded from memory, incremented, decremented, and exchanged with other working registers.

4.9.2.3.4.1.3 Program Counter (PC). The Program Counter is a 16 bit register and is used primarily as the instruction location register. It is also available to the programmer for use in addressing operands (PC relative). This register is incremented by the microprogram with each instruction execution cycle in order to point at the location of the next instruction in memory. Branch instructions are executed by disrupting the sequential updating of the PC and replacing its contents with a new value.

4.9.2.3.4.1.4 MAG Adder-Logical. The MAG adder-logical network generates operand addresses and also performs arithmetic and logical operations during BUI and MXS instruction execution. An all-zero state detector output is transmitted to the CPU control section for monitoring during microprogram conditional branching.

4.9.2.3.4.2 Operand Addressing Modes. Four modes of memory addressing are possible for all instructions which refer to memory, except the Operating Mode Change (OMC) instruction which uses direct PC relative addressing only. The four modes are direct PC relative, indirect PC relative, direct indexed, and indirect indexed; the choice of the four modes and the selection of index register depend on the contents of the X field of the instruction (See Table 4.9.2-17).

TABLE 4.9.2-17. MEMORY ADDRESS MODES

X Field Bits 5	6	7	Addition Required To Form Address Value (bits)	Addressing Mode
0	0	0	(PC) 0-15 + (D) 8-15	Direct PC Relative
1	0	0		Indirect PC Relative
0	0	1	(XZ) 0-15 + (D) 8-15	Direct Indexed with Z
1	0	1		Indirect Indexed with Z
0	1	0	(XY) 0-15 + (D) 8-15	Direct Indexed with Y
1	1	0		Indirect Indexed with Y
0	1	1	(XX) 0-15 + (D) 8-15	Direct Indexed with X
1	1	1		Indirect Indexed with X

(D) is the D field of instruction
(PC) is the Program Counter
(XX) is the X Index Register
(XY) is the Y Index Register
(XZ) is the Z Index Register

All memory addresses are computed as 16 bit numbers. If the computed address value exceeds the connected memory capacity, the address error bit of the Status word will be set and an interrupt initiated.

In the direct addressing modes, the memory location specified by the address value of the table is the effective memory location (i.e., the location of the operand referenced by the instruction). In the indirect addressing modes, the memory location specified by the address value of the table contains an explicit 16 bit address which specifies another memory location which is the effective memory location.

Note that all address values are formed by addition to the instruction D field. One or more of the 3 index registers may be used by the programmer as "address page pointers". Each address "page" comprises a block of 256 locations. The PC Relative modes may be considered to provide a "current page" of memory with boundaries which automatically advance with the Program Counter.

4.9.2.3.4.3 MAG Operations. As shown in Figure 4.9.2-50, there are four paths of entry into the Memory Address Store (MAS). Incremented values of the P register are sent to the MAS for the purpose of fetching instructions. The Adder Logical network output, also connected to the MAS, provides addresses of the operands to be fetched.

The third path is from the memory output directly (without staticizing in a register). This is used during the indirect cycle mode where a first pass at the memory does not produce an operand but an address of an operand. This code is placed immediately in the MAS and the memory is addressed again to fetch the operand.

The fourth path into the MAS is from the ROM data generator. This path is selected whenever the microprogram wishes entry to main memory working locations. The actual address code for microprogram addressing of main memory is normally derived from the CROM field known as the EMIT. This field is occasionally modified by the interrupt level code (see the Control section) to generate interrupt level preference addressing used during interrupt and alarm servicing. Table 4.9.2-18 lists these memory locations.

4.9.2.3.4.4 Read Only Memory (Bootstrap ROM). he bootstrap ROM is located on the MAG-I/O board. ROM is configured using 2 ROM chips of 256 X 16 bit size. The ROM code includes the bootstrap loader program, interrupt masks, and data constants. This code is used by the CPU during power on initialization and during many microprogram service routines. The ROM has a decimal address range of 65344-65416.

TABLE 4.9.2-18. MICROPROGRAM ADDRESSED MEMORY LOCATIONS

Address (Decimal)	Usage
0-15	P Counter, stored when exiting Levels 1-16 on interrupt
16-31	IQR, stored when exiting Levels 1-16 on interrupt
32-47	Status Register Step, stored when exiting Levels 1-16 on interrupt
48	Level Active Code, stored when entering Alarm Mode
49-67	Working storage area reserved for hardware use
68-127	Working storage area reserved for software use
128-143	Starting locations for new entry into Levels 1-16
144-255	Unassigned
65280-65295	Constants
65296-65311	IQR masks
65312	Initial P for Bootstrap program
65313	Zero
65314-65315	MAXPOS Constant used for multiply and divide
65316-65343	Constants
65344-65535	Bootstrap ROM program

All logical instructions such as AND, OR, XOR, IOR are performed on operands residing in A and DRC with the results stored in A. Arithmetic operations such as ADD and SUBTRACT are also performed on operands residing in A and DRC with results stored in A.

Multiply operations are performed with the multiplier initially residing in M/Q, the multiplicand residing in DRC, and the A is initially cleared. During the multiplication process the A contains partial products which are gradually shifted (serially) into the M/Q to displace the multiplier and to finally form a double length product residing across A and M/Q.

Divide operations are performed with the divisor residing in DRC and a double length dividend initially stored across A and M/Q. During the division process the quotient is formed in the M/Q while displacing the dividend as it is shifted leftward into the A. At the end of the division process the A contains the remainder and the M/Q contains the quotient.

The ALU is also used for logical operations under microprogram control (invisible to the program) during OMC and interrupt associated operations.

During single precision mode the least significant half of each register does not participate in any operation. Special hardware (not shown in Figure 4.9.2-51) disables certain CROM functions during multiply to provide register control based on multiplier data bits in the M/Q.

Adder overflow detection logic is enabled under microprogram control during all arithmetic operations where legitimate overflow can occur. When an overflow situation occurs, a bit in the status register is set.

Two multiply instructions are included in the instruction repertoire. The cumulative multiply (MPC) instruction is useful for sum of products type calculations of the form X = A B + C D + E F + ---. The Multiply Single (MPS) instruction restores the multiplier to the M/Q register, thus allowing successive multiplications by a constant k without having to load the M/Q after each multiply operation.

4.9.2.3.5.2 Multiply Algorithm. Multiplication is accomplished by means of a bit pair algorithm. By inspecting the least significant two bits of the multiplier, the multiplication is completed in half the time required by a single bit algorithm. The product is calculated by accumulating a running subtotal of the partial products as they are calculated. Skewing of the partial products is accomplished by shifting the accumulated sum of partial products two bits to the right and simultaneously adding the next partial product.

The multiplicand (M) is held in DRC. Two times the multiplicand (2M) and minus the multiplicand (-M) are formed temporarily as required under hardware control prior to entering the adder. The MQ holds the multiplier and is shifted two places to the right after examining each pair of least significant bits. The accumulator contents are shifted two places to the right within the Adder, and the least significant two bits of the accumulator are shifted into the most significant two bits of the M/Q.

A marker flip-flop (FF_m) is employed during execution of the multiply algorithm. The state of FF_m and the states of the least significant two bits of the M/Q register determine the addend (M, 2M, or -M) and the next state of the marker flip-flop. The augend, always in the accumulator, is shifted right two places. Table 4.9.2-19 summarizes the choices for the least significant 7 or 15 pairs (single or double precision) of M/Q bits.

4.9.2.3.5.3 Divide Algorithm. Division is accomplished by means of a "non-performing" division algorithm; this involves trial subtraction of the divisor from the dividend. The decision to complete or not complete the operation is based on a test of the sign of the difference. The accumulator holds the most significant half of the dividend; the M/Q register holds the least significant half. The divisor is held in data register C.

A trial operation consists of shifting the left source of the adder one place to the left (2 ACC) and subtracting the divisor. If the difference is positive, a quotient bit of "1" is shifted into M/Q and the difference is stored in the accumulator. If the tests indicates "non-performance", the result is not stored and the ACC is shifted internally one place to the left while the M/Q receives a "0" quotient bit with each shift. The most significant M/Q bit (M/Q_0) is shifted into the least significant bit of the accumulator. All quotient bits (including sign), formed one at a time, are injected into the M/Q via the least significant end.

4.9.2.3.6 Main Memory

4.9.2.3.6.1 Program and Data Memory. The main memory provides storage for data, control words, and instructions. The memory is random access and word addressed, 32K words long with each word containing 22 bits. The memory is comprised of a basic section which performs all necessary logic and interfacing functions, and a number of modular sections which perform the actual storage. The modular organization allows the memory to be configured with optimal memory capacity for a variety of applications without making basic changes in the design.

TABLE 4.9.2-19. HARDWARE MULTIPLY

MQ_{2LSB}	00	00	10	11	00	01	10	11
$(FF_m)n$	0	0	0	0	1	1	1	1
Addend	0	M	2M	-M	M	2M	-M	0
$(FF_m)n+1$	0	0	0	1	0	0	1	1

MQ_{2LSB} = the least significant bits of the M/Q register
$(FF_m)n$ = current state of marker flip-flop
$(FF_m)n+1$ = next state of FFm
M = Multiplicand
Augend = 1/4 A for all addends

The specific memory configuration is shown in Figure 4.9.2-52.

The memory elements are of 2 types: the read and write (R/W) sections use monolithic Random Access Memory (RAM) chips with each RAM chip containing 4096 X 1 bits; the Read-Only Memory (ROM) chips form the bootstrap loader function located in the MAG-I/O board. In the R/W memory, a 6-bit word parity is generated for each incoming word and is stored with each word in memory as bits 17 through 22; whenever a word is read from RW memory, it is checked to ensure that its parity word is still correct. If a single error is detected the data word is corrected and flagged. If a double error is detected, the Level 16 Alarm is initiated. Parity does not apply to ROM; the program bit configuration is fixed at manufacture and no real-time checking is needed thereafter.

Each word location in the memory is identified by a unique "address" word containing 16 significant bits; thus, a maximum of 2^{16} or 65,536 words may be addressed. Word locations are consecutively numbered starting with 0.

The processor requests memory access by activating a Read or Write signal line and simultaneously placing an address on the Address bus. For a double precision access, the memory will automatically read or write two words; one at the specified address (which must be even), and the second at the next higher address. Note that in the double precision mode some memory accesses (e.g., instruction fetch) are done in single precision.

4.9.2.3.6.2 Reserved Memory. Table 4.9.2-20 specifies the areas of R/W memory reserved for special use.

4.9.2.3.6.3 Write Protected Memory. Options are open for provision of write protected memory in blocks of 4096 words. There is an interface line called MEPROV which disconnects the write protection. Each group of 4096 R/W memory locations may be connected in one of three ways to constrain the CPU initiated write access to it:

1. Unprotected. CPU write may be enabled for all purposes.

2. Program Protected. CPU write may be enabled only for storage of special data in reserved locations. Falling into this category are certain interrupt data, level 15 and 16 programming applications, and memory load sequences using the MEPROV (write protection) external signal.

3. CPU Protected. This is an option which is the same as 2 above, except that the MEPROV signal cannot be used to enable an CPU write.

The R/W memory map showing the protected and unprotected areas is shown in Table 4.9.2-21. The ATN-HIJ CPU will be configured as item 1 above, with MEPROV signal set to unprotected.

4.9.2.3.6.4 Memory Reconfiguration Feature. The two 8K word modules in the lower address range are interchanged in their address space in response to an external input signal Memswap/Memnormal. The normal configuration assigns addresses 0000_H through $1FFF_H$ to the slot J5 module and addresses 2000_H through

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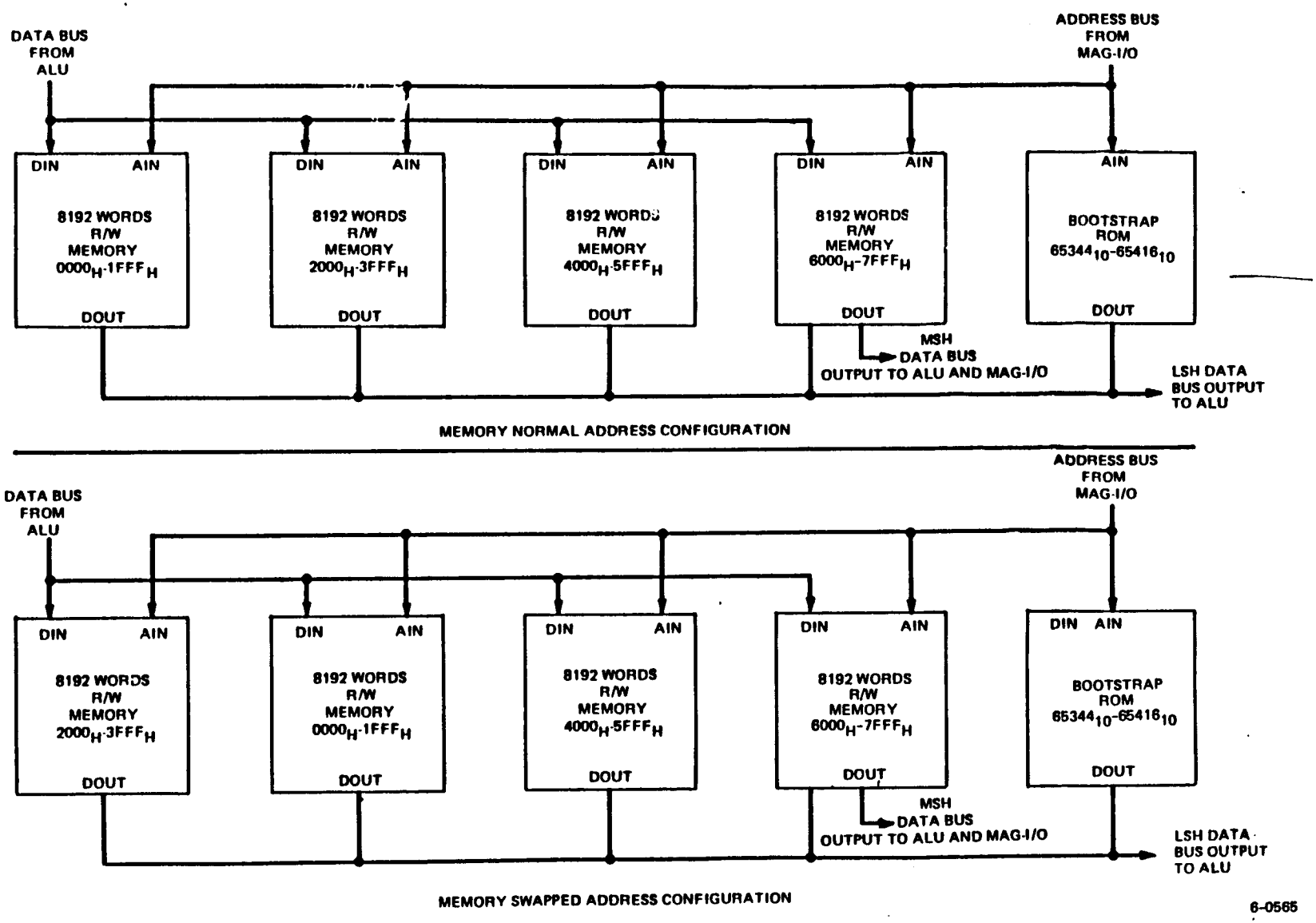

Figure 4.9.2-52. Memory Subsystem Block Diagram

TABLE 4.9.2-20. R/W MEMORY RESERVED ADDRESSES

Address (Decimal)	Usage
0-15	P's stored when exiting levels 1-16 on interrupt
16-31	L's stored when exiting levels 1-16 on interrupt
32-47	S's stored when exiting levels 1-16 on interrupt
48	Level active stored (LAS) for an alarm exit
49-67	Working storage area reserved for hardware use
68-127	Reserved Software temporaries
128-143	Entry P's for levels 1-16

TABLE 4.9.2-21. MEMORY ADDRESS SPACE MAP

Memory Board Slot	Assigned Memory Blocks	Assigned Memory Segments	Assigned Memory Addresses (Normal Configuration)		Memory Protection Provided
			Decimal	Hex	
	0	1	0-4095	0000-0FFF	Yes
0		2	4096-8191	1000-1FFF	No
	1	3	8192-12287	2000-2FFF	Yes
		4	12288-16383	3000-3FFF	No
	2	5	16384-20479	4000-4FFF	Yes
1		6	20480-24575	5000-5FFF	Yes
	3	7	24576-28671	6000-6FFF	No
		8	28672-32767	7000-7FFF	No

$3FFF_H$ to the slot J4 module; the swapped configuration simply reverses these address assignments. The Memswap Memnormal input levels may change at any time, but reconfiguration occurs only when a Reset pulse is applied; the reconfiguration therefore is defined by the level of the Memswap/Memnormal input signal at the time of the Reset pulse. A logic 0 (Ground) is defined as Memnormal.

4.9.2.3.6.5 Error Conditions. The CPU is able to detect a parity error or an address error condition during instruction retrieval and execution.

4.9.2.3.6.5.1 R-W Memory Parity Error Detection. Each 16K R-W Memory module is functionally divided into blocks of 8192 words and each block is further functionally divided into segments of 4096 words. The two 4K segments are assigned addresses such that the even-numbered addresses (LSB=0) of the 8K block are contained in one segment designated the most significant half, and the odd-numbered addresses (LSB=1) are contained in the other segment designated the least significant half. These 4K segments are not constrained to be identical to the 4K segments used for write protection.

During a write operation, the R-W module generates and stores six parity check bits with each single precision word written to the module (see Figure 4.9.2-53). Double precision words shall be stored as two single precision words in contiguous memory addresses and therefore have six parity check bits stored with their most significant half (MA15=0) and six parity check bits stored with their least significant half (MA15=1). During a read operation, the R-W module generates six new parity check bits for each single precision word read from the module. The module compares the read-generated check bits with the stored (write-generated) check bits. The results of this comparison are used to correct a single bit parity error in the read word prior to its insertion onto the data bus. If the comparison results indicate that more than one stored bit is in error, the module activates its multiple parity error flag to signal Alarm Mode entry and for inclusion in the ST. In addition, the memory error control logic has the capability to activate the multiple parity error flag when a single parity error is detected. This capability is controlled by the ALOE/ME SEL input signal. Selection of this function is reserved for ground testing.

The CPU provides telemetry interfaces to the TIP which indicate the last location, by block number and odd or even address, of any parity errors.

4.9.2.3.6.5.2 Memory Address Error. An address error interrupt occurs when an instruction fetch or a read or write operation specifies an odd address when an even address is required, or specifies a memory location that does not exist in the connected hardware, or when a write operation specifies a ROM location or specifies a write protected memory location unless initiated by level 15 or 16 write operation. An instruction fetch address error can occur in conjunction with any instruction. Even data addresses are required in double precision mode for ADD, SUB, ADM, MPS, MPC, DVD, AND, IRO, XOR, CMA, CML, LDA, STA, LMQ, and SMQ. A data read address error can occur with all instructions except for the BUI, MXS, SHF, and XFR. A data write address error can occur with an ADM, DMB, SMQ, STA, and STP.

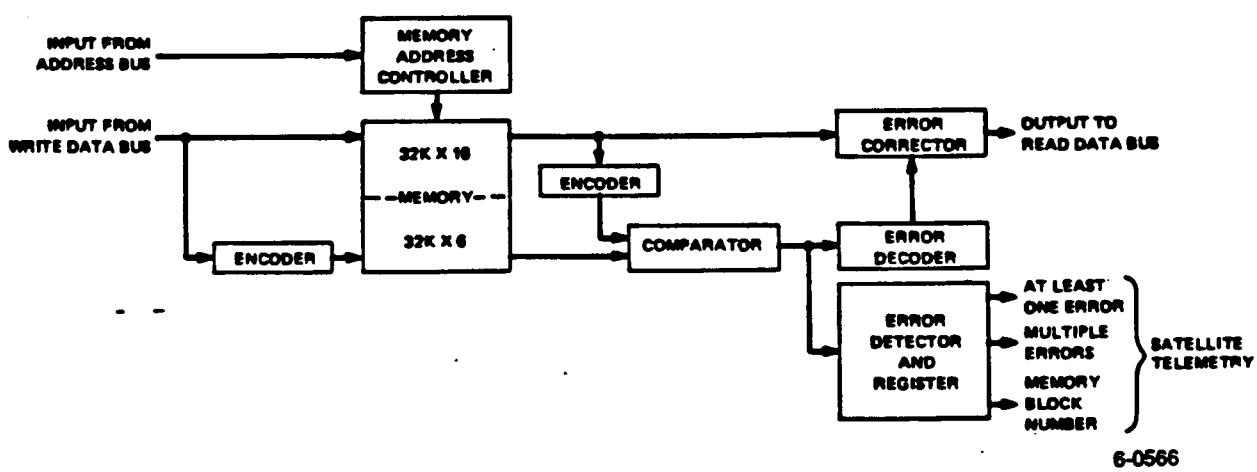

Figure 4.9.2-53. R-W Memory Correction Diagram

4.9.2.3.6.6 Memory Address Store. The Memory Address Store (MAS) is a 16 bit register used to staticize the addresses prior to driving the memory modules.

4.9.2.3.6.7 Memory Read Registers. The memory read registers are two 16 bit registers used for collecting outgoing memory data. These registers synchronize the data to the phase 1 clock prior to transmitting it to the control and MAG section registers.

4.9.2.3.6.8 Memory. An interface diagram of the memory is shown in Figure 4.9.2-54. The memory contains two 16K boards; the basic storage elements are 4096 X 1 RAMs. Each memory word consists of 16 data bits and 6 parity bits.

Data to be stored enters the memory and error correction log via the write bus (WB0-WB31). Input control signals SLT0 through SLT3 are used in conjunction with the address bus to select the appropriate board.

Access to the R/W memory can be either in a Single Precision Mode (SPM) or in a Double Precision Mode (DPM), depending on the level of input signal STSP.

The R/W memory protection feature inhibits any write operations within the address space of protected memory segments (each segment has 4096 word locations). Any attempt to write into protected memory is checked to ascertain if the Memory Protect Override (MEPROV) feature is active, or if the CPU is operating at level 15 or 16. If none of these conditions are true, the write operation is aborted and an alarm condition flag is set in the CPU status register. Input signals, WEN_i, generated on the harness board specify which R/W memory segments are protected.

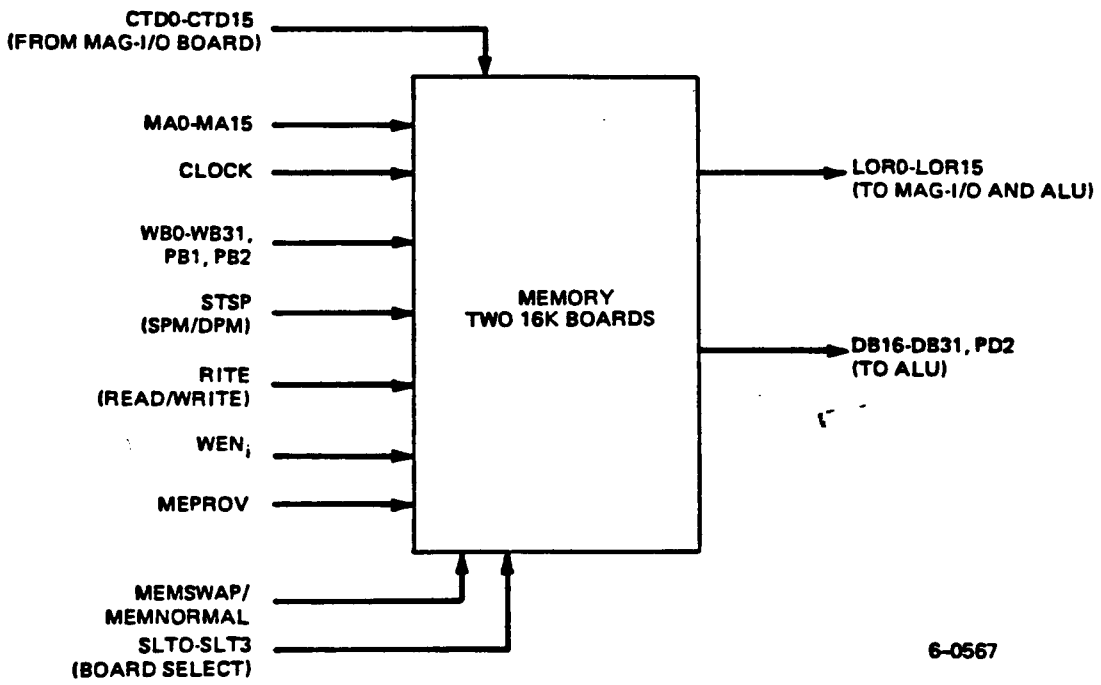

Figure 4.9.2-54. Interface Diagram of the Memory

The Memswap/Memnormal signal is associated with the memory reconfiguration capability. The LOR 0-15 bus transmits Most Significant Half (MSH) or Least Significant Half (LSH) data to both the MAG-I/O and ALU boards. Data bus output (DB16-DB31, PD2) from the LSH of the memory is sent to the ALU during double precision operations.

4.9.2.3.6.8.1 16K Read/Write (R/W) Memory Board. The 16K R/W module uses 88 monolithic static Random Access Memory (RAM) chips (4096 X 1 organization) as the basic storage elements. These are arranged as four blocks of 4096 X 22. Each word location contains 16 data bits and 6 syndrome bits for error detection and correction.

The board select logic decodes the most significant bits of the address bus to establish whether access is desired into this segment of the memory. The remaining address bits (except for bit 15) are staticized in the Memory Address Store (MAS). The outputs of this register drive the RAM input address lines. Specific block selection is performed by the chip enable decoder by decoding of address bus inputs MA3-MA4. These signals are buffered and sent to the Chip Enable (CE) inputs of the RAMs. Write protect decode logic inhibits any attempt to write in the address space of the protected memory segments.

Strobe generating logic accepts the read/write (RITE) signal from the CPU along with the memory segment protection information from the write protect logic. It generates outputs (ST1-ST8) which drive R/W lines of the RAMs. The strobe pulse is inhibited when a write operation into a protected segment is attempted.

The MSH/LSH decode logic uses the MAS15 output and its complement from the MAS register to generate the memory data output control signals Select Left (SEL) and Select Right (SER). These signals control the operation of the tristate output drivers. The Data Bus (DB8-DB31, PD1, PD2) is wire-tied to the corresponding outputs from the other memory boards.

4.9.2.4 Signal Conditioning Unit

The Signal Conditioning Unit (SCU) provides interface signal conditioning between the Ascent Phase Equipment and the satellite portions of the Integrated Spacecraft System (ISS), as shown in Figure 4.9.2-55. In addition, the SCU performs the function of power switching for internal circuits, for the Controls Interface Unit (CIU), for the momentum unloading coils, and for the Integrated Spacecraft System (ISS) Electro-Explosive Device (EED) power buses. The SCU also provides umbilical telemetry power conditioning and resistor current limiting for the RCE pressure transducers.

Three basic types of signal-conditioning circuits are provided in the SCU:

1. Drive conditioning circuits, which convert low level control signals to medium power output signals suitable for driving momentum torquing coils, relay coils, heaters, or solenoid coils at a level of 1.5 amperes or less at +28 volts.

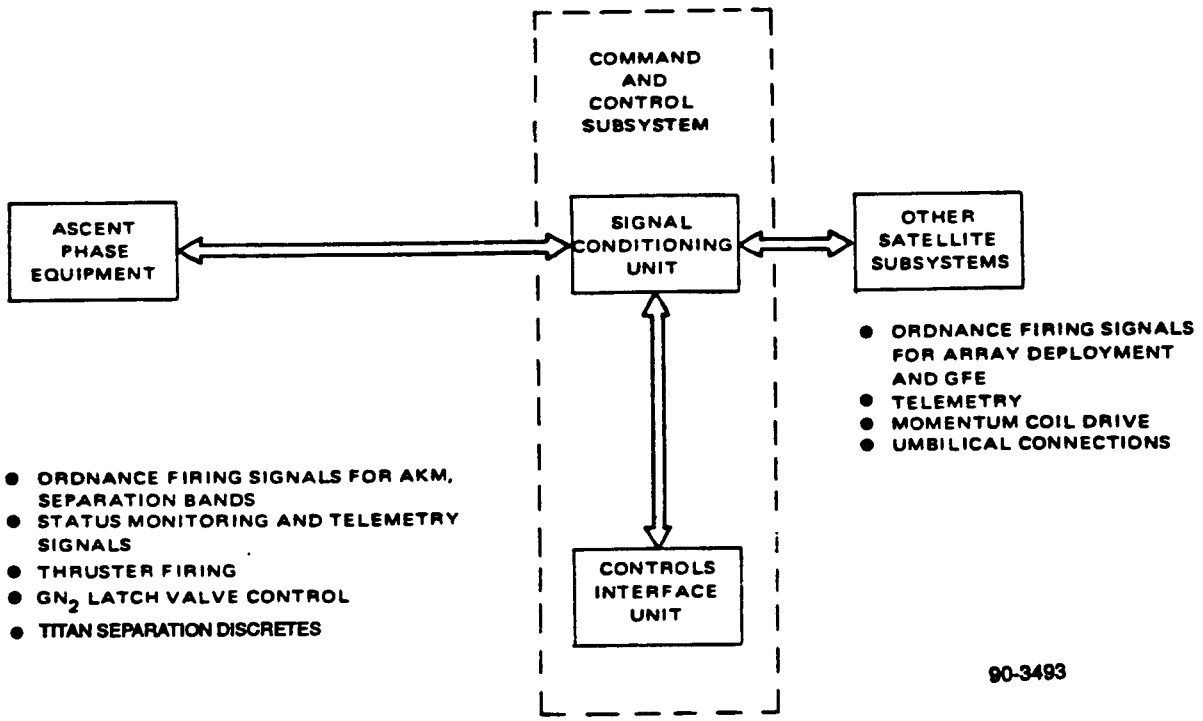

Figure 4.9.2-55. Signal Conditioning Unit Interface Diagram

2. Ordnance power conditioning circuits, which convert low level control signals to high current output signals suitable for actuating (firing) electro-explosive ordnance devices having minimum all-fire currents of 4.5 amperes or less. The power source for the ordnance firing signals is the spacecraft unregulated Battery buses.

3. Status signal conditioning circuits, which distribute and/or convert low level or passive input signals to low level output signals compatible with the requirements of the Controls Interface Unit (CIU), the Telemetry Information Processor (TIP), and the ISS umbilical.

4.9.2.4.1 Design Description

4.9.2.4.1.1 Design Approach

4.9.2.4.1.1.1 Relay Drivers. Relays are extensively used to switch various power buses to the proper load on command. Both latching and non-latching relays are used.

Relay drivers are used to provide the medium power signal required for actuating the relay in response to a low level control signal. Three different relay driver circuits are used, depending on the output drive required; these three types are shown in Figure 4.9.2-56. Each relay type provides a closure to ground capable of sinking the required load current; each relay driver interfaces with COS/MOS CD4041 buffers located in the CIU. The primary characteristics of the three relay drivers are summarized in Table 4.9.2-22.

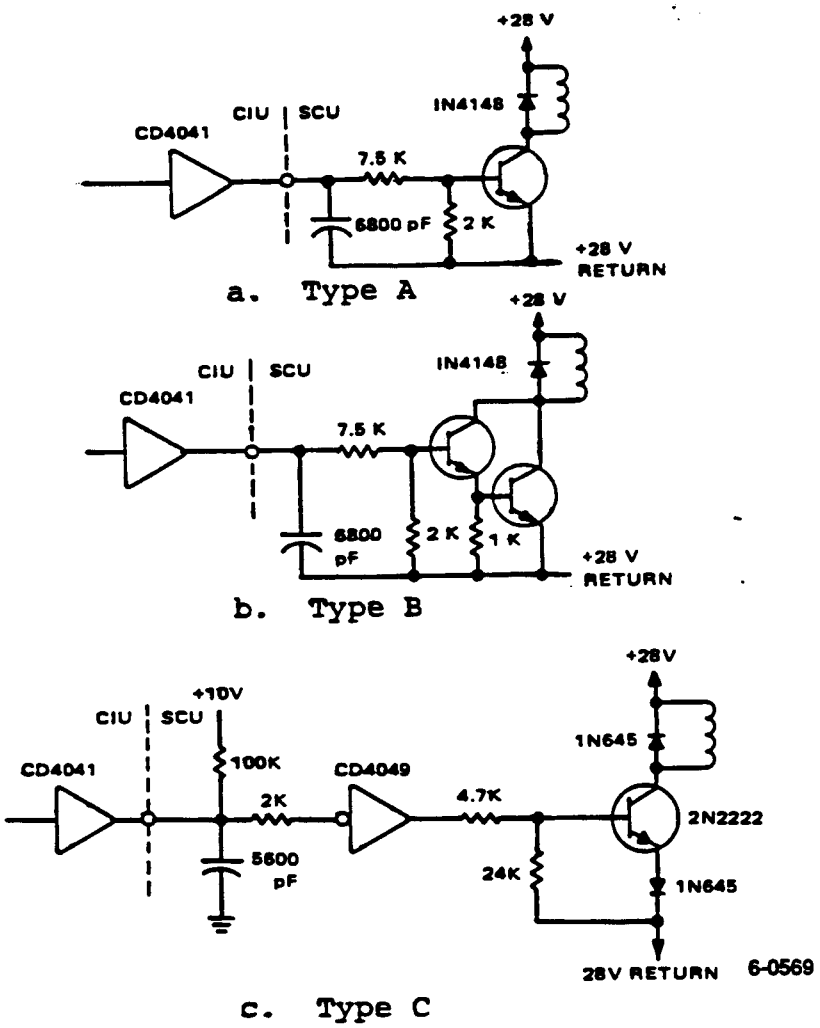

Figure 4.9.2-56. SCU Relay Driver Circuits

4.9.2.4.1.1.2 EMI/RFI Protection. The SCU is designed with the following EMI/RFI protective features:

- There are no high-current (i.e., greater than 50 milliamperes) lines routed through the same connector with control signals.
- All control signals are from a low-impedance source and are filtered at the SCU input.
- The assembled unit is constructed as a contiguous shield, including connector shells.
- A separate return is provided for each thruster and EED event control output.

TABLE 4.9.2-22. RELAY DRIVER CHARACTERISTICS

Driver Type	Input Current (mA)	Output Drive Capability	SCU Use
A	1.37	One 1000 ohm coil returned to +28V	SCU Power Switching Relays CPU Power Switching Relays Momentum Coil Relays (PTC/RYC) RCE Thruster Relays
B	1.37	Two parallel 320 ohm coils returned to +28V	Ordnance (Squib) Firing Relays EED Bus Switching (Arm) Relays
C	1.37	One 1000 ohm coil returned to +28V	Latch Valve Relays RCE Heater Power Relays

4.9.2.4.1.1.3 Pre-Launch Safety. The following pre-launch safety design features have been incorporated in the SCU:

- The power for all ascent phase relay drivers is removed by relays during routine processing. This power is enabled at the proper point during countdown.
- Continuous Safe/Arm (S/A) relay position monitor signals and S/A reset capability is provided via spacecraft umbilical.
- All relays are hermetically sealed.
- Complete redundancy is provided on all ordnance control circuits.

4.9.2.4.1.2 Operating Modes

4.9.2.4.1.2.1 SCU +28V Power Control. The distribution of power from the +28 volt bus within the SCU is controlled in response to two control signals received from the Controls Interface Unit (CIU):

- SCU Power On
- SCU Power Off

Except for the momentum controller, CPU power controller, RCE heater power controller, analog telemetry bus, and latch valve controller, all power and drive outputs are disconnected from the +28 volt bus in response to an SCU Power Off control signal and are re-connected in response to an SCU Power On control signal.

The momentum controller, CPU power controller, RCE heater power controller, and latch valve controller operate independently of the SCU power control signals.

4.9.2.4.1.2.2 CPU Power Control. Power to each Standard Controls Processor (CPU) and its associated electronics in the CIU is controlled in response to four control signals received from the CIU:

- CPU1 On
- CPU1 Off
- CPU2 On
- CPU2 Off

CPU power is controlled in accordance with the state diagram shown in Figure 4.9.2.57, which is discussed in detail in Section 4.9.2.4.2.2. Note that both CPU1 and CPU2 can never be turned off at the same time.

4.9.2.4.1.2.3 EED Bus Control. The EED bus supplied to the ordnance controllers in the SCU is controlled by safe/arm relays in response to four control signals:

- EED Bus Arm (from CIU)
- EED Bus Arm Reset (from umbilical)
- EED Bus Off
- CIU Orbit-B Mode

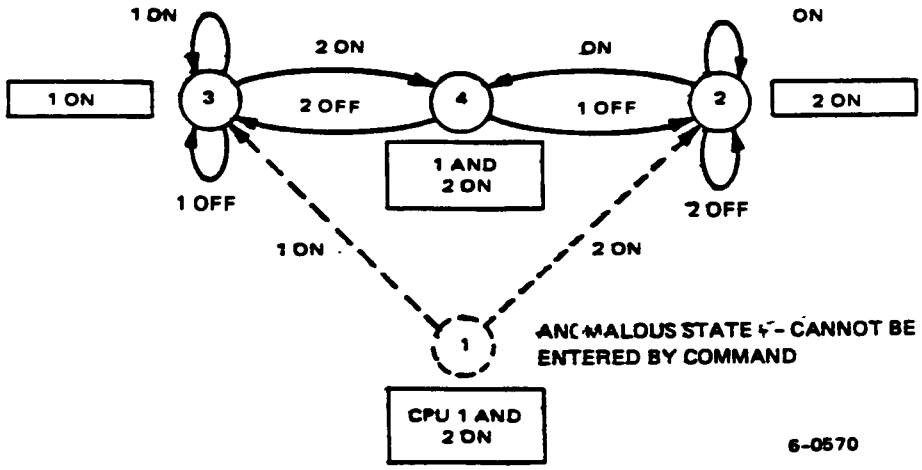

Figure 4.9.2-57. CPU Power Controller State Diagram

In response to the EED Bus Arm control signal, the EED bus is turned on to the various ordnance controllers, thus enabling or arming ordnance actuation. In response to the EED Bus Arm Reset control signal (or both the EED Bus Off and CIU Orbit-B Mode signals), the EED bus is turned off, disabling or safing ordnance actuation.

4.9.2.4.1.2.4 RCE Heater Power Control. Power to the RCE heaters is controlled in response to the following control signals received from the CIU:

- RCE A Heaters On
- RCE A Heaters Off
- RCE B Heaters On
- RCE B Heaters Off
- RCE C Heaters On
- RCE C Heaters Off
- RCE D Heaters On
- RCE D Heaters Off

4.9.2.4.1.2.5 Latch Valve Control. The latch valve controlling the distribution of nitrogen to the N_2 attitude control thrusters is either opened or closed in response to two control signals from the CIU:

- Latch Valve Open
- Latch Valve Close

4.9.2.4.1.3 Design Characteristics. The design characteristics of the Signal Conditioning Unit are listed in Table 4.9.2-23.

4.9.2.4.1.4 Physical Description. The physical arrangement of the Signal Conditioning Unit is shown in Figure 4.9.2-58. All SCU circuits are distributed on 5 slide-in circuit board assemblies. Each board assembly has several connectors at one end, which provide all input and output connections. The connector types used are Microdot for low level signals and Cannon "Golden D" for power buses and high current level signals. The assembled unit is a contiguous shield (including connector shells) for EMI/RFI protection.

TABLE 4.9.2-23. SCU DESIGN CHARACTERISTICS

Parameter	Value
Power Requirements	
Ascent Mode (On)	1.0 watt
Orbit Mode (Off)	0.1 watt
Size	8.70 x 6.82 x 6.41 (inches)
Footprint	8.70 x 8.00 (inches)
Weight	8.7 pounds

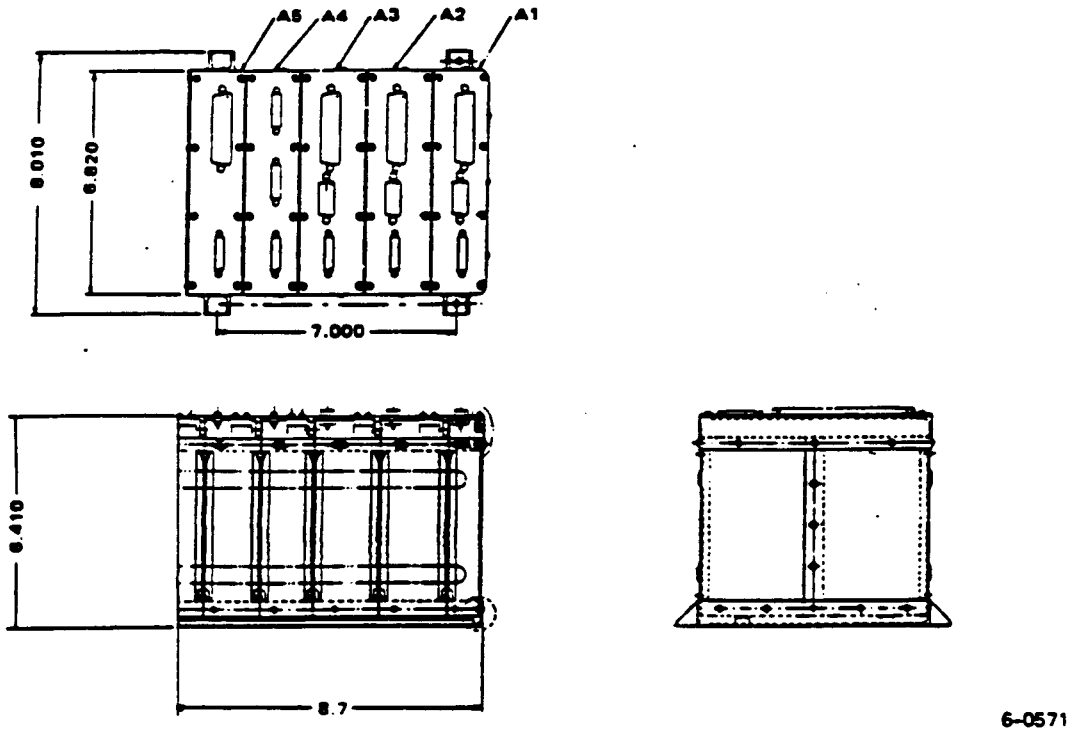

Figure 4.9.2-58. SCU Physical Configuration

4.9.2.4.2 Functional Description

The SCU provides interface signal conditioning for all signals between the Ascent Phase Equipment and all other parts of the ISS, and for certain non-standard signals between the Controls Interface Unit and other subsystems in the satellite. A functional block diagram of the SCU is shown in Figure 4.9.2-59.

4.9.2.4.2.1 SCU Power Controller. The SCU controls the distribution of +28 volt power within the SCU in response to three control signals:

- SCU Power On
- SCU Power Off
- SCU Power Reset (ground test only)

As shown in Figure 4.9.2-60, the SCU power controller consists of a pair of latching relays with their associated relay drivers. The +28V Switched bus power is turned on at receipt of an SCU Power On control signal, and is turned off at receipt of an SCU Power Off control signal; a telemetry indication of the status of the bus is provided.

The SCU also responds to a 28V SCU Power Reset control signal from the ground test equipment. As shown in Figure 4.9.2-61, the SCU Power Reset control signal inhibits SCU power commanding and forces the SCU into the off state. This circuit provides additional safing of ordnance during ground test operations. The circuit becomes non-functional at umbilical disconnect, after which normal SCU power control is restored.

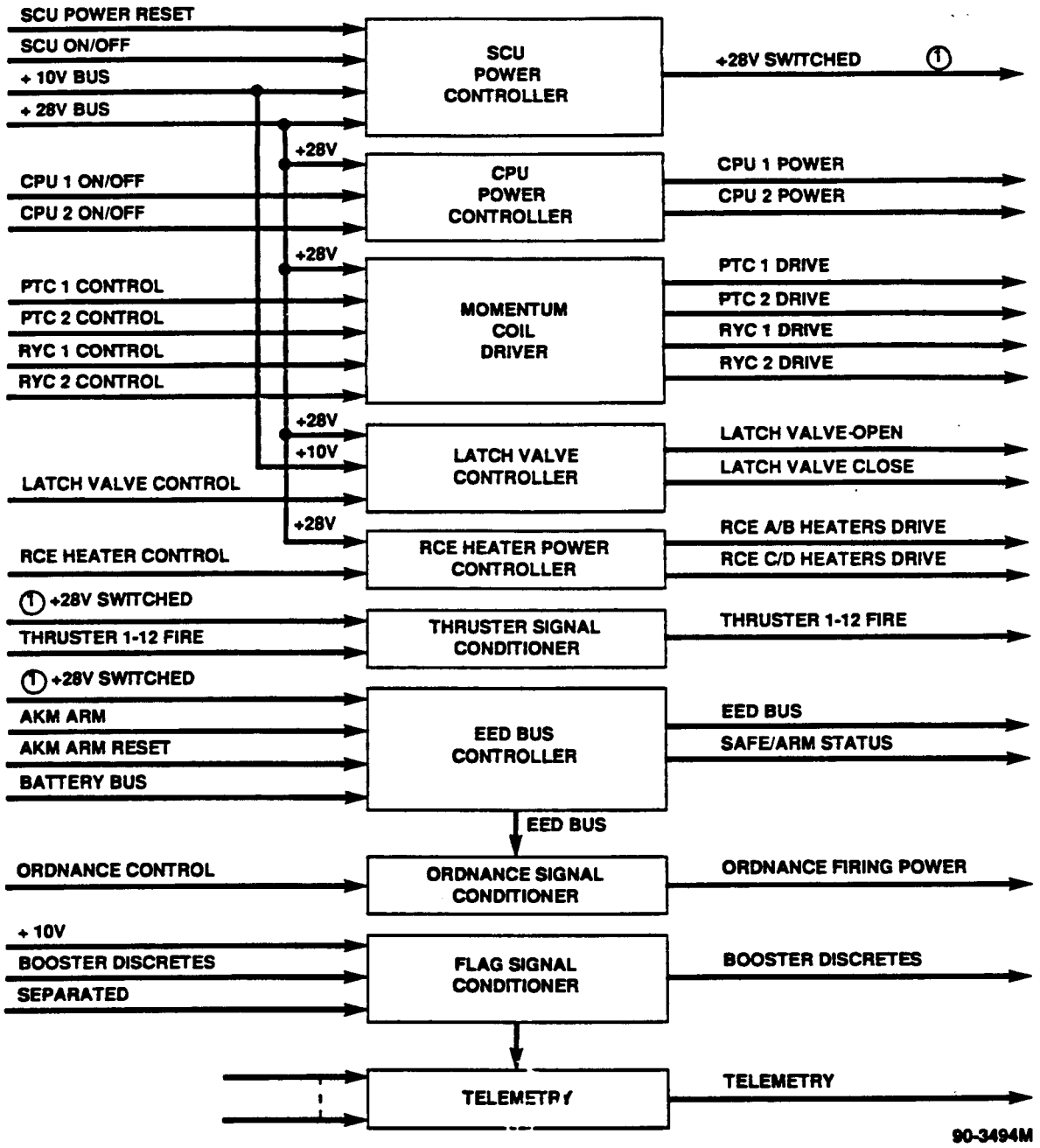

Figure 4.9.2-59. SCU Functional Block Diagram

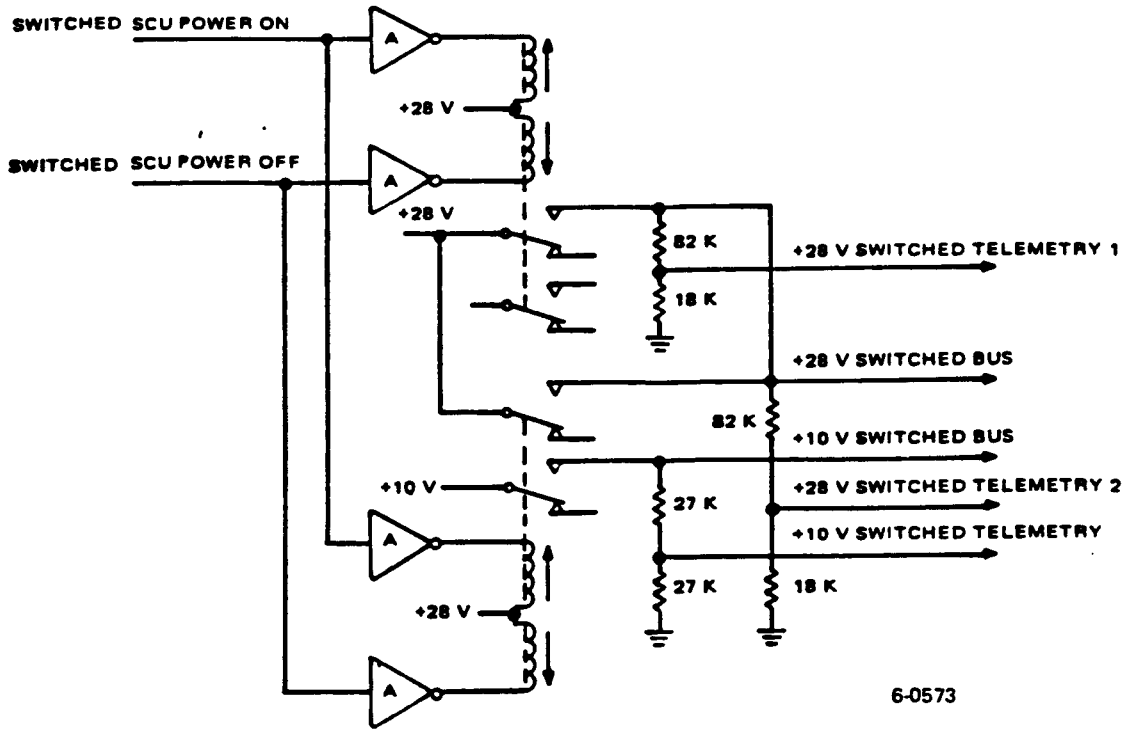

Figure 4.9.2-60. SCU Power Controller Schematic Diagram

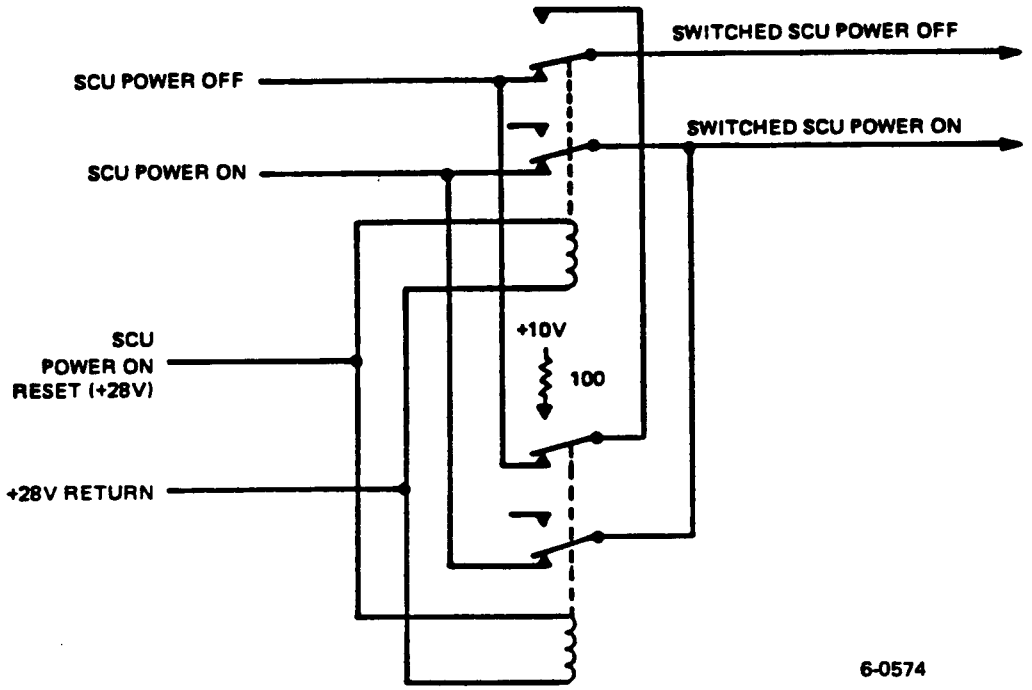

Figure 4.9.2-61. SCU Power Inhibit Schematic Diagram

The +28V Switched bus is provided to all other controllers within the SCU except for the momentum controller, CPU power controller, latch valve controller, analog telemetry bus, and RCE heater power controller.

4.9.2.4.2.2 CPU Power Controller. The CPU power controller provides power to CPU1, CPU2, and the CIU in response to four control signals:

- CPU1 On
- CPU1 Off
- CPU2 On
- CPU2 Off

As shown in Figure 4.9.2-62, the CPU power controller consists of two latching relays and their associated relay drivers. The relays control the +28 volt power to the two dc to dc converters in the Controls Power Converter, which in turn supply +10 volt power to CPU1, CPU2, and their associated electronics in the CIU.

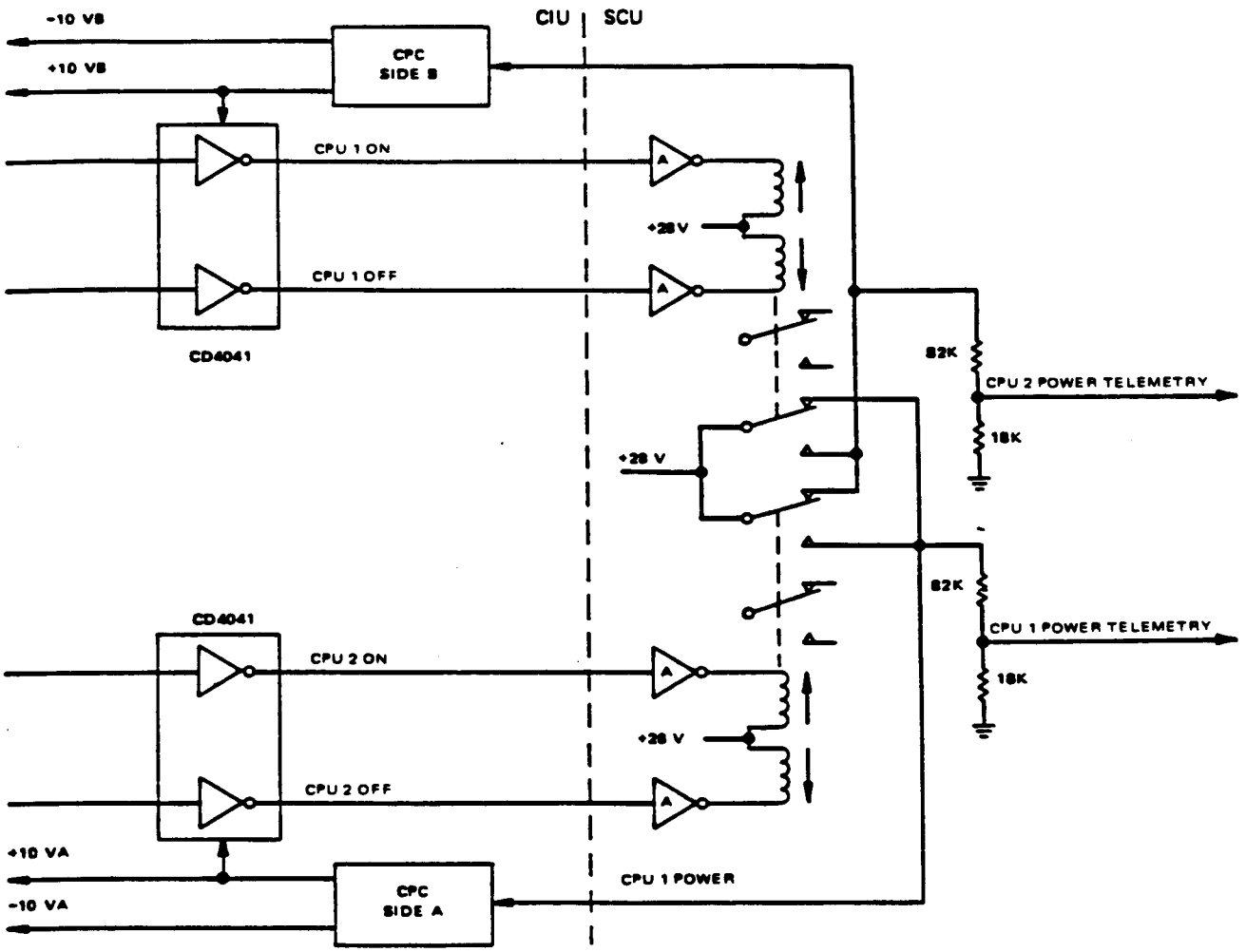

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Figure 4.9.2-62. CPU Power Controller Circuit Diagram

The CPU power controller operates as shown in Figure 4.9.2-63. The controller normally resides in state 4, with both CPU1 and CPU2 turned on. If a CPU2 Off control signal is received, the controller enters state 3; while in state 3, all CPU1 control signals are essentially ignored (CPU1 On does nothing, since CPU1 is already on; CPU1 Off is inhibited by the CD4041 buffer in the CIU, since the +10 volt bus is turned off). The only control signal that will be "honored" is CPU2 On, after which the controller enters state 4 again.

If a CPU1 Off control signal is received while in state 4, the controller enters state 2, where all CPU2 control signals are essentially ignored. The only exit from state 2 is back to state 4 after a CPU1 On control signal.

Note that state 1 is also shown on the state diagram. State 1 corresponds to both latching relays in the reset state, which requires receipt of an CPU Off control signal while the other CPU is already off; however, this is inhibited in the output buffer of the CIU. Therefore, State 1 cannot be entered by command, and should not occur in the absence of major transients on the spacecraft power buses. If state 1 should occur, both CPU1 and CPU2 are turned on; as shown, exit from state 1 occurs after a CPU On control signal, which results in entry to state 2 or state 3.

4.9.2.4.2.3 EED Bus Controller. The EED bus controller provides power for the actuation (firing) of all ordnance devices. As shown in Figure 4.9.2-64, the EED power bus is controlled in response to four signals:

- EED Bus Arm (from CIU)
- EED Bus Arm Reset (from umbilical)
- EED Bus Off (from CIU)
- CIU Orbit-B Mode (from CIU)

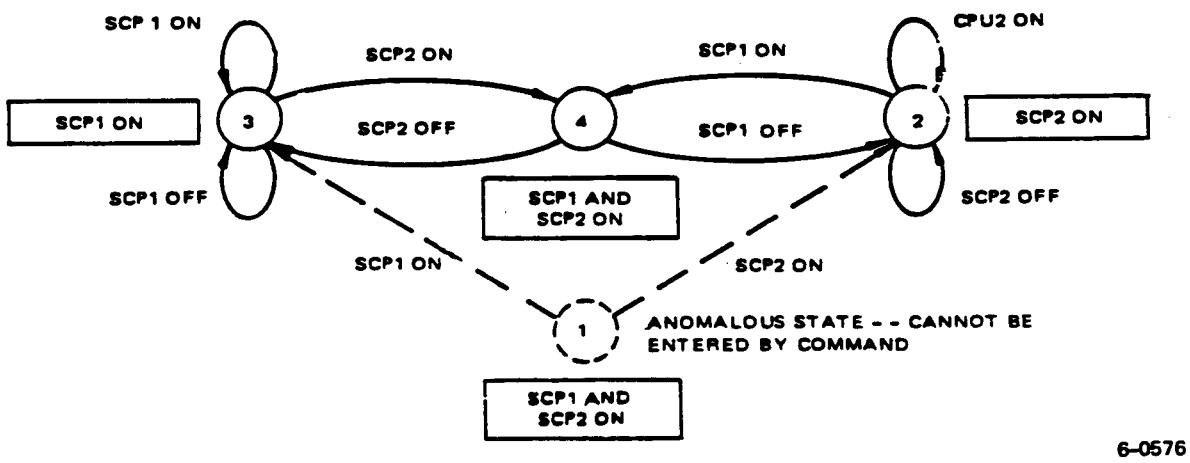

Figure 4.9.2-63. CPU Power Controller State Diagram

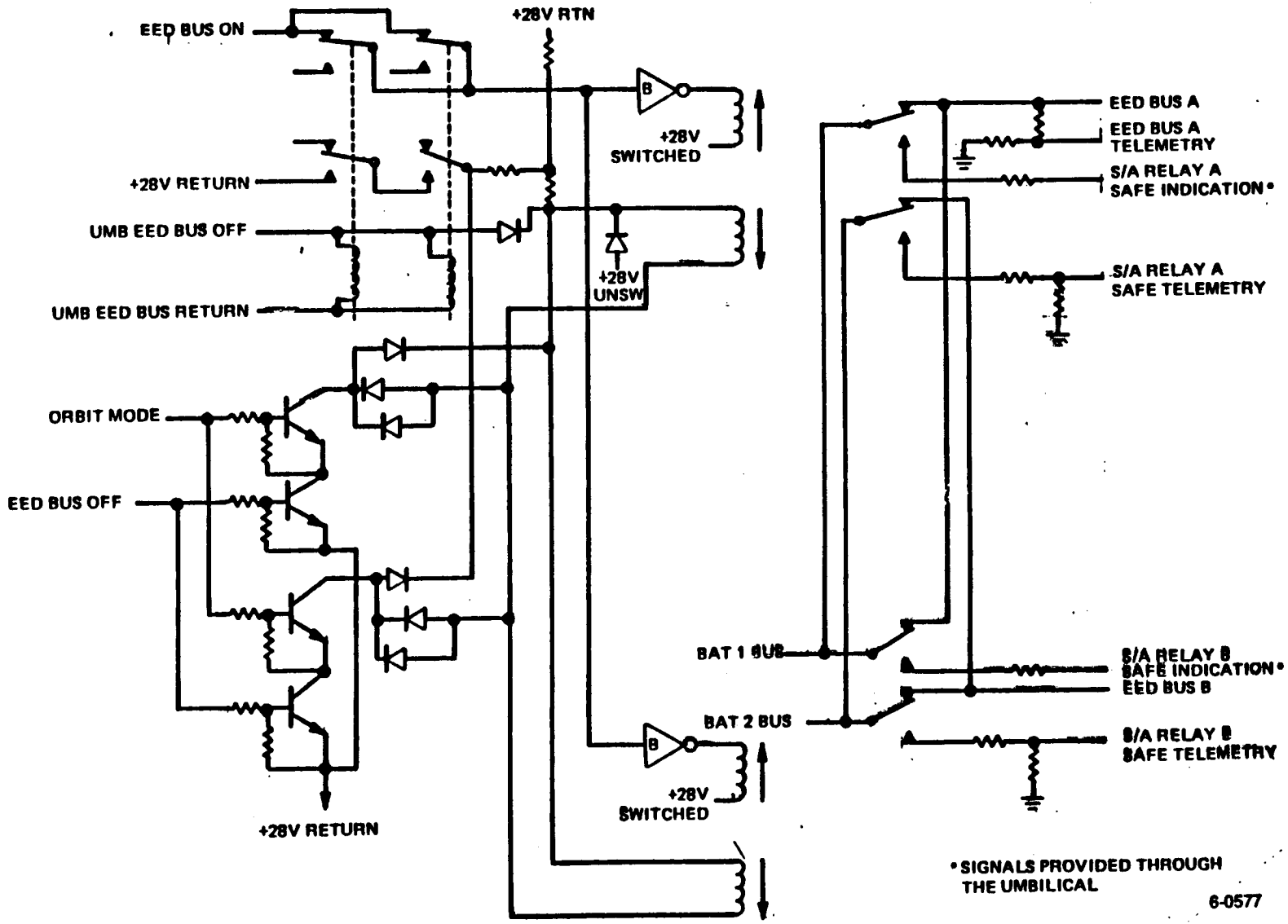

Figure 4.9.2-64. EED Bus Controller Schematic Diagram

In response to an EED Bus Arm control signal, the spacecraft battery 1 and battery 2 buses are connected to EED Bus A and EED Bus B, respectively; this enables the firing of all ordnance devices (squibs) through their individual control circuits. In response to an EED Bus Arm Reset control signal (received only through the umbilical), the spacecraft Batteries are disconnected from the EED buses, which disables the firing of all ordnance devices and also inhibits EED Bus Arm commanding. The spacecraft batteries are also disconnected from the EED buses in response to both an EED Bus Off command and a CIU Orbit-B Mode indication.

A positive indication of the safe status of each safe/arm relay is provided to the spacecraft umbilical; a positive indication of the safe status of each relay and the arm status of EED bus A is available through telemetry.

4.9.2.4.2.4 Momentum Coil Driver. The SCU provides momentum coil drive signals to Pitch Torquing Coil 1 and 2 (redundant pair) and Roll/Yaw Coil 1 and 2 (redundant pair). A typical momentum coil drive circuit diagram is shown in Figure 4.9.2-65. The SCU utilizes latching relays to initiate or terminate the appropriate polarity drive signal to each coil in response to the following control signals:

- PTC1 On
- PTC1 Off
- PTC1 +
- PTC1 -
- PTC2 On
- PTC2 Off
- PTC2 +
- PTC2 -
- RYC1 On
- RYC1 Off
- RYC1 +
- RYC1 -
- RYC2 On
- RYC2 Off
- RYC2 +
- RYC2 -

A reversible drive/return line pair is used for the drive output to each coil.

4.9.2.4.2.5 RCE Thruster Signal Conditioner. The SCU provides 12 non-latching relays that switch power from the +28 volt bus to activate any or all of 12 solenoid coils which fire Reaction Control Equipment (RCE) thrusters. A circuit diagram of a typical thruster signal conditioner is shown in Figure 4.9.2-66. Each of the 12 thruster drive signals is activated in response to 1 of 13 separate control signals designated as follows:

- Thruster 1 Fire
- Thruster 2 Fire
- Thruster 3 Fire
- Thruster 4 Fire

} N_2H_4 Pitch/Yaw

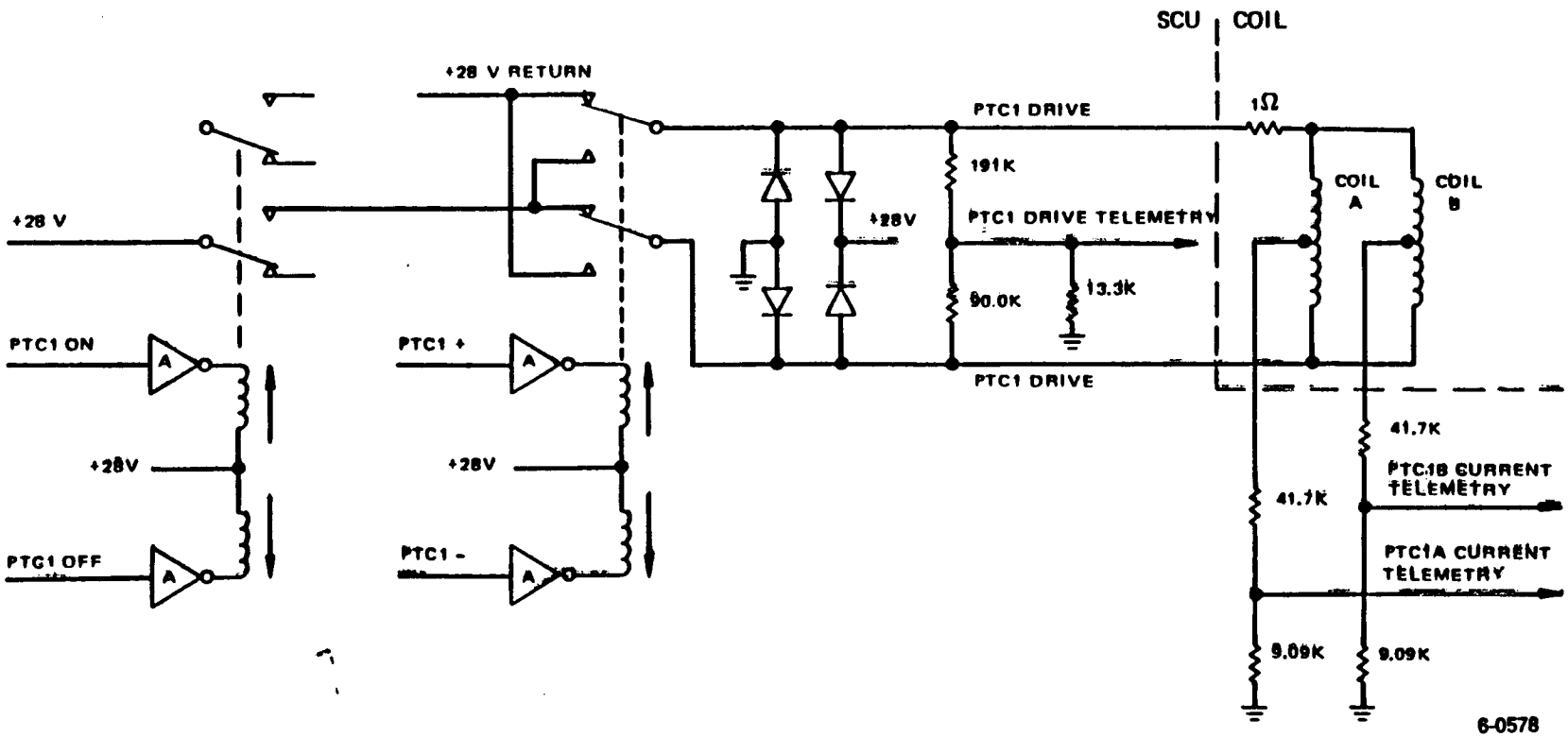

Figure 4.9.2-65. Typical Momentum Coil Driver Circuit Diagram

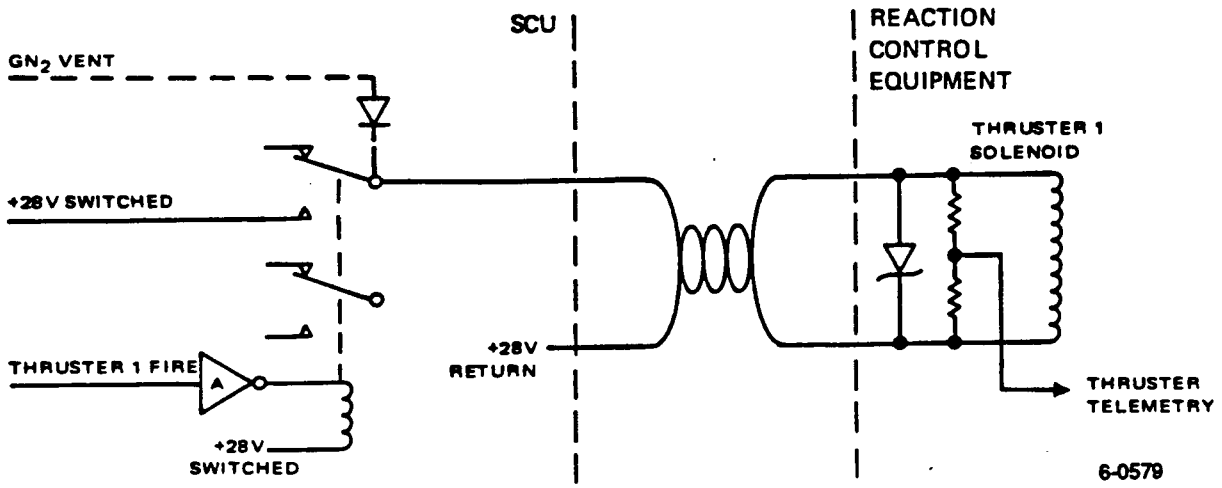

Figure 4.9.2-66. Typical Thruster Signal Conditioner Circuit Diagram

- Thruster 5 Fire
- Thruster 6 Fire
- Thruster 7 Fire
- Thruster 8 Fire

} N_2 Pitch/Yaw

- Thruster 9 Fire
- Thruster 10 Fire
- Thruster 11 Fire
- Thruster 12 Fire

} N_2 Roll

- GN_2 Vent

The SCU provides access to the Thruster 11 Drive and Thruster 12 Drive signal outputs such that they may be separately activated via the spacecraft umbilical by means of a single +28 volt GN_2 Vent control signal. The GN_2 Vent control signal is connected through isolation diodes directly to the thruster drive output lines. The GN_2 Vent signal also opens the latch valve (see Section 4.9.2.4.2.8).

Each thruster drive signal output is active as long as its associated control signal input is present.

4.9.2.4.2.6 RCE Heater Power Controller. The SCU provides latching relays for the selective connection or disconnection of +28V power to the RCE heaters; four independent latching relays are used to control four independent sets of RCE heaters. A circuit diagram of one of the latching relay circuits is shown in Figure 4.9.2-67.

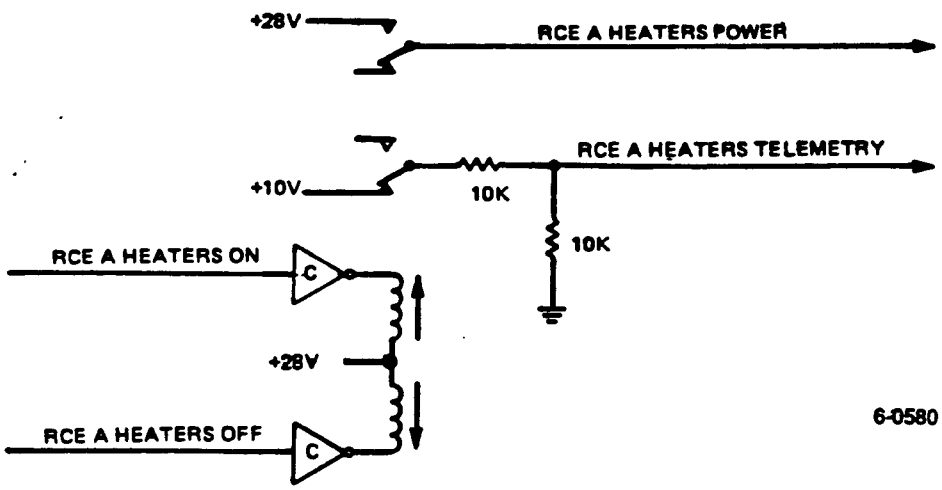

Figure 4.9.2-67. Typical RCE Heaters Power Controller Circuit Design

The relays are switched in response to the following control signals:

- RCE A Heaters On
- RCE A Heaters Off
- RCE B Heaters On
- RCE B Heaters Off
- RCE C Heaters On
- RCE C Heaters Off
- RCE D Heaters On
- RCE D Heaters Off

Each latching relay has a telemetry signal to indicate its status.

4.9.2.4.2.7 <u>+28 Volt Switched Telemetry Bus</u>. The SCU provides a latching relay for the selective connection or disconnecting of +28V power to +28V switched telemetry bus. The circuit is identical to that of Section 4.9.2.4.2.6 and Figure 4.9.2-67. The relay is switched in response to the following control signals:

- Telemetry Bus On
- Telemetry Bus Off

4.9.2.4.2.8 <u>Latch Valve Controller</u>. The SCU switches power from the +28V bus to either open or close the latch valve in the distribution line to the N_2 thrusters. A circuit diagram of the latch valve controller is shown in Figure 4.9.2-68. The latch valve is controlled in response to the following control signals:

- Latch valve open
- Latch valve closed

The latch valve may also be opened via the spacecraft umbilical by means of the +28 volt GN_2 Vent control signal. The GN_2 Vent control signal is connected through isolation diodes directly to the latch valve open output line.

4.9.2.4.2.9 Ordnance Signal Conditioner. The SCU contains several non-latching relays which switch power from the spacecraft Battery buses to provide ordnance firing output signals. Each firing signal is separately switched; i.e., any one relay contact (pole) is not connected to more than one squib.

A schematic diagram of a typical ordnance firing circuit is shown in Figure 4.9.2-69. Ordnance firing signals are activated by control signals in accordance with Table 4.9.2-24. All output firing signals are active as long as the associated control signal is present.

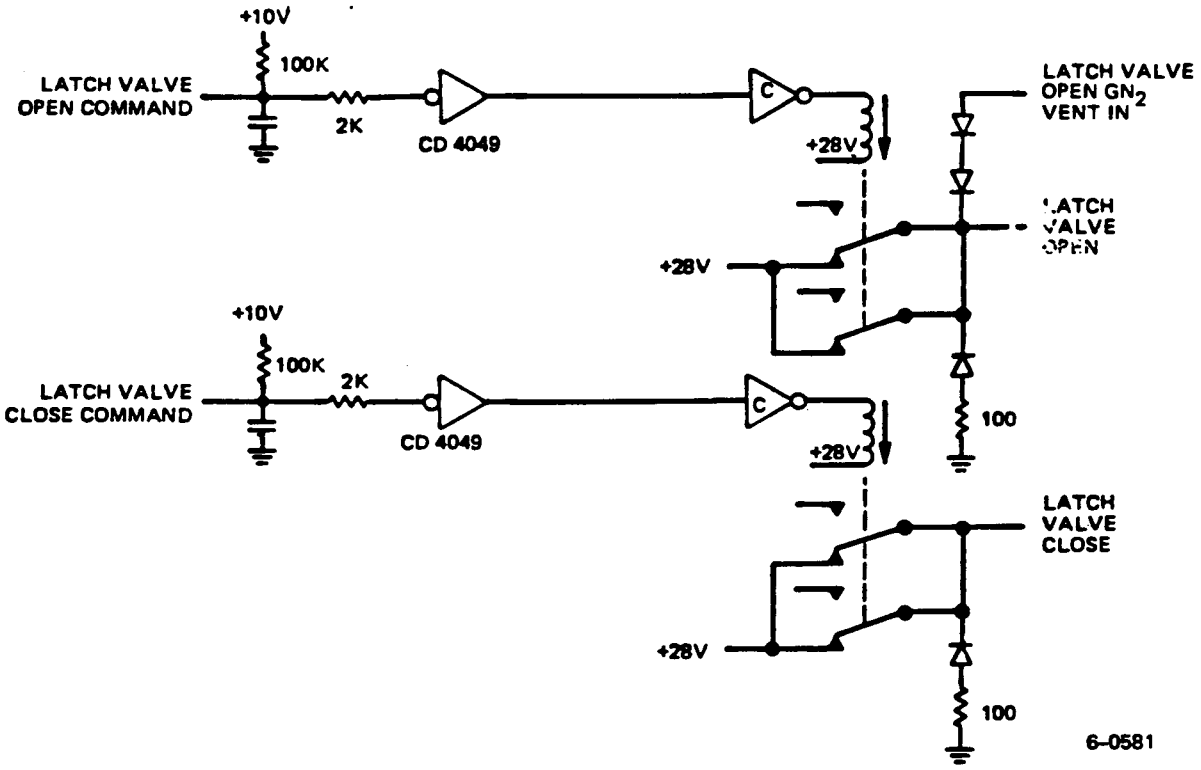

Figure 4.9.2-68. Latch Valve Controller Schematic Diagram

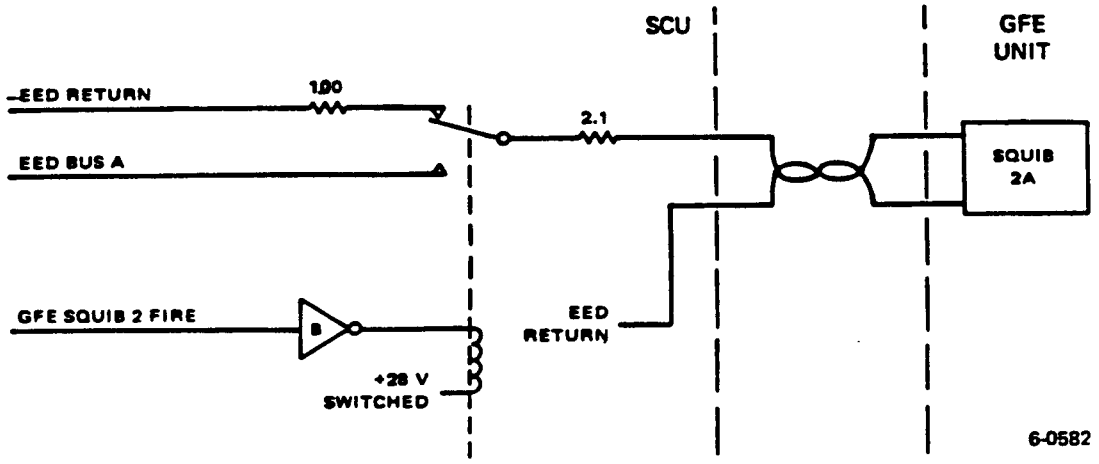

Figure 4.9.2-69. Typical Ordnance Signal Conditioner Circuit Diagram

TABLE 4.9.2-24. SCU ORDNANCE FIRING SIGNALS

Input Control Signal	Output Drive Signal	EED Bus
AKM Ignition 1	AKM Ignition A	B
AKM Ignition 2	AKM Ignition B	A
N_2H_4 Isolation A	N_2H_4 Shutoff 1A	B
	N_2H_4 Shutoff 2A	B
N_2H_4 Isolation B	N_2H_4 Shutoff 1B	A
	N_2H_4 Shutoff 2B	A
SA Panel -Z1	SA Panel Deploy -Z1	A
SA Panel +Z1	SA Panel Deploy +Z1	B
SA Panel -Z2	SA Panel Deploy -Z2	B
SA Panel +Z2	SA Panel Deploy +Z2	A
SA Boom 1	SA Boom 1 Deploy +X	B
SA Boom 2	SA Boom 2 Deploy -X	A
SA Cant 1	SA Cant A	B
SA Cant 2	SA Cant B	A
SRA 1	SRA Deploy A	B
SRA 2	SRA Deploy B	A
Spacecraft Separation 1	Spacecraft Separation A	B
Spacecraft Separation 2	Spacecraft Separation B	A
UDA 1	UDA Deploy A	B
VRA 1	VRA Deploy A	B
UDA 2	UDA Deploy B	A
VRA 2	VRA Deploy B	A
Sunshade 1	Sunshade Deploy A + Y	B
	Sunshade Deploy B - Y	A
Sunshade 2	Sunshade Deploy B - Y	A
	Sunshade Deploy A - Y	B

Each output consists of a drive/return line pair; when not active, each drive line is connected to its respective return within the SCU.

Resistance in the EED bus path consists of the following:

A1 Board	(PC traces, input and output connectors with 4 pins paralleled, and EED arm relay contacts)	0.043 ohm
A2 Board	(PC traces, input and output connectors with 4 pins paralleled, and squib fire relay)	0.085
Wire between A1 and A2	(4 No. 20 wires in parallel less than 6 inches in length)	0.003
	Subtotal SCU Wiring	0.131 ohm

Allowance for Temperature Effects:

(Assume T = 50°C and allow additional 50° for heating, making ΔT = 80° at 0.4%/°C)

R = 0.32% =		0.042 ohm
	Total SCU Wiring Resistance	0.173
Current Limiting Resistor		2.121
	Total SCU Resistance	2.294 ohms

A current limiting resistor having a value of 2.1 ohms is provided in series with each ordnance firing signal to limit the maximum current to 10 amperes with a 0.9 ohm external load. At the opposite extreme, the circuit supplies a minimum current of 4.5 amperes with a 1.7 ohm external load and a minimum EED bus input of +18 volts.

In normal operation, the squib load becomes an open circuit at firing. In the event that this does not occur, the current limiting resistor has been selected such that it will fail in an open circuit condition.

4.9.2.4.2.10 Flag Signal Conditioner. The SCU provides several "flag" signals to the CIU. A circuit diagram of the flag signal conditioner is shown in Figure 4.9.2-70; the output state of the flag signal is shown in Table 4.9.2-25, along with the corresponding operational conditions.

4.9.2.4.3 Telemetry

The SCU provides analog and discrete telemetry signals to the Telemetry subsystem. Telemetry signals derived from high level signals (18 to 38 volts) are clamped to limit the maximum telemetry voltage to approximately +6 volts.

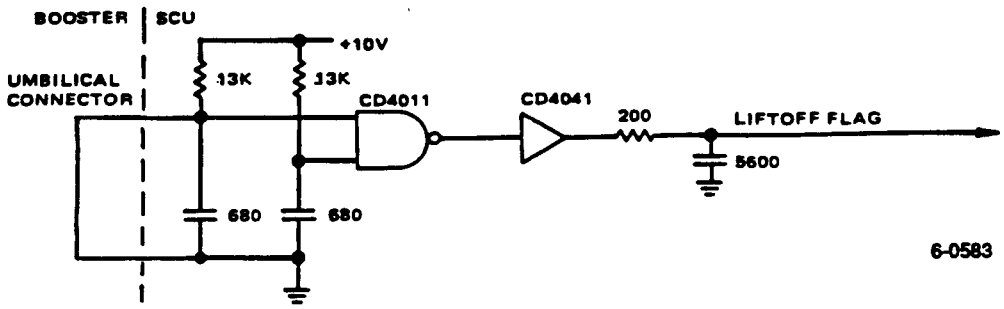

Figure 4.9.2-70. Liftoff Flag Signal Conditioner Circuit Diagram

TABLE 4.9.2-25. FLAG SIGNAL GENERATION

Condition	Liftoff	Flag State: Titan SEP-1	Titan SEP-2	Separated
SCU Off	True	True	True	True
SCU On	False	False	False	False
After Event	True	True	True	True

4.9.2.4.3.1 Analog Telemetry

4.9.2.4.3.1.1 Momentum Coil Drive Telemetry. Momentum coil drive telemetry is provided by a resistive matrix tied to the bi-level, reversible momentum coil drive lines. The coil drive telemetry points provided are:

a. PTC1 Drive Telemetry
b. PTC2 Drive Telemetry
c. RYC1 Drive Telemetry
d. RYC2 Drive Telemetry

With the momentum drive turned off, the telemetry voltage is 0 volts; with the momentum drive turned on, the telemetry voltage is approximately +1.6 volts in the ON + state or +3.4 volts in the ON - state.

4.9.2.4.3.1.2 Momentum Coil Current Telemetry. Momentum coil current telemetry is provided by a simple resistive divider connected to the center tap of each coil winding. The coil current telemetry points provided are:

a. PTC1A Current Telemetry
b. PTC1B Current Telemetry
c. PTC2A Current Telemetry
d. PTC2B Current Telemetry
e. RYC1A Current Telemetry
f. RYC1B Current Telemetry
g. RYC2A Current Telemetry
h. RYC2B Current Telemetry

With the momentum drive turned off, the telemetry voltage is 0 volts; with the momentum drive turned on, the telemetry voltage is approximately +2.5 volts in either the ON + or the ON - state.

4.9.2.4.3.1.3 Reaction Control Equipment Pressure. RCE pressure telemetry is provided by 3 pressure transducers that give an indication of the operating pressures in the nitrogen and hydrazine manifolds in the Reaction Control Equipment. The RCE pressure telemetry points provided are:

a. RCE High (Unregulated) GN_2 Pressure Telemetry
b. RCE Low (Regulated) GN_2 Pressure Telemetry
c. RCE N_2H_4 Pressure Telemetry

With the RCE pressurized to the proper pre-launch operating pressure, the telemetry output from the transducers is approximately +4.5 volts for the RCE high pressure and N_2H_4 pressure telemetry, and 3.5 volts for the RCE low pressure telemetry.

4.9.2.4.3.2 Discrete Telemetry. The discrete telemetry provided by the SCU is shown in Table 4.9.2-26.

4.9.2.5 Controls Power Converter

The Controls Power Converter (CPC) is a dual dc to dc converter, as shown in Figure 4.9.2-71. Each converter accepts +28 volts and provides output voltages of +10 and -10 volts. The output voltages from converter A are provided to CPU1 and to the CIU logic dedicated to CPU1; output voltages from converter B are provided to CPU2 and to the CIU logic dedicated to CPU2. A +10 volt common bus is also provided, through a diode OR gate from either converter; this uninterruptible bus is provided to all spacecraft units requiring +10 volt interface power. Telemetry indications are provided of the CPC operating mode and of the voltage level on the +10 volt common, -10 volt A, and -10 volt B buses.

4.9.2.5.1 Controls Power Converter Description

The CPC consists of two identical dc to dc converters. As shown in Figure 4.9.2-72, each converter consists essentially of an input filter, a switching regulator, an over-voltage protect circuit, a chopper feeding a transformer, and a pair of rectifiers and filters.

The line filter removes some of the noise on the +28 volt line and inhibits the reflection of chopper noise back onto the +28 volt line. The line filter also contains a transistor switch which is initially used to limit surge current at turn on; this switch is also opened if the voltage out of the switching regulator rises too high (to prevent over-voltage at the +10V output terminals).

The switching regulator accepts the +28 volt bus input (which may, under transient failure conditions, be anywhere in the range of 17 to 38 volts) and provides regulated +15 volt power to the chopper.

The over-voltage protect circuit monitors the output voltage from the switching regulator to protect the CIU and CPU from over-voltages.

TABLE 4.9.2-26. SCU DISCRETE TELEMETRY

Telemetry Point	State	Value (V)
Power Status Telemetry		
+28V Switched	SCU Off	0
	SCU On	+5
+10V Switched	SCU Off	0
	SCU On	+5
CPU1 Power Telemetry	CPU1 Off	0
	CPU1 On	+5
CPU2 Power Telemetry	CPU2 Off	0
	CPU2 On	+5
Ordnance Status Telemetry		
EED Bus A Status	EED Safe	0
	EED Armed	+4.75
EED Bus B Status 1	EED Safe	+4.75
	EED Armed	0
EED Bus B Status 2	EED Safe	+4.75
	EED Armed	0
Event Status Telemetry		
AKM Ignite A	Inactive	+5
	Active	0
AKM Ignite B	Inactive	+5
	Active	0
Miscellaneous		
Latch Valve Status	Closed	+5
	Open	0
RCE A Heaters	Heaters On	0
	Heaters Off	+5
RCE B Heaters	Heaters On	0
	Heaters Off	+5
RCE C Heaters	Heaters On	0
	Heaters Off	+5
RCE D Heaters	Heaters On	0
	Heaters Off	+5
Telemetry Bus	On	0
	Off	+5

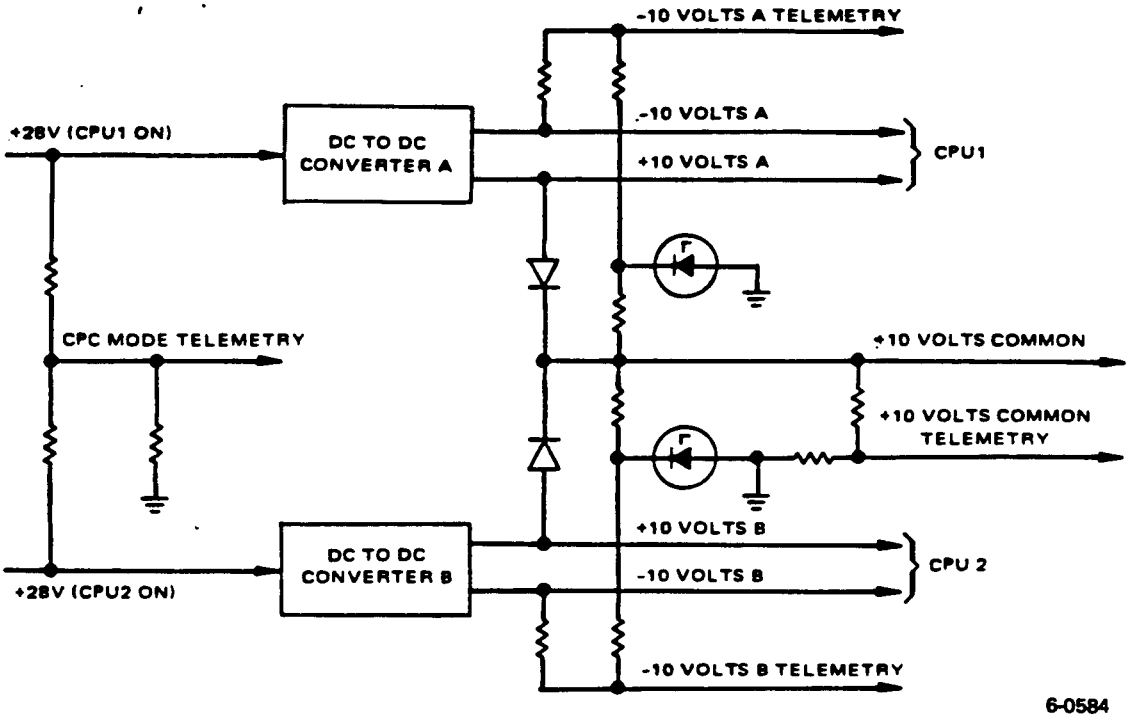

Figure 4.9.2-71. Controls Power Converter Functional Block Diagram

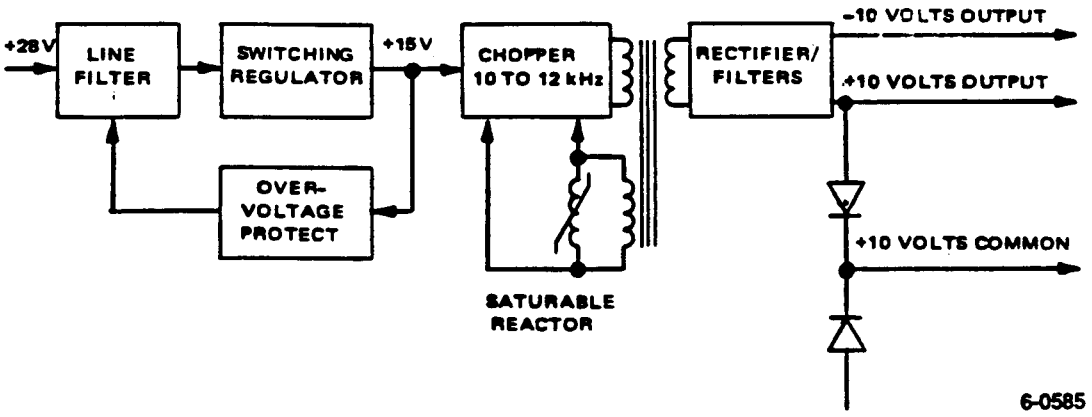

Figure 4.9.2-72. DC to DC Converter Functional Block Diagram

If this voltage goes too high (approximately 16 volts), then the over-voltage protect circuit latches up and opens the line filter transistor switch, removing power from the switching regulator. The over-voltage protect circuit remains latched up until power is removed and re-applied, after which operation returns to normal until an excessive voltage again trips the latch. The chopper is a free running inverter, with the operating frequency controlled by the saturable reactor. The transformer saturates at a frequency of approximately 6 kHz; operating the inverter at from 10 to 12 kHz thus assures

that the transformer does not saturate, which minimizes switching transients and spikes and maximizes conversion efficiency.

A pair of full wave rectifiers operating from a single transformer secondary convert the ac input voltage into two dc output voltages. The output filters remove the switching spikes and transients from the output, and minimize the effects of load current switching.

4.9.2.5.1.1 Design Approach. The design of the CPC is conventional; each dc to dc converter consists essentially of a switching regulator and a power oscillator followed by rectifiers and filters to provide the desired output voltages. The CPC is configured to protect the CIU and CPU from any abnormal voltage deviation on the spacecraft +28 volt bus and from abnormal operations within either converter.

4.9.2.5.1.2 Operating Modes. The operating modes are:

- Off (Inhibited in SCU)
- Side 1 On
- Side 2 On
- Both Sides On

The operating mode is controlled by the presence or absence of the +28 volt CIU power applied to each converter; if the +28 volts is present, then that converter is operating and providing output voltages.

The +28 volt CIU power is controlled by the SCU, which turns CIU power 1 on or off and turns CIU power 2 on or off in accordance with control signals received from the CIU. Circuits in the SCU are interlocked such that CIU power 1 and CIU power 2 can never be turned off at the same time; the CPC Off mode cannot be commanded.

4.9.2.5.1.3 Performance Summary. The performance characteristics of the CPC are listed in Table 4.9.2-27.

4.9.2.5.1.4 Physical Description. The CPC is a single rectangular assembly, as shown in Figure 4.9.2-73.

4.9.2.5.2 Telemetry

There are four telemetry signals provided by the CPC:

- CPC Mode Telemetry
- -10 Volts A Telemetry
- -10 Volts B Telemetry
- +10 Volts Common Telemetry

The CPC mode telemetry provides a level discrete output signal indicating the operating mode of the CPC. The operating modes are listed in Table 4.9.2-28, along with the resulting converter states and associated telemetry values.

The -10 volt telemetry circuits provide an analog indication of the -10 volt output level. This signal is +1.3 volts at a normal output level of -10 volts, and is +4.4 volts at an output level of zero volts.

TABLE 4.9.2-27. CONTROLS POWER CONVERTER DESIGN CHARACTERISTICS

Parameter	Value
Input Voltage	+17 to +38V (+28V nominal)
Output Voltages	
Converter A	+10 ±0.50V -10 ±0.50V
Converter B	+10 ±0.50V -10 ±0.50V
Common	+10 ±0.50V
Output Current	
+10V (A or B)	200 to 1200 mA
-10V (A or B)	15 to 75 mA
+10V (common)	100 to 800 mA
Output Ripple	<50 mV p-p
Conversion Efficiency	63% (EOL)
Size	5.0 x 7.0 x 1.0 (inches)
Weight	<2.25 lbs.

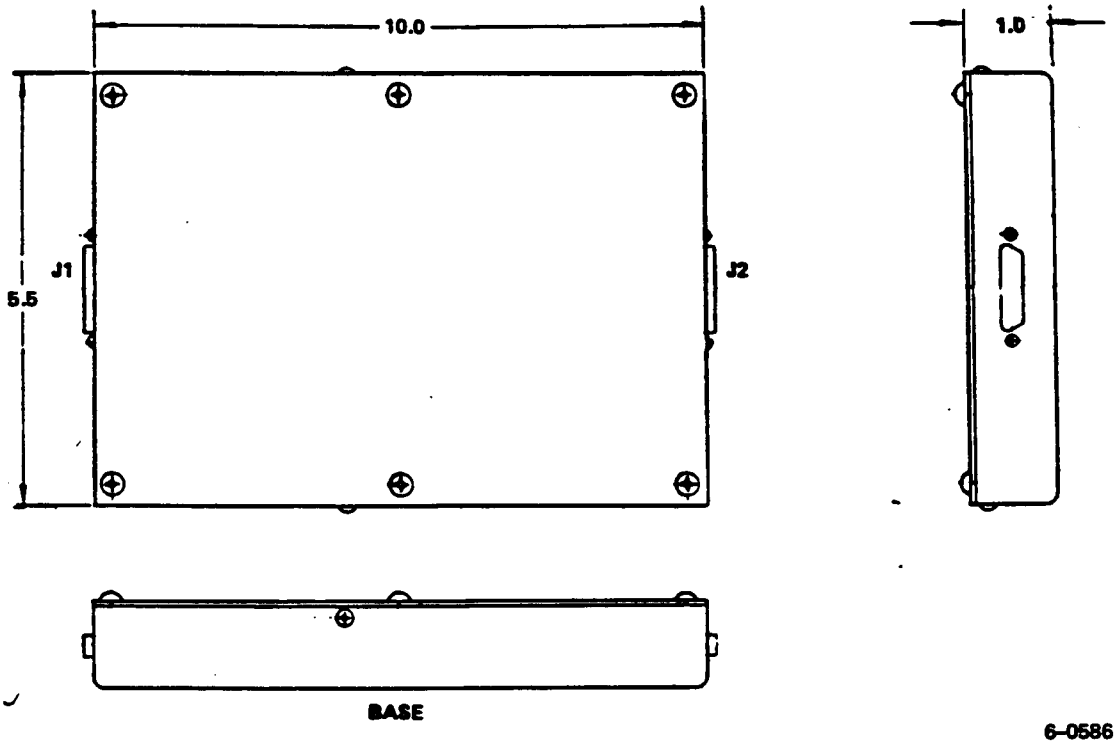

Figure 4.9.2-73. Controls Power Converter Outline Drawing

TABLE 4.9.2-28. TYPICAL CPC MODE TELEMETRY

Converter State 1	Converter State 2	Telemetry Value (V)
Off	Off	0
Off	On	1.62
On	Off	3.33
On	On	4.59

The +10 volt telemetry circuit provides an analog indication of the +10 volt output level. This signal is +3.88 volts at a normal output level of +10 volts.

4.9.2.6 Controls Interface Annex

The Controls Interface Annex (CXU) serves as an extension to the output capability of the CIU. The CXU accepts serial 16-bit address/data words from the CIU and steers the data to one of 16 level-command Parallel Output Buffers (POB) or to one of 16 pulse-command buffers.

4.9.2.6.1 Functional Description

There are three basic functions of the CXU as shown in Figure 4.9.2-74, these functions are:

- Receive and decode command messages from the CIU
- Distribute the command messages in the form of the pulse-discretes and level-discretes to other spacecraft systems.
- Provide redundancy for both command inputs, outputs and cross-strapping capability

4.9.2.6.2 Design

4.9.2.6.2.1 Control Logic and Sequencer. The transfer of command/data from the CIU to the CXU is as follows.

The CXU receives a 16 bit command data word from the CIU. The data source in the CIU is a standard serial output buffer utilizing single word transfer as described in 4.9.2.2.2. The CIU transmits to the CXU a Start signal, Data, and a burst of 16 Clock pulses at 102.4 kpbs when the data transfer takes place. When the Start signal is activated, the CXU activates the Transfer signal to the CIU, indicating a readiness to accept data. When that occurs, the shifting of data across the interface will commence. Data is clocked into the CXU on the positive-going transitions of the data clock. A 0-volt signal on the Data input will represent a Data 1 while +10 volts represents a Data 0.

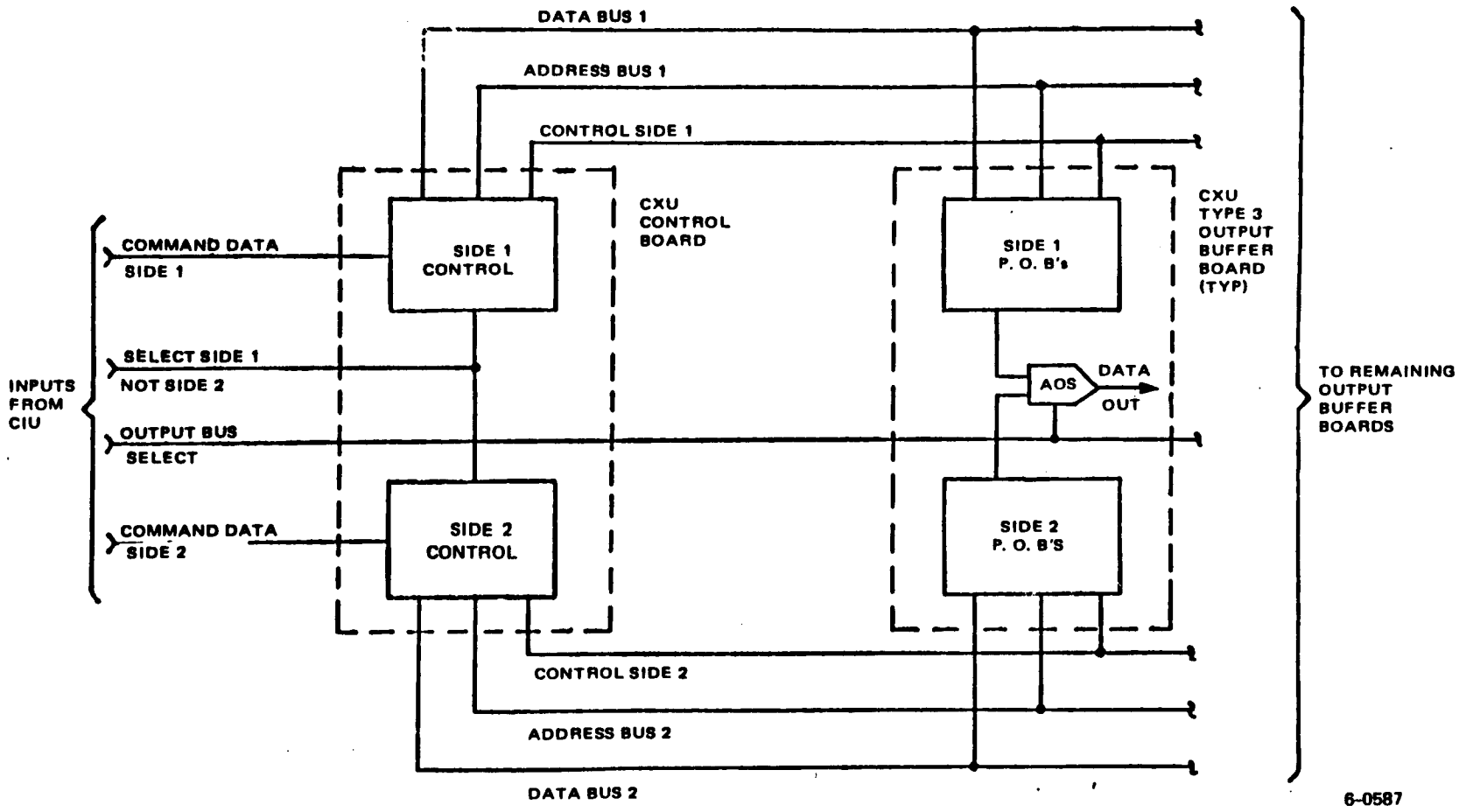

Figure 4.9.2-74. Control Interface Annex (CXU) Block Diagram

When the 15th data bit has been clocked into the CXU, the Transfer signal is terminated. One additional clock pulse is received to clock the 16th data bit and the Start signal is terminated concluding the data transfer. If the Start signal is terminated at any time during a data transfer but before a complete 16 bit-word has been accepted, the CXU will clear its input data sequencer until the Start signal is once again activated. Figure 4.9.2-75 shows the timing details of the serial data transfer.

The CXU commanded side select is used by the CIU SOB so that only the transfer signal from the selected CXU side is accepted.

When this level discrete is in the active state, the CIU will respond to the Transfer signal from CXU side 1. When in the inactive state, the CIU will respond to the CXU side 2 Transfer signal. In this sense, the "select CXU side" signal may be thought of as selecting the "master" CXU side. The CXU inputs data to both CXU sides simultaneously without regard to the state of the "select" CXU side signal.

4.9.2.6.2.2 Command Execution. After a valid 16-bit word has been received, the command word is executed. Execution consists of transferring the contents of the 8-bit data field to an output holding register as dictated by the address field as shown in Figure 4.9.2-76.

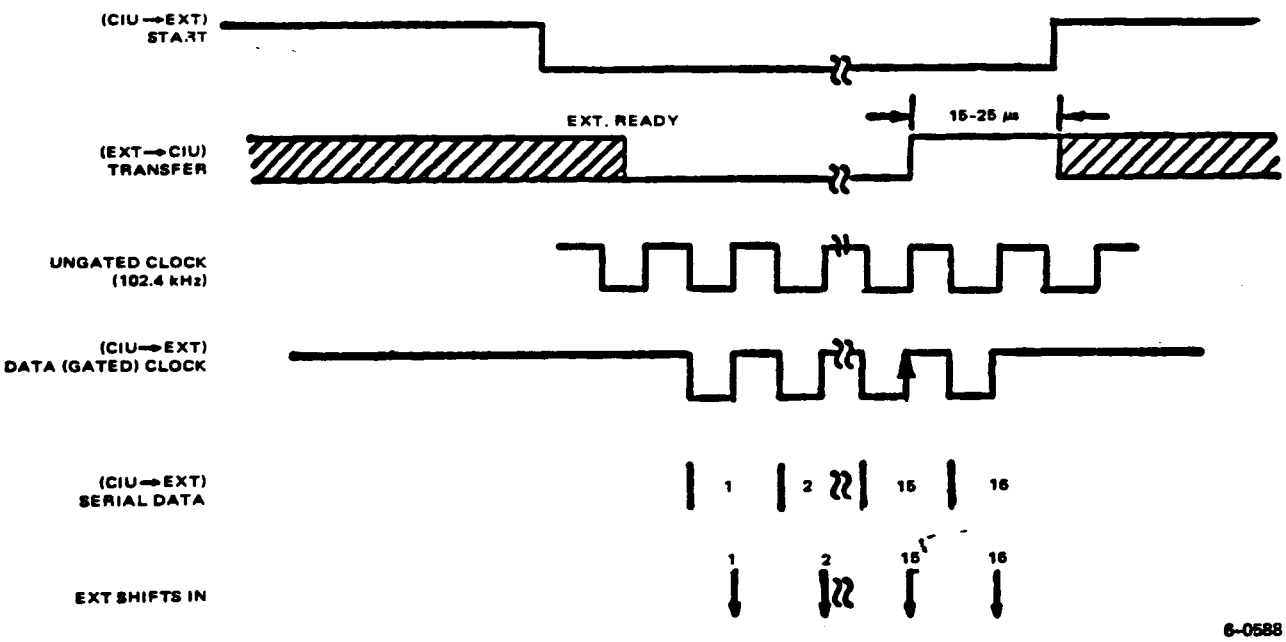

Figure 4.9.2-75. Data Transfer Timing Diagram

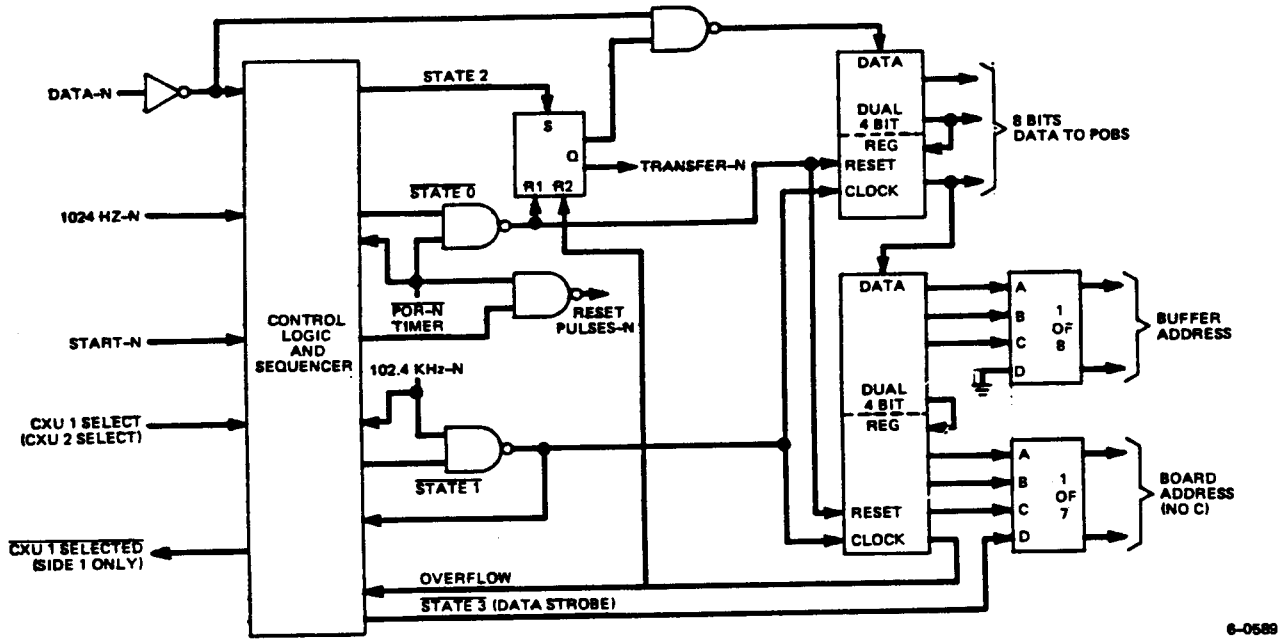

Figure 4.9.2-76. CXU Control and Output Logic

The execution of an input command sequence results in the storage of the data field of the command word into a Parallel Output Buffer (POB), see Figure 4.9.2-77. Each POB consists of an 8-bit register address decoding which can retain its contents statically until its address is detected. At that time it shall update its contents to the latest state of the data field. Two types of POB's are provided by the CXU for storage of level-discretes and pulse-discretes. Each I/O board contains eight redundant POBs and four are dedicated to each of the two types.

4.9.2.6.2.2.1 Level Discretes. Whenever bit 8 of the input command word is a data 0, the data field is to be stored in a POB dedicated to level discretes. In this case, each POB retains its contents until it is subsequently addressed with new data content. Any number from one to eight level-discretes may be simultaneously changed by a single input command. Each POB is initialized at power turn-on to be in the inactive state.

4.9.2.6.2.2.2 Pulse Discretes. Whenever bit 8 of input command word is a data 1, the data field is to be stored in a POB dedicated to pulse discretes. In this case, after the data has been transferred to the POB, the CXU initiates a timing function which causes all output pulse-discretes to become inactive after a period of 60 $\pm$5 milliseconds has elapsed. The input command repetition rate will not exceed one command word per 75 milliseconds. Any number from one to eight pulse-discretes may be simultaneously changed by a single input command. Each POB is initialized at power turn-on to be in the inactive state.

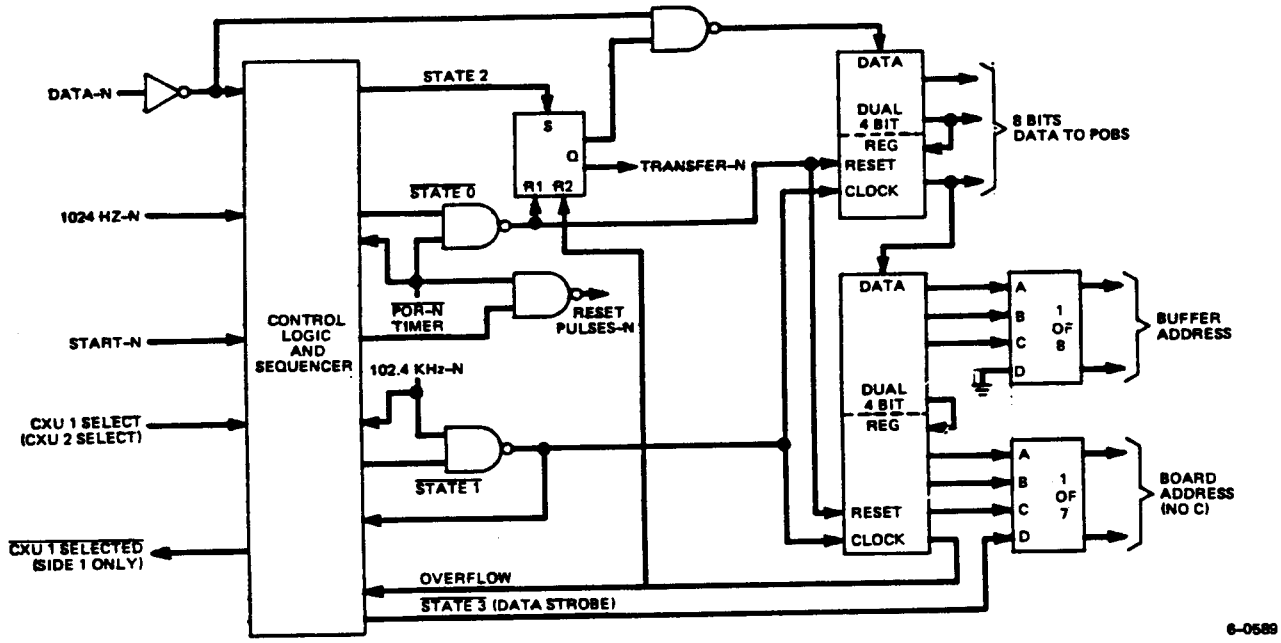

Figure 4.9.2-76. CXU Control and Output Logic

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4.9.2.6.2.2.2 Pulse Discretes. Whenever bit 8 of input command word is a data 1, the data field is to be stored in a POB dedicated to pulse discretes. In this case, after the data has been transferred to the POB, the CXU initiates a timing function which causes all output pulse-discretes to become inactive after a period of 60 $\pm$5 milliseconds has elapsed. The input command repetition rate will not exceed one command word per 75 milliseconds. Any number from one to eight pulse-discretes may be simultaneously changed by a single input command. Each POB is initialized at power turn-on to be in the inactive state.

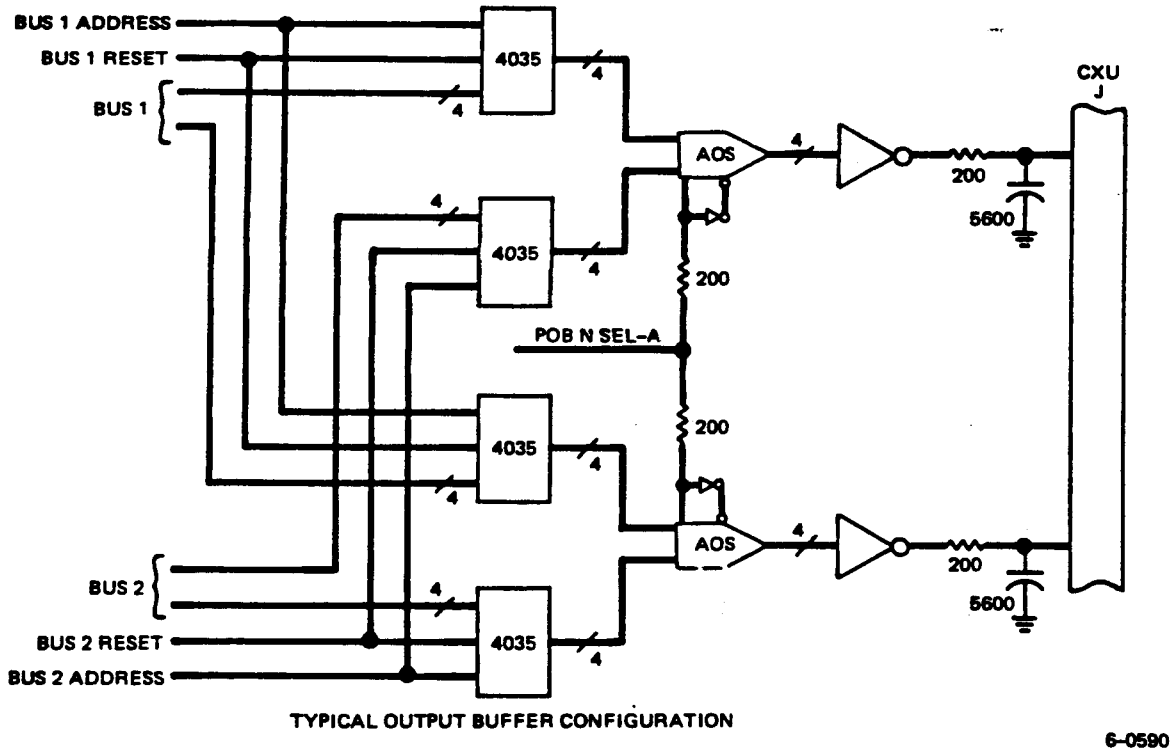


Figure 4.9.2-77. Typical Output Buffer Configuration

4.9.2.6.2.3 Command Word Format. The 16-bit command word will be received with bit 1 (MSB) occurring first in time. Bit 1 is unused, bits 2-8 contain a command destination address and bits 9-16 represent the 8 bit data field associated with the command address. Each bit of the data field corresponds to a unique command-discrete output signal. Command word bit 9 corresponds to bit 1 of an output buffer. The detailed bit assignments are specified below:

Bit No.	Function
1	Not Used
2-4	I/O Board Address (000 is invalid code)
5	Not Used
6-8	Buffer Address
9-16	Cmd Data to be Stored in Addressed Output Buffer

4.9.2.6.2.4 Timing. Timing of pulse discretes is accomplished by a CD4024, 7 stage counter, using a 1024 Hz clock as the timing reference. This method produces 62.5 microsecond pulse commands.

4.9.2.6.2.5 Power-On Reset (POR). The CXU provides a reset pulse which is generated at the initial application of the +10 volt power bus. This POR pulse is used to initialize sequential logic to a standby state and resets all command outputs to the inactive state.

4.9.2.6.2.6 Telemetry. The CXU provides telemetry discretes for the purpose of monitoring internal states. The bi-level telemetry signals are:

1. CXU Selection Status

   Data 0 = side 1 commanded decoder selected
   Data 1 = side 2 commanded decoder selected

2. CXU Bus Status

   Data 0 = side 1 output buffers selected
   Data 1 = side 2 output buffers selected

4.9.2.6.2.7 Physical Description. The CXU outline drawing is shown on Figure 4.9.2-78. The outline dimension of the CXU are 4.8 x 7.7 x 8.8 (inches). The CXU weights 4.8 lbs.

4.9.2.6.2.8 Output Buses. The CXU contains two output buses -1, and -2. Each bus is associated exclusively with a CXU side. Since both CXU sides process data simultaneously, both buses always contain the same data. The SELECT BUS 1/SELECT BUS 2 commands cause data on the selected bus to be connected to external units.

4.9.2.7 Decryption/Authentication Unit (DAU)

4.9.2.7.1 DAU Overview

The NOAA-KLM spacecraft has the capability to operate with an encrypted command uplink. Onboard the spacecraft, the Decryption/Authentication Unit (DAU) provides the means for converting the encrypted uplink back to plain text. The DAU consists of two redundant, continuously powered units within a common assembly. The functional organization of the DAU is shown in Figure 4.9.2-79. The DAU:

- Receives cipher text 64-bit command uplink from GRD
- Decrypts uplink command utilizing NSA KIR-23B cryptographic algorithm
- Authenticates uplink message, compares uplinked Vehicle Command Count (VCC) to DAU VCC
- Outputs clear text 32-bit command word to CIU for processing
- Decodes uplink command for decryption key selection and VCC change CMD
- Flags non-authenticated commands in telemetry and to the CIU
- Operates in one of two modes:
  - Clear or bypass mode
  - Decrypt and authenticate mode
- Contains a hardware timer which will command DAU to clear mode if a valid command is not received within 10-12 hours (Note: A software timer will also be provided)

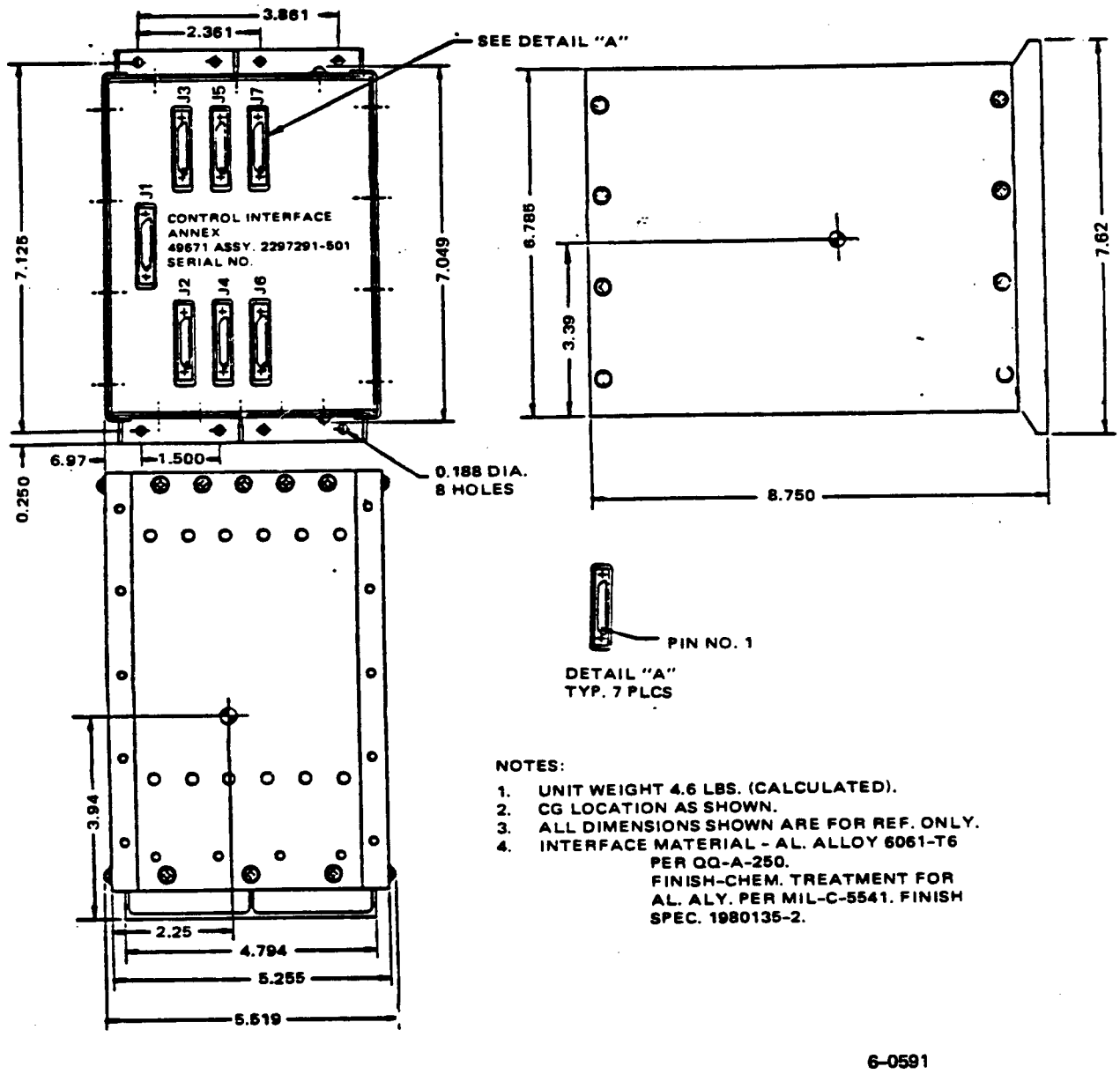


Figure 4.9.2-78. CXU Outline

Authentication of decrypted data makes command verification unnecessary. Any bit error in transmission will prevent authentication and the DAU will reject the command (VCC will not increment). After a rejected command, no command will authenticate because the VCC loses sync with the original sequence used for block encryption. A rejected command causes the CIU to begin looking for new sync. When in the Decrypt On mode, the DAU is readied for decryption/ authentication. The Decrypt On mode is set and reset with the decrypt signal. This signal must be asserted in order for the DAU to enter Decrypt On mode. The Decrypt On mode is active providing the decrypt signal is asserted. While in the Decrypt On mode, the DAU will perform decryption/authentication of the

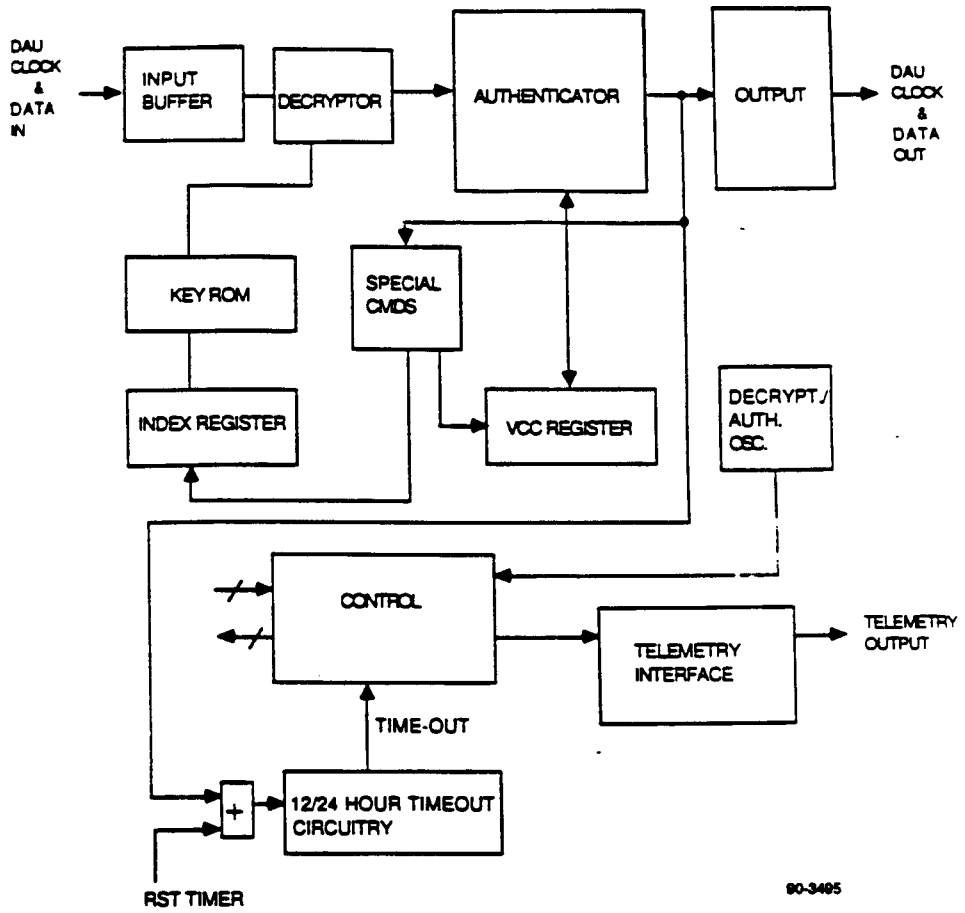


Figure 4.9.2-79. DAU Block Diagram

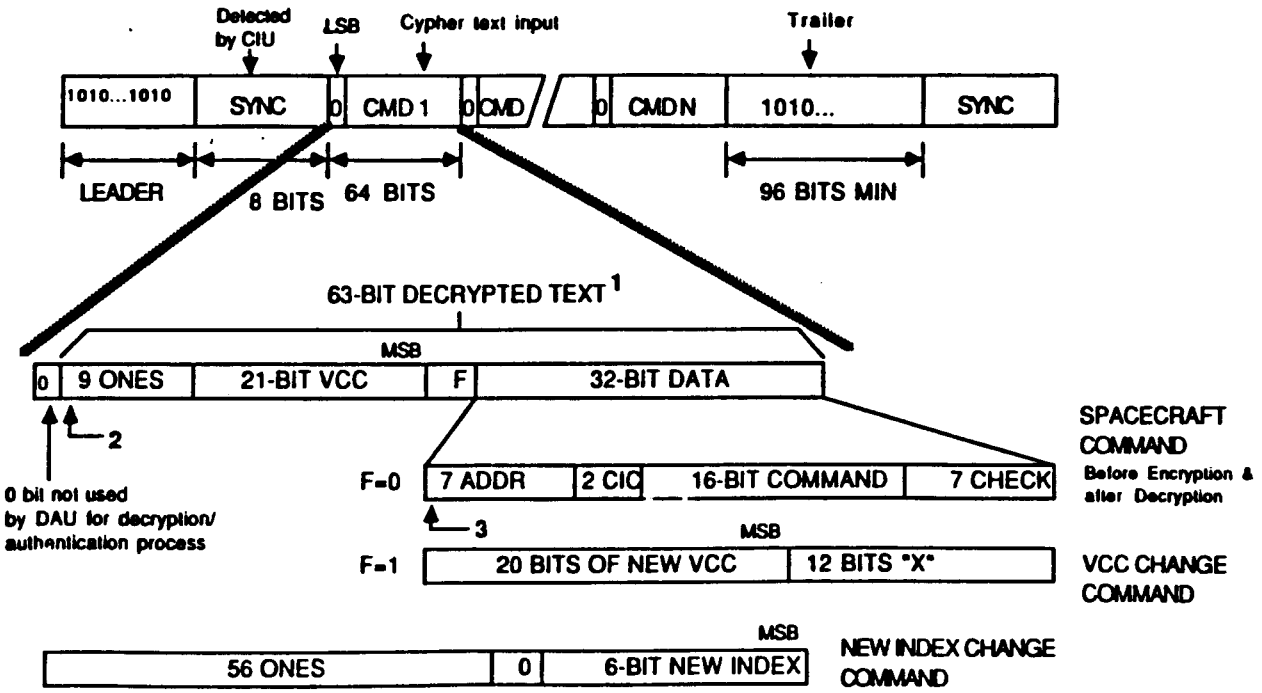
command data received from the GRD. The uplinked command data format will be comprised of 64 bits consisting of a leading zero followed by 63 bits of cipher text. The format for the cipher/decrypt command is shown in Figure 4.9.2-80. The current command will be decrypted and the decrypted message will be examined for a valid VCC as well as nine leading 1's necessary for authentication. All subsequent commands shall be subject to this process.

When the DAU is in the Decrypt Off mode, spacecraft commands do not pass through the DAU for decryption or authentication. The DAU enters the Decrypt Off mode whenever the decrypt signal is deasserted. The DAU maintains the encrypt signal deasserted in the Decrypt Off mode. No other signals are asserted to the CIU. The DECRYPT/AUTHENTICATE ON bit, BUSY, and COMMAND AUTHENTICATED bits of the serial telemetry data are all reset. The VCC is held constant. The timer shall be held reset while the DAU is in the Decrypt Off mode.

The decryption/authentication of decrypted command data as sent by the GRD will be bypassed if either of the two conditions is active:

a) The decrypt signal is deasserted, or

b) The encrypt signal is not asserted (however, this signal-affecting bypass of decryption would depend on system configuration).



NOTES: 1. This format corresponds to 63-bit plain text command before encryption.
2. First bit into encryptor.
3. First bit of plain text sent to CIU.

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Figure 4.9.2-80. Cipher/Decrypt Text

4.9.2.7.2 DAU Inputs

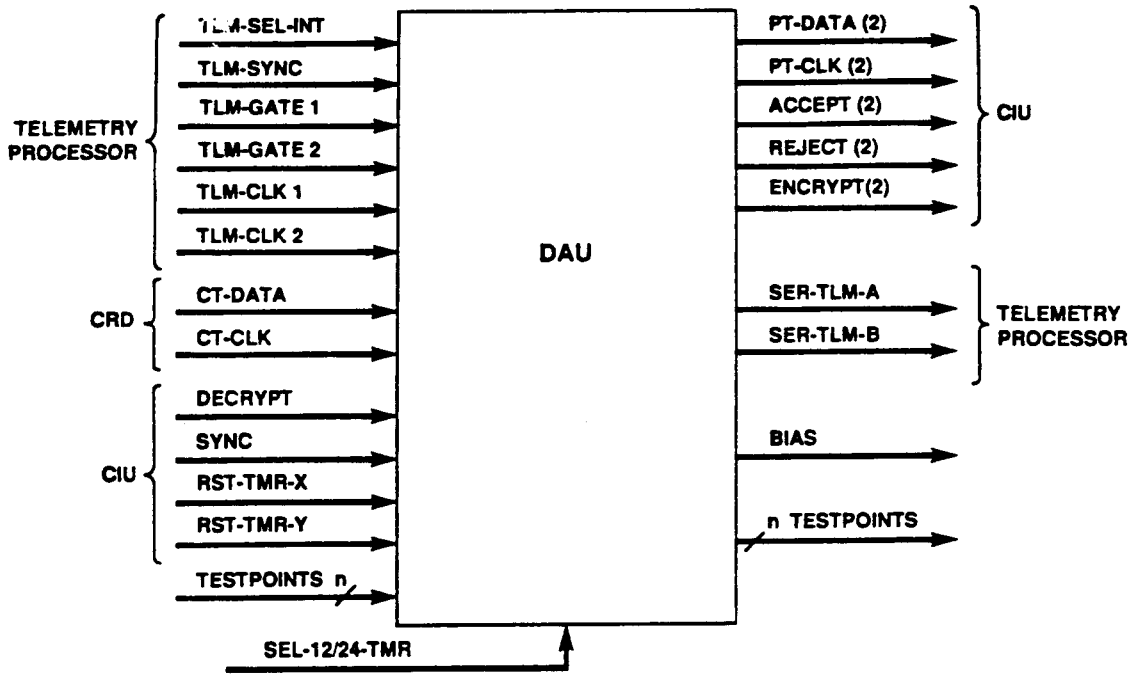
Interfaces between the DAU and the rest of the spacecraft are shown in Figure 4.9.2-81. Inputs consist of telemetry handshaking signals from the TIP, uplink data and clock from the GRD, and commands and synchronization from the CIU. The telemetry handshaking signals are described in the next section along with the corresponding telemetry outputs.

Each redundant side of the DAU receives two signals from the GRD: data and clock. All signal interfaces with the GRD are non-cross-strapped. Side 1 of the GRD interfaces only with side 1 of the DAU. Similarly, side 2 of the GRD interfaces only with side 2 of the DAU.

Each redundant side of the DAU receives the following signals from the CIU: DECRYPT, RST-TMR-X, RST-TMR-Y, and SYNC. A description of these signals is as follows:

DECRYPT: A logic level command from the CIU indicating to the DAU to decrypt encrypted messages from the GRD.

RST-TMR-X: A pulse command from the CIU which enables the reset of the DAU internal timer (provided this asserted pulse is overlapped with the [asserted] signal, RST-TMR-Y).



NOTES: 1. ONLY ONE REDUNDANT SIDE IS SHOWN.
2. THE 12/24 RESET MODE IS HARDWIRED BY THE SPACECRAFT HARNESS.

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Figure 4.9.2-81. DAU Box Interface Diagram

RST-TMR-Y: A logic pulse from the CIU which enables the reset of the DAU internal timer (provided this asserted pulse is overlapped with the [asserted] signal, RST-TMR-X).

SYNC: A logic pulse from the CIU indicating to the DAU to reset the decrypt/authentication logic and begin decrypting the next sequence of encrypted commands received from the GRD. The DAU will act upon the sync signal being asserted provided the decrypt signal is asserted.

4.9.2.7.3 DAU Outputs

The DAU outputs are shown in Figure 4.9.2-81 and consist of telemetry data to the TIP and command data and control signals to the CIU. The DAU telemetry consists of five words of Digital A data to the TIP from each DAU side, one word from each side of each minor frame. The five words are given in Table 4.9.2-29.

Each side of the DAU generates five words consisting of 8 bits per word. The data is transmitted most significant bits first.

A description of the telemetry output is as follows:

The KEY INDEX telemetry bits indicate the value of the current key index being used. The first bit transmitted shall be the MSB. At initial power turn-on, the key index is reset to zero.

TABLE 4.9.2-29. TELEMETRY WORD CONTENTS (FOR ONE REDUNDANT SIDE)

Word	Bits	Description
1	1-6	KEY INDEX BITS 5-0 (5 is MSB)
	7	POWER TRANSIENT
	8	BUSY
2	1	SIDE-1
	2	DECRYPT MODE ON
	3	TIME-OUT
	4	TIMER WARNING
	5	FILL STATE
	6	COMMAND AUTHENTICATED
	7	ROM PARITY ERROR
	8	VCC BIT 20 (MSB)
3	1-8	VCC BITS 19-12
4	1-8	VCC BITS 11-4
5	1-4	VCC BITS 3-0
	5	logic level 0
	6	logic level 0
	7	logic level 0
	8	logic level 0

The POWER TRANSIENT telemetry bit provides an indication that the 10 volt power to the decrypt/authenticate digital logic has dropped below a value in which the proper operation of the DAU cannot be ensured. Note that this measurement is of the 10V output from the DAU EPC board and not of the external bus power entering the DAU into the EPC. A power transient will be detected (for the nominal case) if the 10 volt level drops below 7.8 volts for a period of time exceeding 200 NS.

This bit is SET:

1) at initial power turn-on, or
2) at the occurrence of a power transient.

This bit is RESET:

1) following any decrypted/authenticated command.

The FILL STATE telemetry bit indicates that the last command decrypted/authenticated by the DAU is a VCC fill Command.

This bit is SET:

1) if a VCC fill command was successfully decrypted/authenticated, or

2) if a key index change command was successfully decrypted/authenticated with a current VCC of all 1's.

This bit is RESET:

1) following any decrypted/authenticated command which is neither a VCC fill command nor a key index change command, or

2) at initial power turn-on.

The VCC telemetry bits indicate the value of the current VCC being used. The first bit transmitted shall be the MSB. At initial power turn-on, the VCC is reset to zero.

The COMMAND AUTHENTICATED telemetry bit indicates if the last command processed by the DAU was successfully decrypted/authenticated.

This bit is SET by successful execution of:

1) a spacecraft command, or
2) a key index change command, or
3) a VCC fill command.

This bit is RESET:

1) if the last command processed is rejected, or

2) if the DAU is in the Decrypt Off mode, or

3) at initial power turn-on.

The BUSY telemetry bit indicates if the telemetry serial data which was last interrogated by the telemetry processor is questionable.

This bit is SET:

1) if the DAU telemetry is requested during a currently active authentication/decryption cycle or key ROM parity check.

This bit is RESET:

1) if the DAU telemetry is requested during a period in which there is no active authentication/decryption cycle.

2) at initial power turn-on.

The DECRYPT MODE ON telemetry bit indicates the current processing state of the DAU.

This bit is SET:

1) if the decrypt signal (to the DAU) is asserted.

This bit is RESET:

1) if the decrypt signal is deasserted.

The TIMER WARNING telemetry bit indicates that no command had been decrypted and authenticated by the DAU (while in the Decrypt On mode) for 8(20) hours since the timer reset signal was last initiated.

This bit is SET:

1) if 8(20) hours have elapsed without the authentication of any commands or without the receipt of the reset timer command, or

2) at initial power turn-on.

This bit is RESET:

1) if a command is authenticated, or
2) if the decrypt signal is deasserted, or
3) if the reset timer command is initiated.

The TIME-OUT telemetry bit indicates that no command was decrypted and authenticated by the DAU (while in the Decrypt On mode) for 12(24) hours since the timer reset signal was last initiated.

This bit is SET:

1) if 12(24) hours have elapsed without the authentication of any commands or without the receipt of the reset timer command.

2) at initial power turn-on.

This bit is RESET:

1) if a command is authenticated, or
2) if thee decrypt signal is deasserted, or
3) if the reset timer command is initiated.

The ROM PARITY ERROR telemetry bit will be set if a parity error occurs.

This bit is SET:

1) upon the occurrence of a ROM parity error.

This bit is RESET:

1) if no ROM parity error occurred during the specific parity check that the DAU is currently performing, or

2) at initial power turn-on.

The SIDE-1 telemetry bit will indicate which redundant side of the DAU is providing its five words of telemetry information as specified in Table 4.9.2-29.

This bit is SET:

1) if DAU side 1 is transmitting telemetry.

This bit is RESET:

2) if DAU side 2 is transmitting telemetry.

Each redundant side of the DAU outputs the following signals to the CIU: ACCEPT, PT-CLK, PT-DATA, ENCRYPT, and REJECT. A description of these signals is as follows:

ACCEPT: A logic pulse to the CIU indicating that the previously decrypted command was authenticated.

PT-CLK: This clock is sent with the decrypted output to the CIU. It maintains the same relationship with the output data as that clock from the GRD maintains with its data.

PT-DATA: This data line will output the decrypted message to the CIU. It maintains the same clock and data relationship as that clock and data being input to the DAU from the GRD. However, the output format is NRZ-L.

ENCRYPT: This signal, when asserted, indicates that the decrypt signal is asserted and time-out has not occurred (i.e., Decrypt On Mode is active). At initial power turn-on, the Encrypt signal is deasserted (i.e., Decrypt On Mode is inactive) as a result of the telemetry Time-out bit being set.

REJECT: A logic pulse to the CIU indicating that the previously decrypted command did not authenticate. A Reject pulse will also be issued on the occurrence of a Power Transient condition.

4.9.2.7.4 DAU Processing

The DAU and the CIU work hand in hand to locate, decrypt, authenticate, and execute commands.

The CIU sync signal is used by the DAU to reset the decryption/authentication logic. The ensuing 64-bit command will then be decrypted/authenticated (upon reception) and an accept or reject signal issued accordingly depending upon the success or failure to authenticate the respective command.

The DAU does not wait for the sync signal to be received before allowing the reception and decryption/authentication of a 64-bit command. As long as the Decrypt On mode and the cipher text clock to the DAU is active, the following

actions will be indefinitely repeated (a received sync signal will restart the sequence at action 1):

1) Upon reception of a 64-bit command data word, decrypt/authenticate the current command while beginning to receive a new 64-bit command data word.

2) Output an accept or reject signal and plain text data (as appropriate).

3) Continue with step 1.

Figure 4.9.2-82 shows the functional state diagram as performed by the DAU.

The 63 bits of cipher text embedded in the 64-bit command word is decrypted using the KI-23 algorithm. The key is one of 62 keys stored in a ROM and selected by a 6-bit key index word. This key index word is available in telemetry.

The validation process consists of comparing the VCC value stored in the DAU's VCC register to the VCC field of the current decrypted command. The value in the VCC register is the sum of the number of authenticated commands received since the last Fill VCC command and the last Fill VCC Command value. This value is available in the telemetry from the DAU. For authentication to be successful the decrypted command contains a 21-bit VCC code that must match the value in the counter. The decrypted command must also have nine 1's in the first 9 bits.

The decrypting algorithm uses a set of keys which are stored in a ROM. There are 64 locations in the ROM all of which will contain valid known keys. The all 1's index code is not used since it intentionally contains bad parity (for test purposes). However, it contains a valid and known key. The use of all 0's index code is limited to initial power turn-on and pre-launch field tests. Each redundant side of the DAU has a separate and independent key ROM.

There are five unique, unclassified keys used per DAU side and a common test key for both DAU sides. The key index selects the decryption key. Each key resides in a specific area of the ROM. The index points to the beginning of that key's location. This index consists of six bits and is selectable through a special format command. Each redundant side of the DAU has a separate and independent key index.

The DAU stores a 21-bit word to be used in comparing the 21 bits labeled VCC in Figure 4.9.2-80. Each redundant side of the DAU maintains a separate and independent VCC. At initial power turn-on, the VCC resets to zero. The VCC value is incremented by one after each authenticated command (the key index change command will not increment the VCC). The incrementing is performed only by the VCC counter associated with the redundant side which is processing the current command; therefore, the two VCCs generated by the redundant DAU normally will be different. The VCC is loadable through a special format command.

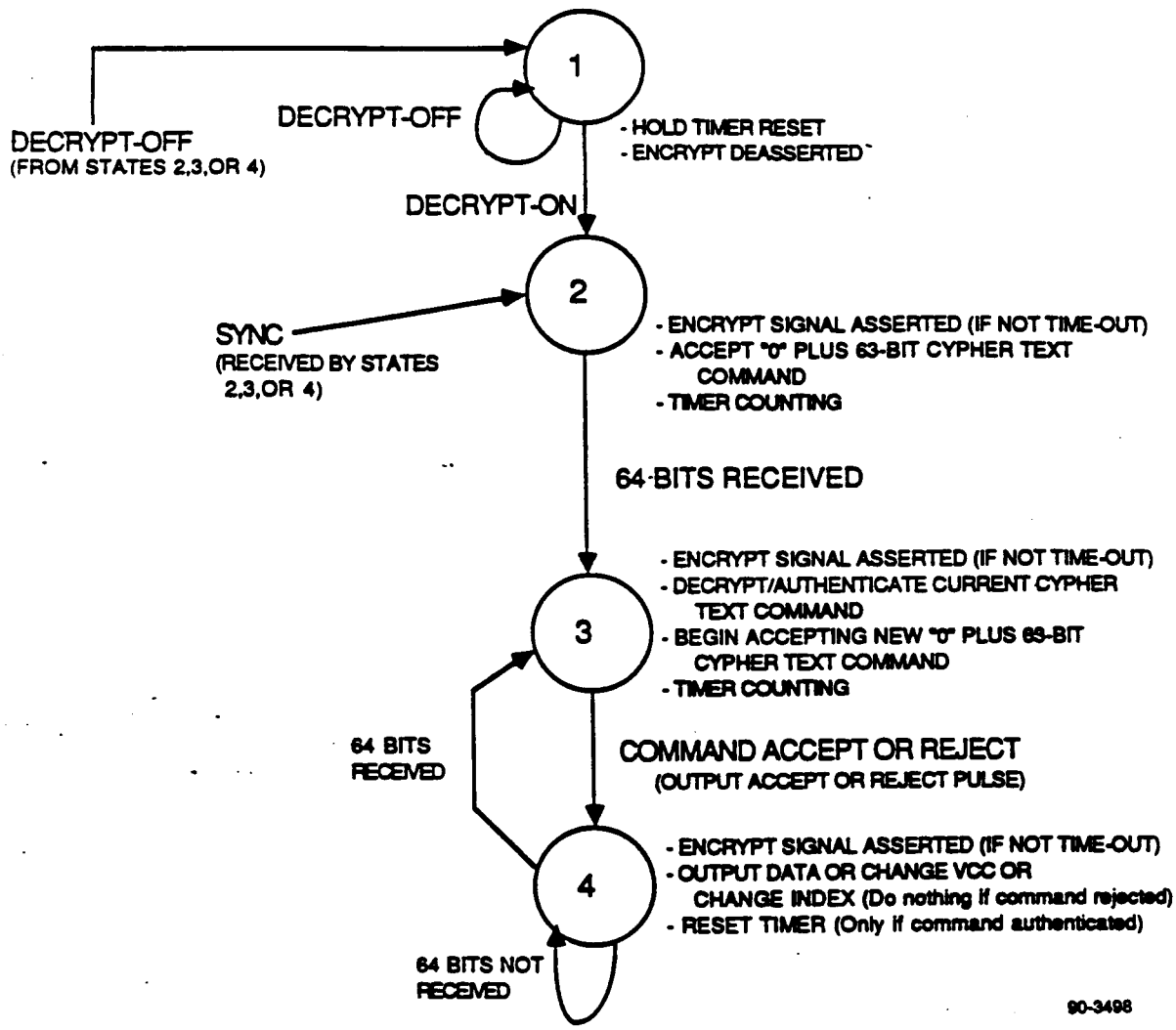


Figure 4.9.2-82. DAU Functional State Diagram

The load key index command implements a key index change. The format for this command is shown in Figure 4.9.2-80. The first 56 bits of the decrypted command contain 1's followed by one zero then followed by the 6-bit index code. The all 0's and all 1's key index (i.e., key 0 and key 63 respectively) cannot be selected.

The fill VCC Command format is shown in Figure 4.9.2-80. The first 9 bits of the decrypted command contain 1's followed by the current 21-bit VCC, a 1 in the fill bit, 20 bits of data for the new VCC and 12 unused bits. The 1 in the fill bit is used for the LSB of the 21 bit VCC so that an even VCC value cannot be loaded. The VCC shall not be all zeroes except on power turn-on.

The DAU will provide a timer used to detect the absence of an authenticated command within a pre-specified time period. An input pin will be open (tied low) for 12(24) hour timeouts. The TIMER WARNING status bit, a bit of serial

telemetry data, will be set when 8(20) hours have elapsed in the Decrypt On mode without the authentication of any commands and without the receipt of the reset timer command. The telemetry TIMER WARNING status bit will remain set until the timer is reset.

The following will occur if no command is successfully authenticated within the remaining four hours after the telemetry TIMER WARNING bit becomes set. The DAU will set the TIME-OUT bit in telemetry and deassert the encrypt signal to the CIU. These signals will remain in this state until the timer is reset. If during the remaining four hours an authenticated command is received, or a reset timer is received, then the telemetry TIMER WARNING bit will be reset.

The timer will be reset by any of the following:

a) Authentication of any command, or
b) Receiving a reset timer command, or
c) When the decrypt input signal is deasserted.

The DAU timer will be reset upon an overlapping assertion of the following two DAU input signals: RST-TMR-X and RST-TMR-Y.

When a spacecraft command has been authenticated, the DAU will:

a) Set the COMMAND AUTHENTICATED bit in the telemetry data (it will remain set by consecutive authenticated commands).

b) Add one to the VCC (Note that a key index change command will <u>not</u> increment the VCC by one).

c) For a fill bit equal to zero, send the 32-bit decrypted command to the CIU. Reset the FILL STATE telemetry bit (Note that key index change command(s) following a VCC fill command <u>will not</u> reset the FILL STATE telemetry bit).

d) For a fill bit equal to one, reload the VCC with the 20 bits fill VCC data in the command and the fill bit which sets the LSB of the VCC to 1. Set the FILL STATE telemetry bit.

e) Reset the timer.

f) Issue a command accept signal.

All VCC bits must be checked before a reject can be sent. When the stored VCC and the received VCC are not identical or the 9 leading bits are not all 1's or the decrypted command is not of the proper form, the command will be rejected. Under any of the above specified conditions, the DAU will:

a) Reset the COMMAND AUTHENTICATED bit in the telemetry data, and
b) Issue the command reject signal.

The response to a rejected command will not occur until all 63 bits of cipher text have been received and decrypted.

When the DAU receives a valid key index change command, the DAU generates a new operating key index. The DAU will not pass any serial data to the CIU. The DAU will issue a command accept response. The timer will be reset. The VCC register does not increment by one when this command is authenticated and executed. However the COMMAND AUTHENTICATED telemetry bit will be set.

NOTE: Performing a load key index command when the current VCC is all 1's (its maximum value), will set the FILL STATE telemetry bit. This is due to the command structure similarity between a VCC fill command (when the current VCC is all 1's) and a key index change command. This is not an error condition and the VCC register does not increment by 1 (i.e, remains all 1's).

When the DAU receives a valid VCC fill command, the DAU generates a new VCC. The DAU will not pass any serial data to the CIU. The DAU will issue a command accept response. The timer will be reset. The COMMAND AUTHENTICATED bit in telemetry will be set.

A ROM parity check is performed across the address and data lines of the key ROM against a bit stored in each word of the key ROM. The check is made during any of the following:

a) When changing the index, cycle the new key and accept the new key only if it does not show any parity errors.

b) Check the parity of the key in use during every attempt at decryption/ authentication.

c) When Decrypt Off mode is asserted, cycle the key ROM through all keys while checking for a parity error.

For each redundant side, the serial telemetry data will contain a ROM parity error bit.

The cipher data and clock entering the DAU is in NRZ-M data format with a bit rate of 2 Kbps, in which data is clocked on every positive edge of the input clock.

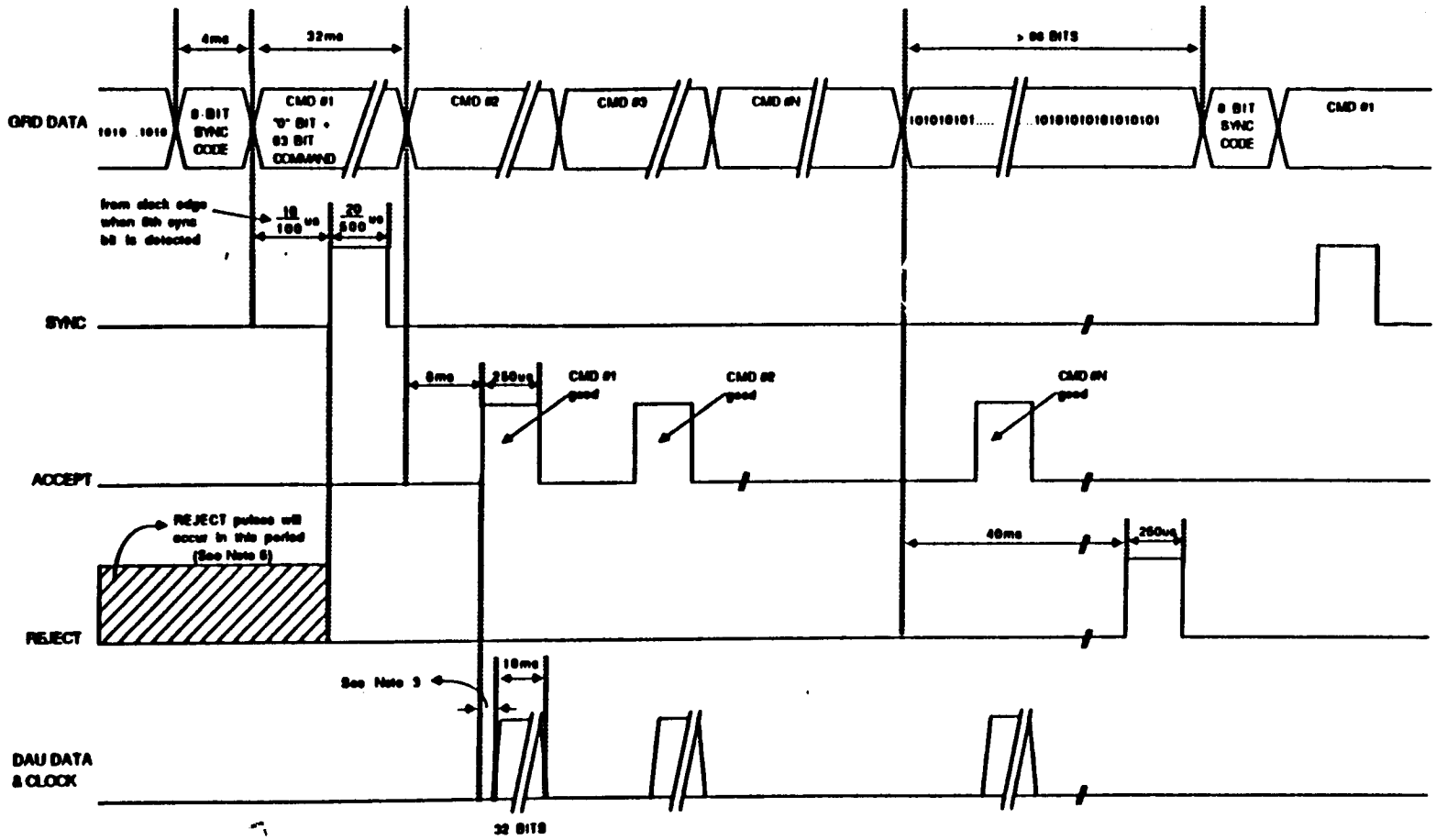
The decrypted output data exiting from the DAU and its associated clock are maintained with the identical relationship as the cipher data and clock input to the DAU. However the DAU output data format will be NRZ-L.

The signal timing relationships of the command decryption sequence is given in Figure 4.9.2-83. No decrypted data will be output from the DAU if the encrypted command is either a key index change command or VCC fill command. However, a command accept response will still be issued.

4.9.2.7.5 Commanding Operation Summary

Figure 4.9.2-84 depicts the interfaces between the GRD, DAU, and CIU. Figure 4.9.2-85 shows the necessary uplink for different modes of commanding. A summary of uplink commanding operations is given below.

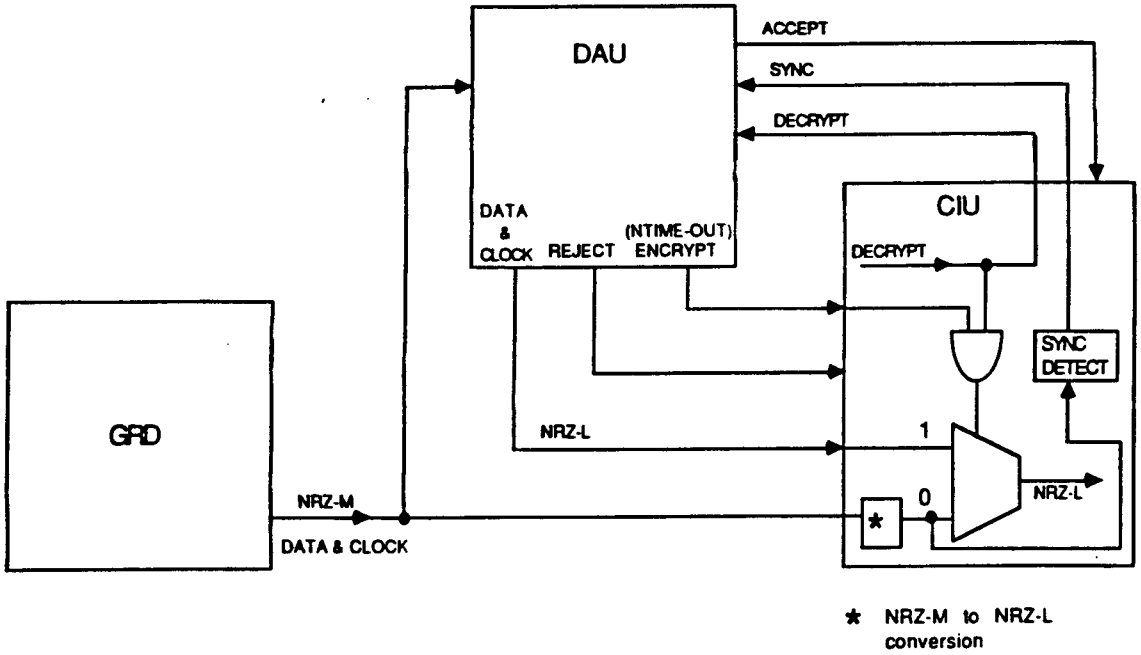
- Operation Sequence
  - All commands sent using DAU 1 key and DAU 1 VCC
  - DAU 2 key and DAU 2 VCC will remain unchanged



NOTES:
1. Timing Diagram is not drawn to scale.
2. All times shown are typical.
3. Leading edge of ACCEPT/REJECT pulse will occur 500us before output of DATA and CLOCK.
4. No DATA or CLOCK will exit DAU from a Key Index Change or VCC Fill command. However an ACCEPT/REJECT pulse will be issued as appropriate.
5. REJECT pulses will occur providing DECRYPT signal from CIU is asserted and GRD clock is active.

90-3499

Figure 4.9.2-83. DAU I/O Signal Timing



NOTES: 1. ONLY ONE SIDE OF THE COMMAND SYSTEM IS DEPICTED.
2. POSSIBLE CROSS-STRAPPING BETWEEN SIDES IS NOT SHOWN. 90-3500

Figure 4.9.2-84. Uplink Functional Block Diagram

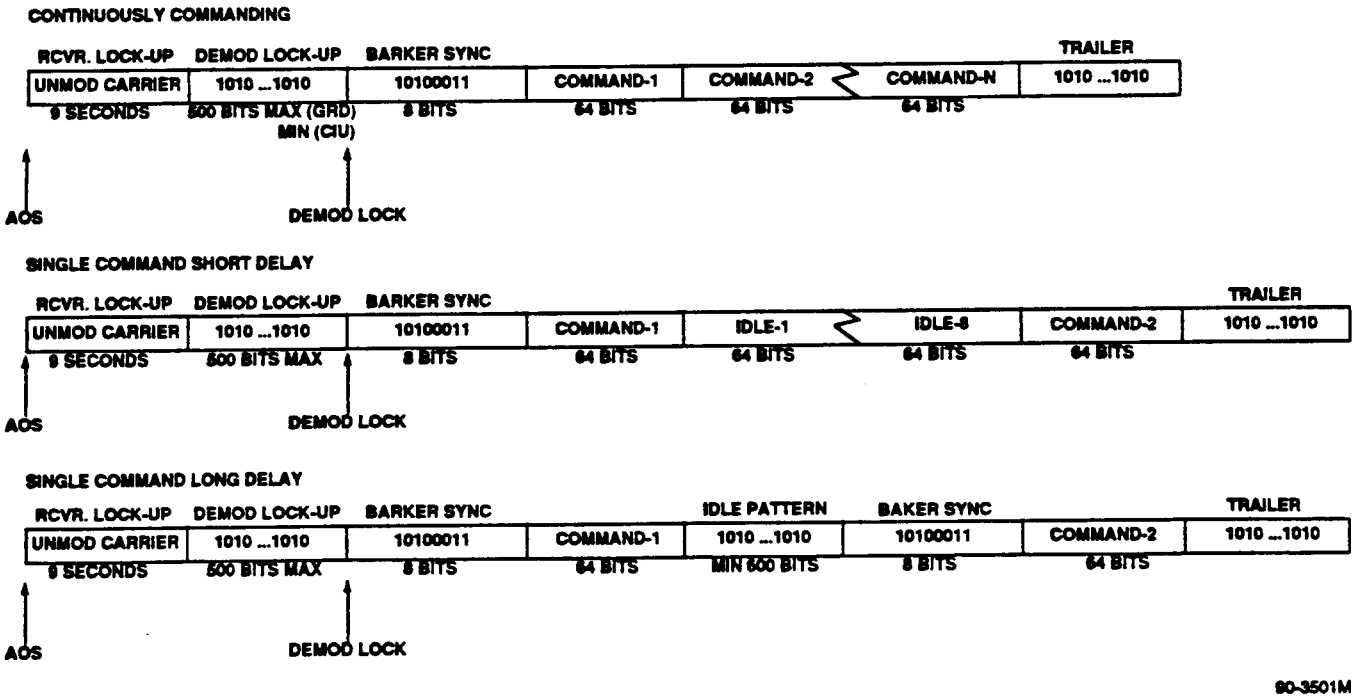


Figure 4.9.2-85. Uplink Format (Encrypted)

- DAU 2 will be "Hot Backup" key and VCC always known

- On selected DAU timer has no effect on either uplink processor

- Selected DAU timer will cause both uplink processors to go to clear path (encrypt signal)

- Command to go to clear mode (B10 Bus) will be from CIU buffer 138. Therefore, CPU 1 - affects only uplink 1, CPU 2 affects only uplink 2

- CIU buffer 141 (B10 Bus) will contain UP1 and UP2 clear/encrypt mode status for both CPUs

- The CIU will perform single error correction and double error detection on uplink data (32 bits)

- Control of DAU Selection

  - The control DAU will be determined by the CIU based on DAU accept and reject signals

  - Four consecutive accept with no rejects will trigger DAU selection

  - Identical to selection logic used on DMSP decryption system

  - Independent circuits for UP1 and UP2

- Uplink Sync Logic

  - The CIU will look for sync when

    - G data enable goes low (GRD demod not locked)
    - The selected DAU sends 9 consecutive reject pulses
    - The uplink processor detects a double bit error

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4.10 SPACECRAFT SOFTWARE ORGANIZATION

4.10.1 SYSTEM OVERVIEW

The Flight Software Subsystem (FSS) includes all programs intended for execution during operation of the ATN-KLM satellite. It also includes all data structures (variables, parameters, and constants) associated with the operation of these programs. The FSS forms a part of:

a. The Command and Control Subsystem (C&CS)
b. The Attitude Determination and Control Subsystem (ADACS)
c. The Ascent Guidance and Control Subsystem (AGS)
d. The Electrical Power Subsystem (EPS)

and as such, performs many tasks associated with these subsystems. It also performs tasks concerned only with the operations of the software and the cycling of the CPU.

4.10.2 OVERALL ORGANIZATION OF THE FSS

The major functions performed by the Flight Software are described in the following paragraphs:

Executive

The FSS provides for the execution of the various software modules and provides for the transition between the Ascent phase and the Orbit phase of satellite operations. In the orbit mode, the executive modules provide for the periodic execution of ADACS functions and allow for the timely execution of the Command and Control tasks.

Command and Control

As part of the C&CS, the FSS:

- receives real-time commands
- processes stored commands
- executes commands
- provides for loading and dumping the CPU memories
- provides CPU telemetry

Attitude Determination and Control

As part of the ADACS, the FSS:

- collects and processes ESA data
- collects and processes IMU data
- calculates S/C reference position data
- computes and issues control signals
- provides simulated sensor data for ground testing

Ascent Guidance

The Ascent Guidance Software is operable only before and during the ascent of the vehicle into orbit. Once its task is complete, control is given to the orbit phase software. The AGS replaces the orbit ADACS and assumes the executive functions when it operates.

Power Management

As part of the EPS, the FSS:

- performs routine battery and solar array calculations
- monitors battery parameters and efficiency
- monitors solar array parameters
- triggers power economization functions
- performs a battery reconditioning function when required

Data Storage

The FSS also includes areas of global variables and stored command data. Also included in this group are Ephemeris and CPU telemetry data.

4.10.2.1 Definition of Executable Modules

The Flight Software is composed of the following modules. Each module functions as described in Section 4.10.9.

AGS, HAND, RWACS, and SOPS operate in the ascent mode.
MEMCHK, ITEST, LIBRY, CMDPRO, and RTP operate in both modes.
All other modules operate in orbit mode.

Executive

TIREX. This program provides the operating system for both the cyclic tasks and the interrupt-driven tasks, when in the orbit mode. A routine named CYCLE activates those modules which require processing at 10 Hz.

TSRS. This module interfaces with the TIP and collects the TIP subcom data for further processing.

MODE. This module schedules those cyclic tasks which execute at 2 Hz time; mainly ADACS and Stored Command processing. It checks that lower levels have run to completion and takes corrective action as necessary. It supervises hardware redundancy. This module issues the "MEOK" signal which keeps the CPU "on-line".

STESM. This module provides a series of commands which place the satellite into a known, safe, reduced power mode of operation.

HAND. This module performs the transition (handover) from the ascent phase of operation to the orbit phase in the CPU which is in control during ascent.

SOPS. This module performs the rudimentary executive functions in the Standby CPU during the prelaunch and ascent phases. It also provides the transition to orbit mode operations in that CPU.

CARP. This module responds to CPU alarms, providing both telemetry via CTEL, and memory dumping via GDUMP. Control is returned to TIREX at the next 2 Hz interrupt.

MEMCHK. This module performs a summation on the contents of selected segments of memory and sets a flag if the value does not agree with the expected value. It is used in the background as a check on memory integrity.

ITEST. This module performs a periodic check of the CPU instructions by executing a predetermined sequence in both single and double precision.

CTEL. This module interfaces with the TIROS Information Processor (TIP), and provides a commutated set of data words from the CPU memory at regular intervals for inclusion in the telemetry frame.

LIBRY. This module provides the following mathematical functions: sine, cosine, arctangent, magnitude of a vector, rotation of a vector, square root. These routines execute on the level at which they are invoked and are intended for use by ADACS only. In addition, LIBRY includes a data-move routine to operate on Level 15 (PRIVMOV) which is available to all lower levels.

Command and Control

POPS. This routine is permanently engraved in Read Only Memory (ROM) of the CPU and provides for memory load, dump and CIU buffer initialization when the CPU is cold-started, or whenever the C/C software is not resident in memory.

XPOPS. An extended software version of POPS that may be used after cold-starting a CPU. An instruction set larger than POPS is featured.

RTP. This module responds to interrupts from the uplink processor, examines and collects the uplink words into command sequences for execution by CMDPRO. RTP also performs the memory loading function.

CMDPRO. This program tests and executes all real-time, stored, and internally generated command sequences.

The routines CVQI and CVQO maintain a queue of Command Verification information. Routine TIKS assists in executing commands which require delayed action.

SCPRO. This module extracts stored command sequences from a table and passes them to CMDPRO for execution, based on a Command Clock.

GDUMP. This module interfaces with the TIP and transfers the contents of selected segments of CPU memory to the TIP for inclusion in the telemetry frame. This is initiated by a special series of dump commands.

Attitude Determination and Control

GEODAT. This module provides the necessary satellite, sun, and moon position data with sufficient accuracy to allow nominal attitude maintenance. It also provides sun angle information for use in positioning the solar array.

ESRS. This module responds to interrupts from the Earth Sensor Assembly (ESA) and collects and formats the data for later use by ADS.

DFS. This module collects and filters the data from the IMU (gyros).

ADS. This module uses the ESA and IMU data to determine the instantaneous attitude of the satellite. By comparison with the reference position it computes the attitude errors and rates.

ACS. This module implements the attitude control laws and generates control signals based on the attitude error history.

MMUS. This module directs the unloading of momentum from RWAs under normal circumstances. It uses magnetic latitude information from GEODAT, and provides the necessary coil commands to ACS.

SADCS. This module interfaces with the Array Drive Electronics (ADE) and provides control signals to keep the array tracking the sun.

ADACTEST. This module provides simulated nominal orbit (or other predetermined) input data for use in ground testing (spacecraft integration and prelaunch). Different test states are commandable, and ADACTEST is prevented from operating after launch.

SADTEST. This module provides simulated nominal or test-specific Solar Array Drive responses to commands issued by SADCS. SADTEST is prevented from operating after launch.

Ascent Guidance

AGS. This module provides the executive and vehicle control functions in the master CPU during the ascent guidance phase of operations. It provides prelaunch testing. It navigates from liftoff to separation from the Atlas and provides guidance from separation to handover to orbit mode.

RWACS. This module, operating in the master CPU during ascent, runs all four reaction wheels at a constant speed to protect the bearings.

Power Management

PMS. This module performs the routine battery and solar array calculational functions.

PSSS. This module economizes on power consumption by activating STESM, and CTCES, thus putting the spacecraft into a known state of low power consumption.

CTCES. This module controls a ground defined set of TCEs to be cycled.

BATREC. This module controls the charging of the batteries during a ground initiated reconditioning event.

Data Storage

SCTABL. This area contains commands to be processed by both the SCPRO and the CMDPRO module of the C&CS.

TNPOOL. This area is the global data area for use by all other program modules.

GPNOMNL. This area contains nominal Ephemeris data to be used for test purposes. The true Ephemeris data is loaded into this area just prior to launch time. The Ephemeris is used by GEODAT.

NOMLIMUK. This area contains nominal IMU parameters used for test purposes. AGIMUCAL is overlayed into this area for the Flight Load Package (FLP).

UVERSION. This area contains the load package spacecraft ID codes.

UCPUTLM. This area contains CPU-specific telemetry data.

MISSIONK. This area contains ascent guidance parameters specific to one of the two possible orbits utilized in the TIROS system.

AGIMUCAL. This area contains ascent guidance parameters specific to the IMU to be used.

CALIN. This area contains calibration and alignment constants for the IMU and ESA.

UMCON (1 & 2). This area contains other mission constants not specified in earlier data areas.

Applications

NULS. This program commands a backup momentum unloading capability to counteract disturbances which exceed the capability of the magnetic system. Module ATMUL (Automatic Thruster Momentum Unloading) monitors system momenta (body and reaction wheels) and sequences events of the unloading cycle. Module TCNTRL (Thruster Control) commands 0.1 second pulses of the nitrogen thrusters.

4.10.2.2 Load Package Organization

Ascent, Handover and Orbit mode software are assembled starting at fixed locations in a Unified Load Package (ULP.) The ULP can be altered to produce a Test Load Package (TLP) for test purposes. The final package loaded into the spacecraft is designated the Flight Load Package (FLP.) The FLP contains a ULP plus an additional data area containing the modules AGIMUCAL, CALIN, and UMCON 1 or UMCON 2 (depending on whether the FLP is loaded into CPU 1 or CPU 2 respectively.)

Various modules operate at different times. The regime of operation is shown in Figure 4.10.2-1. The software for the ascent phase also operates in the prelaunch phase. The transition to orbit phase is very short (approximately 2 seconds).

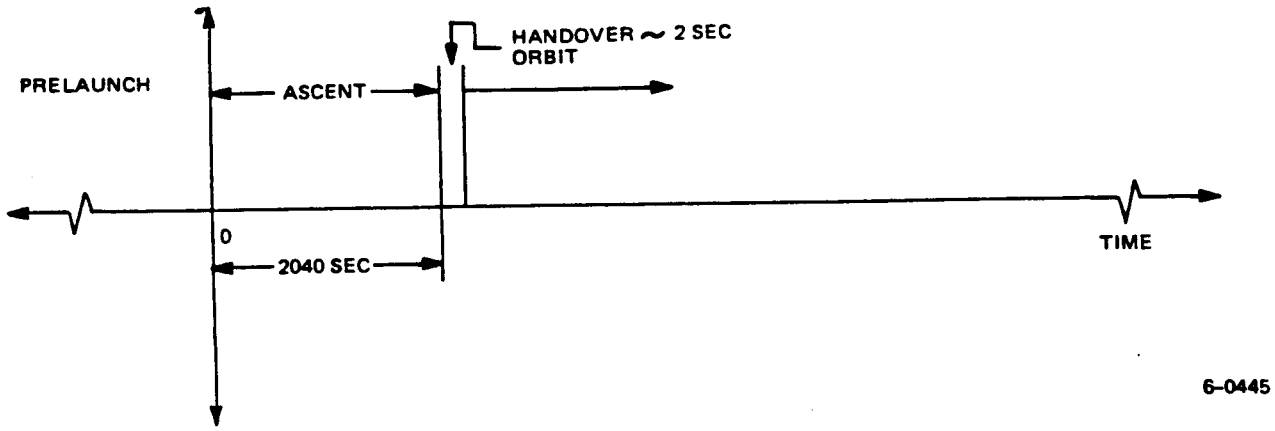

Figure 4.10.2-1. Temporal Phases of Software Operation

4.10.2.3 Priority Levels and Interrupts

The CPU provides for 16 priority levels of operation. These are controlled by an interrupt structure which can be activated by either the CPU software or an external interrupt requested through the CIU. These levels are used to provide a hierarchical structure, through which the various tasks can be performed on a timely basis. The assignment of interrupts to the priority levels is listed in Table 4.10.2-1 for orbit mode.

The assignment of the levels and the external interrupts is based on the expected rate of execution of the software modules, and the allowable delay in responding to external requests for service. These rates and delay times are also shown in Table 4.10.2-1.

Figure 4.10.2-2 is a hierarchy of the orbit phase flight software showing the precedence of calls to routines and subprograms. All the interrupt handling and level executives are considered part of TIREX.

4.10.3 PROGRAM OPERATION

The following paragraphs discuss the overall operation of the software in various modes. More detailed descriptions of AGS, C&CS, ADACS and PMS software follow.

4.10.3.1 Ascent Mode Operations

Ascent Guidance and Master CPU Operation

During ascent, AGS has control of the master CPU, which is placed on the B-bus, which is the selected bus. AGS controls the vehicle during ascent. AGS

TABLE 4.10.2-1. PRIORITY LEVELS, INTERRUPTS, AND PROGRAM EXECUTION - ORBIT MODE CONTROL CPU

Interrupt Source		Level	Programs	Activation Rate	Max Delay Permitted	Max Normal Execution Time Allowed
H/W	S/W					
CPU		16	CARP	Alarm only	0	500 ms
	FSS	15	PRIVMOV	Irregular	0	1 ms
		14	Reserved-Ground Testing			
	FSS	13	CMDPRO	Irregular	0	4 ms
CIU		12	RTP	62.5 or 31/S max**	2 ms	1.5 ms
TIP		11	CTEL	10/S	25 ms	2 ms
TIP		10	GDUMP	20/S	25 ms	3 ms
IMU		9	CYCLE, DFS, CVQO, TCNTRL	10/S	10 ms*	12 ms
CIU	CYCLE	9	MODE	2/S	50 ms*	20 ms
ESA		8	ESRS	8/S	20 ms	3 ms
TIP		7	TSRS	10/S	20 ms*	4 ms
	MODE	6	ADS, ACS, GEODAT	2/S	100 ms*	75 ms
		5	(Spare)			
	MODE	4	SCPRD, TIKS	2/S	500 ms*	15 ms
	MODE	3	ATMUL, MMUS, SADCS	2/S	500 ms*	40 sec
	MODE	2	PMS	2/S	1 sec*	100 sec
CPU		1	MEMCHK	Background	2 sec*	200 sec
			ITEST	Background		

*Suggested to avoid degraded performance.
**In clear or decrypted mode, respectively.

NOTES: Periodic interrupts are synchronized (bear fixed relationships). Times for programs include calls to CMDPRO,PRIVMOV, and subroutines.

Although levels 6, 4, 3, and 2 all execute at 2Hz, distribution of programs reflects relative importance and allows better monitoring by the executive (MODE).

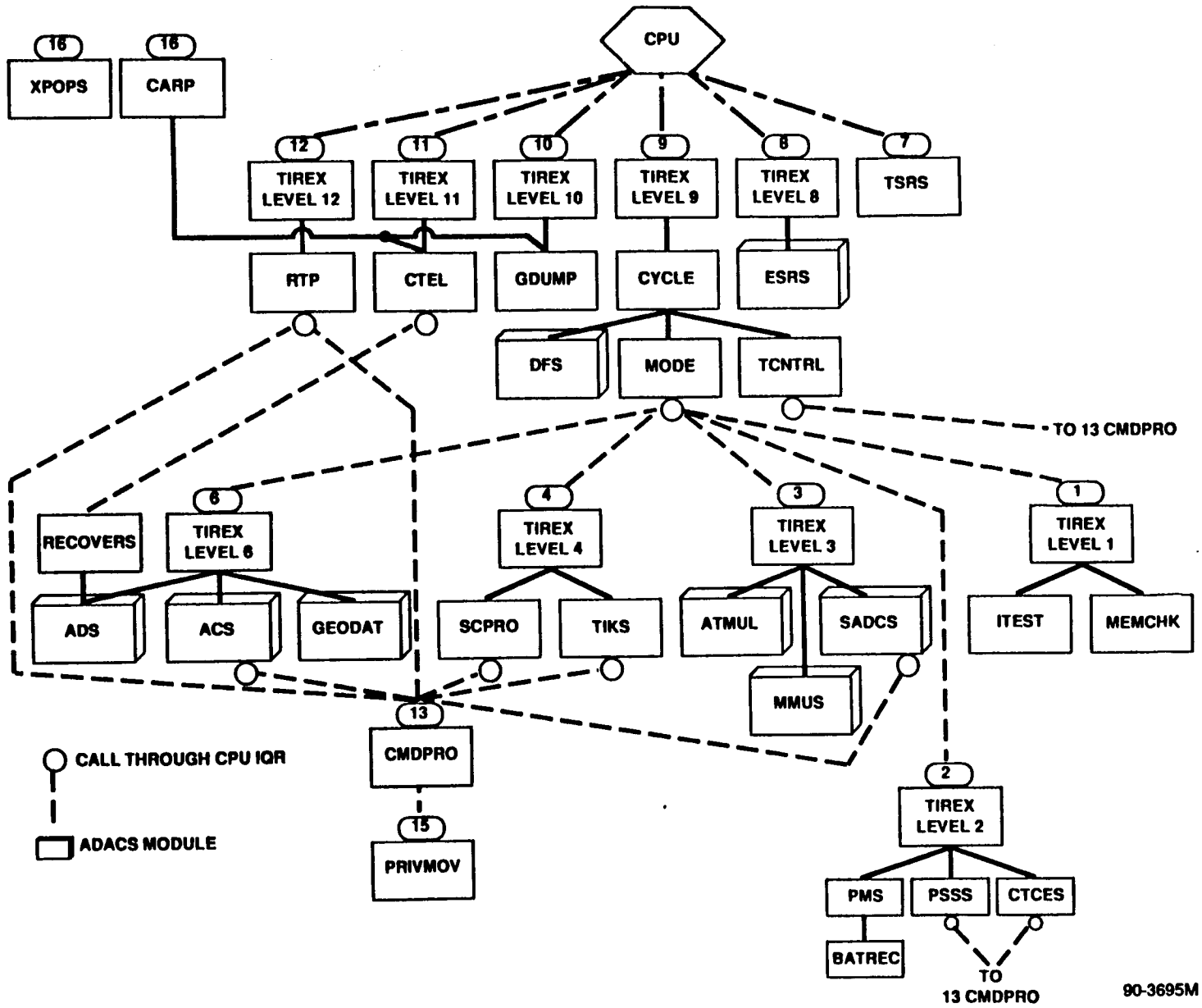

Figure 4.10.2-2. Orbit Phase Software Hierarchy

navigates, guides and controls the vehicle during this phase. At the end of the ascent guidance phase, AGS provides a coast phase during which it will turn the vehicle into the orbit orientation, and provide a series of discretes to effect the required deployments. At the appropriate time, AGS turns control over to HAND.

4.10.3.2 Handover Mode Operations

HAND completes the handover to the orbit mode software, placing the CIU and IMU in the orbit mode of operation. Other discretes are issued as necessary to place the satellite in the proper configuration. HAND insures that the system continues to execute with the master CPU on the B-bus. HAND terminates its operation by handling control to TIREX and the orbit software.

Ascent phase operations in the standby CPU.

The program SOPS has control in the standby CPU during prelaunch and ascent. It permits real time commands to be executed via RTP and CMDPRO. Upon receiving a signal from the master CPU it performs handover in the standby CPU. SOPS also performs handover independently of the master CPU if the signal is not received within 2500 seconds after liftoff.

4.10.3.3 Orbit Mode Operations

Command and Control Subsystem

The master CPU (chosen by ground command or CIU logic) operates on the selected bus. It accepts and executes real-time commands at up to 31 words per second when encrypted or 62.5 words per second when in the clear mode, providing command verification and error messages at a maximum rate of one per 0.1 seconds. It provides for the testing and execution of stored commands from a sequential list with a time resolution of one second. The table provides for 2048 entries (commands and data words).

The standby CPU also provides for real-time and stored command processing; however, only the control CPU may access the selected CIU bus. It is not necessary to provide commands to the standby CPU. Each CPU provides for CPU telemetry at the rate of 30 words per second. This is interrupt driven: 10 interrupts per second, 3 words per interrupt.

Each CPU provides the capability to dump selected portions of memory upon command. The dump function is designed for a maximum rate of 20 interrupts per second with 3 words transferred per interrupt. It protects against spurious interrupts on the dump buffer link.

It is possible to load the memory of either CPU by command at the maximum rate of 62.5 words per second.

All commands, telemetry and dump functions operate while the CPU software performs its cyclic ADACS and executive tasks. The overall design of the software insures that the system continues to operate in the presence of maximum uplink interrupts of 62.5/sec. with simultaneous dump or telemetry. The system protects against spurious interrupts at higher rates. The software provides for all functions specified in the Command and Control Subsystem.

Attitude Determination and Control Subsystem

Each CPU contains the software necessary to effect the ADACS function. Only the master CPU actually performs this function. The standby CPU performs such portions of this as are necessary to permit it to assume the task if it becomes the master CPU.

The ADACS software reads the SSA, ESA and IMU data, and filters the IMU data to eliminate the structural frequencies from the control passband. The IMU data is sampled and filtered at a rate of 10 per second. The ESA is sampled at 8 per second.

This software provides for the calculation of attitude errors and rates as discussed in the ADACS Section 4.4. These errors are used to compute torque commands to the RWAs, control the momentum unloading coils and affect other control functions.

As part of the ADACS software, the FSS provides for the calculation of satellite position and the relative position of the sun/moon. It also provides for the overall control and pointing of the solar array drive.

Executive Control

Each CPU provides executive control functions which insure that the command/control and ADACS functions execute as required, and that in the event of a failure, suitable recovery procedures are taken.

The executive mode provides a MEOK each 0.5 seconds when the software is executing correctly or while suitable fixup action is being taken. When the software (or hardware) has been determined to have failed, the MEOK is not issued. This affects the status of the CPU, marking it as not OK.

The MODE software takes cognizance of the present OK status and past status. In the event that the master CPU fails (not OK) it enters a quiescent mode. If the (previously) STANDBY CPU becomes MASTER, it places the satellite in a safe state using the Software to Establish Safe Mode (STESM), and then performs the normal operations of the Control CPU.

Each CPU contains software to perform a background check on the CPU instructions (ITEST) and to continually checksum the memory (MEMCHK). The output of these tests are incorporated as part of the status testing.

Each CPU contains a program to respond to CPU alarm interrupts (CARP).

The control CPU provides software to collect and aggregate the TIP Subcom data.

4.10.4 MODE CONTROL AND EXECUTIVE SOFTWARE

The ATN-KLM Command/Control System uses two redundant CPUs in a configuration that permits the ground controller to choose the basic operational configuration, while providing for autonomous in-orbit control by the on-board systems. This is considered part of the command/control subsystem and is discussed in Section 4.9. The software modules TIREX and MODE are at the heart of this control. TIREX is the executive and MODE is the master control for periodic software execution.

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This section provides a discussion of the basic philosophy of the operation and the implementation of MODE.

4.10.4.1 Operational Philosophy

The two computers operate such that a single CPU is in "control" (i.e., performing all required tasks) at any one time. The second CPU operates in a standby mode such that it is ready to assume control if the system indicates a failure in the control CPU.

All routine operation of the spacecraft is effected through the control CPU. This includes autonomous attitude control, processing of stored commands, real-time commands, and other routine tasks for the continued operation of the system.

The control CPU makes full use of the available redundancy, and in general, it is not necessary to wait for a ground command to switch to a redundant ADACS unit, or CIU bus.

The checking of a CPU for faults or errors (self-check) includes a check of the memory contents (instructions and constants), where such contents are known and constant, a test of the CPU instruction set, and a test of the interface with the spacecraft (i.e., the I/O bus and CIU).

CPU failure testing continues to use the required active response (MEOK) on a periodic basis, and failure of the CPU is indicated after the absence of three successive MEOK. The criteria for not issuing MEOK includes a failure of the additional self-checks.

When the control CPU fails (the hardware indicates that the secondary CPU is now in control), the standby CPU assumes control. Before proceeding with the routine operations, it establishes the configuration of the system by setting (resetting) or otherwise commanding the available functions and equipment into a known state. The intent of this is to maximize the survivability of the system. The "failed" off-line CPU is not allowed to issue commands on the selected control bus.

The standby CPU provides for safe autonomous operation and control until the ground controller can react. This requirement implies that after takeover, the standby CPU provides the full spectrum of redundancy management and control.

If it is determined that the original control CPU has indeed failed, it is possible to operate the system with the remaining CPU.

4.10.4.2 Mode Switching

The CPU mode switching is shown in Figure 4.10.4-1. There are four operational states:

C (Control)	-	Nominal state of the selected CPU
S (Standby)	-	Nominal state of the secondary CPU
SC (Safe Control)	-	Takeover state of the secondary CPU
OL (Off-Line)	-	"Failed" CPU state

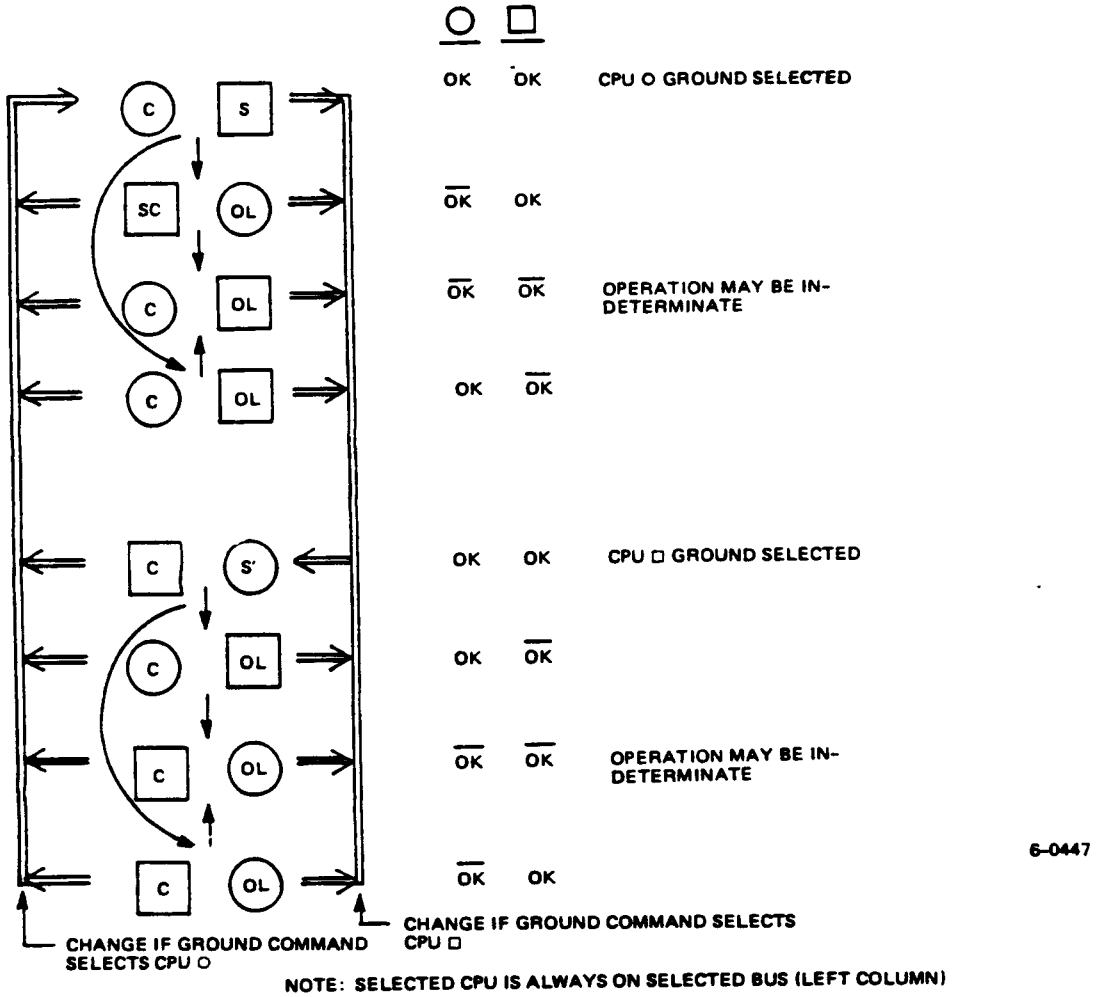

Figure 4.10.4-1. CPU MODE States

The major operating functions of the four states are described in Table 4.10.4-1.

The operation proceeds as follows:

(1) The SOCC selects a bus via CIU decoded command.

(2) The SOCC selects a CPU via CIU decoded command.

(3) Each CPU requests the CIU to place it on the selected bus. Only the Selected CPU will have its request granted.

(4) This establishes the nominal mode of operation. The selected CPU will CONTROL and will be on the Selected bus.

CPU failures (No MEOK) will result in mode changes as shown in Figure 4.10.4-1. If the standby CPU fails first it will be inhibited from assuming control.

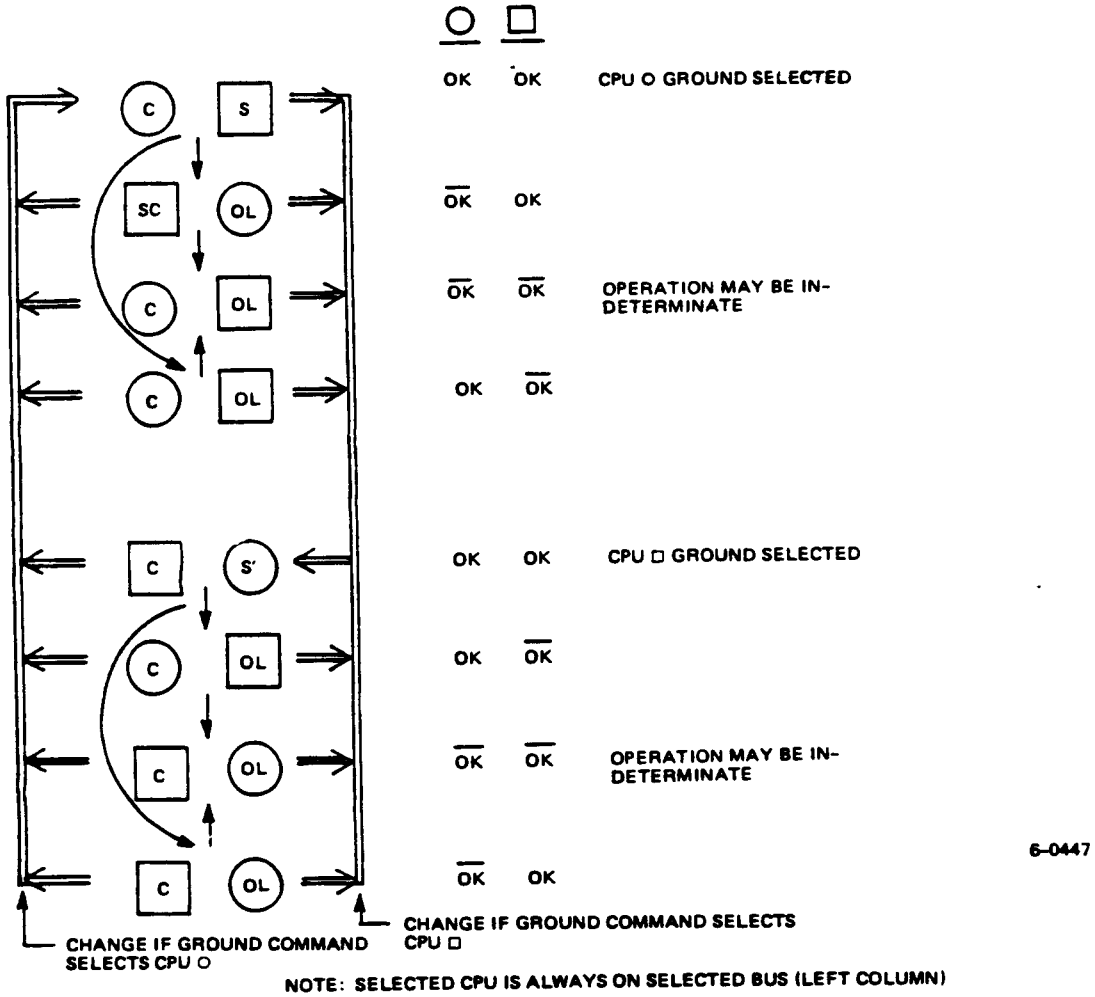

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TABLE 4.10.4-1. CPU SOFTWARE STATES

Failed State - System Operation	
Safe Control • Command/Control - Real Time - Stored CMD Capability • Establish Safe State • All ADACS Modes • Redundancy Management • CPU Telemetry • Self Check	Off-Line • Command/Control - Real Time • Minimum repetitive operations • CPU Telemetry • Provide C/C functions to allow diagnostics • Operation of failed CAP cannot be insured
Nominal State - System Operation	
Control CPU Functions • Command/Control - Real-Time CMD - STORED CMDS • Attitude Determination & Control • CPU Telemetry • Self Check •Redundancy Management	Stand-by CPU Functions • Command/Control - Real-Time Capability - STORED CMD INHIBITED • CPU Telemetry • Software Housekeeping - Clock Updating - Ephemerides • Self Check

If the control CPU fails, the secondary CPU will enter SAFE-CONTROL, establish the safe-state, and then operate as if it were in the nominal Control state. In general, this results in the equipment being switched to a known (previously determined) state. The bus use reverts back to the original state. The new control CPU software will execute the redundancy management software.

MODE tests for a request to switch the bus before it tests for request to switch redundant devices. A request to switch the bus takes precedence over all device switch requests. If there is no requested bus switch, MODE tests for device-switch requests.

Bus Switching - If the bus switch request flag is set, MODE tests both bus-switching veto flags:

a. FVETO - set by MODE after the bus has been switched already. Must be reset by ground command.

b. FVETOI - set by ground command. Must be reset by ground command.

If either flag is set, MODE sets the MEOK Inhibit flag (which, later-on in MODE, may inhibit the sending of a MEOK thus taking the CPU offline after three such occurrences).

If both flags are reset, MODE sets FVETO and then switches buses, by means of the commands BIXFR and PIOLO. Immediately after sending the PIOLO command, MODE complements the FBUS flag.

Device Switching - MODE processes requests to switch redundant devices independently. If the device-switch request flag is set, MODE tests the device-switch inhibit flag (which gets set after the device has been switched already).

If the flag is reset, MODE sets the flag, and then switches devices. There are two commands for each device: one which selects the backup device, and one which selects the primary device. The command selected is determined by the value of the device-state flag. After the command is sent, the device state is set to indicate whether the backup or primary device is in use.

If the device-switch-inhibit flag is set, then bus-switching is attempted. For ESA only, if bus switching cannot be performed (because of the veto flags), then the state of the other CPU is tested before MEOK is inhibited. The other CPU has to be OK because MEOK inhibit is set-which will force a "CPU-switch".

ESA Read Check - MODE clears the ESA switch flag at each entry prior to failure testing. Module ESRS decrements variable QCNTR as each set of three ESA data words is read. MODE checks QCNTR to see if it equals zero. If it does not for three consecutive cycles, MODE sets the ESA Switch Request flag for use by the Switching-Strategy Function. Following each QCNTR test, MODE resets the quadrant counter to 4 in anticipation of next ESRS cycle.

ESA Quad Fault - Module ADS will set flag FESAOUT indicating ESA data should not be used. ADS also sets bits in the variable QUW corresponding to given ESA quads, indicating that data from that quad should not be used. Module GEODAT sets bits in the variable SMWARN corresponding to given quads, indicating that data from that quad should not be used due to interference from the sun or moon.

If FESAOUT is set, MODE compares QUW with SMWARN. If bits from two opposite quadrants (1-2 or 3-4), or from more than two quads, are set in QUW but are not set in SMWARN, and this condition exists for three consecutive cycles, then MODE sets the ESA Switch Request Flag.

IMU Electronics - MODE switches IMU electronics if the conditions specified in the next few paragraphs exist. After switching IMU electronics, MODE issues four gyro turn-on commands through CMDPRO. Before switching buses, in an attempt to correct an IMU failure, three gyro turn-on commands are issued. The three gyro commands are organized in contiguous memory locations to allow easy gyro reconfiguration by ground command.

IMU Interrupts - Module TIREX sets and then decrements the variable SUBCYC at each 0.1 second interrupt from the IMU. MODE checks SUBCYC to see if it equals zero. If it does not equal zero for five consecutive cycles, MODE sets the IMU Switch Request Flag for use by the Switching-Strategy function.

IMU Rate Nulling - Module ADS sets the variable SMODE which indicates the attitude control submode. If SMODE indicates rate nulling is in effect, MODE initializes a cycle counter to 1800, and MODE will:

a. Check flag FRTERR which, when cleared by ADS, indicates that all three error rates are nulled. If FRTERR is clear, re-initialize the cycle counter. If FRTERR is set, decrement the cycle counter.

b. If the cycle counter becomes equal to zero, then set the IMU Switch Request Flag.

IMU Data Late - Module DFS sets flag DFSIER if the data is not received within a given time limit. If DFSIER is set for three consecutive cycles, MODE sets the IMU Switch Request Flag.

IMU Data Unreasonable - Module ADS tests the gyro data for reasonableness and after four cycles of bad data, sets a bit in the variable GRFAIL corresponding to the tested gyro. IMU status word SIMU indicates if any gyro has a spin motor failure. These two variables are checked by MODE. If GRFAIL indicates two or more gyros have bad data, or indicates only one has bad data and SIMU indicates a different gyro has a spin motor failure, and this failure(s) exists for a consecutive period of 60 seconds, then MODE sets the IMU Switch Request Flag. MODE also clears GRFAIL and GRCNT at this time.

SAD POWER

Solar Array Position Error - Module SADCS sets the error flag FERRNC to indicate an error in solar array pointing which could not be removed by slewing the array. If MODE finds the flag set, it sets the SAD Switch Request flag for the Switching for the Switching-Strategy function. MODE clears the FERRNC error flag.

RWA - Module ACS controls the testing and selection of the wheels. If the skew wheel is being used and any wheel fails the passive wheel test for two consecutive tests, ACS will set the flag FRWAF. If MODE finds FRWAF set, it will set the Bus Switch Request flag for the Switching Strategy function. MODE clears the FRWAF error flag.

IMU Electronics - MODE switches IMU electronics if the conditions specified in the next few paragraphs exist. After switching IMU electronics, MODE issues four gyro turn-on commands through CMDPRO. Before switching buses, in an attempt to correct an IMU failure, three gyro turn-on commands are issued. The three gyro commands are organized in contiguous memory locations to allow easy gyro reconfiguration by ground command.

IMU Interrupts - Module TIREX sets and then decrements the variable SUBCYC at each 0.1 second interrupt from the IMU. MODE checks SUBCYC to see if it equals zero. If it does not equal zero for five consecutive cycles, MODE sets the IMU Switch Request Flag for use by the Switching-Strategy function.

IMU Rate Nulling - Module ADS sets the variable SMODE which indicates the attitude control submode. If SMODE indicates rate nulling is in effect, MODE initializes a cycle counter to 1800, and MODE will:

a. Check flag FRTERR which, when cleared by ADS, indicates that all three error rates are nulled. If FRTERR is clear, re-initialize the cycle counter. If FRTERR is set, decrement the cycle counter.

b. If the cycle counter becomes equal to zero, then set the IMU Switch Request Flag.

IMU Data Late - Module DFS sets flag DFSIER if the data is not received within a given time limit. If DFSIER is set for three consecutive cycles, MODE sets the IMU Switch Request Flag.

IMU Data Unreasonable - Module ADS tests the gyro data for reasonableness and after four cycles of bad data, sets a bit in the variable GRFAIL corresponding to the tested gyro. IMU status word SIMU indicates if any gyro has a spin motor failure. These two variables are checked by MODE. If GRFAIL indicates two or more gyros have bad data, or indicates only one has bad data and SIMU indicates a different gyro has a spin motor failure, and this failure(s) exists for a consecutive period of 60 seconds, then MODE sets the IMU Switch Request Flag. MODE also clears GRFAIL and GRCNT at this time.

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SSA - Module GEODAT sets flag FSSA when it begins reading sun sensor data and clears it after a successful series of sun sensor reads. If FSSA is found set by MODE for 21 consecutive cycles, it sets the Bus Switch Request flag if bus switching is possible (FVETO and FVETOI are clear). If bus switching is not possible, MODE sets the flag FYGC to indicate to ADS to go to the YGC operating mode, rather than cause the CPU to go offline.

MODE is called once each 0.5 seconds. If not called, the MEOK signal will not be issued. MODE tests the lower level IQRs to determine which of the lower levels have not completed processing. A level is "hung-up" if it exceeds its maximum allowable run time shown in Table 4.10.2-1. After that time, the MODE software restarts the software on the uncompleted level and MODE issues no MEOK signal on that pass.

This check is correlated with CARP (CPU Alarm Software) and the CPU self test programs ITEST and MEMCHK.

Description of other Executive Modules

Specific descriptions of the other executive modules TIREX, CTEL, CARP, ITEST, MEMCHK and LIBRY as well as MODE are given in Section 4.10.9.

4.10.5 COMMAND AND CONTROL SOFTWARE

System Description - The command and control software is part of the C&C Subsystem and is defined here to include the functions of decoding, testing and executing both real-time and stored commands. The C&C Subsystem also includes the function of control of system configuration through selection of the CPU and bus. This includes telemetry to verify the configuration.

The Command and Control Software, shown in Figure 4.10.5-1, is described in the following paragraphs.

Real-Time Processor - The Real-Time Processor (RTP) software performs initial processing on commands, provides command verification and error messages to the command verification queue, and performs the memory load function.

RTP processing begins when a level 12 (uplink processor) interrupt is generated. RTP reads the GSTDN Receiver/Demodulator (GRD) status word shown in Figure 4.10.5-2, and the 16 bit active field portion of the uplinked word shown in Figure 4.10.5-3. If the status word indicates neither a CPU decoded command nor a CPU data word (i.e., indicates an uplink processor error or a valid CIU hardware command), a message is formed for command verification.

If the status word indicates valid CPU commands or data, RTP attempts to form the command sequence:

COMMAND · DATA · EXECUTE

where "Data" is optionally zero to three data words, being required of only certain commands. All command sequences are checked to verify that no more than three data words are present. If RTP cannot form the sequence, error messages for CV identify the reason. If a correct sequence was formed, RTP calls CMDPRO and passes the number of data words and the starting address of the command sequence.

LEVEL	SOFTWARE FUNCTION
16	ERROR HANDLER
15	PRIVILEGE MOVE
14	(SDF INTERFACE)
13	COMMAND PROCESSOR
12	REAL TIME PROCESSOR
11	CPU TELEMETRY
10	CPU DUMP
9	EXECUTIVE, IMU READ, MODE CONTROL, THRUSTER CONTROL
8	EARTH SENSOR READ
7	TIP SUBCOM READ
6	EXECUTIVE – ATTITUDE DET. AND CONTROL
5	SPARE
4	EXECUTIVE – STORED CMDS, TIMED EVENTS
3	EXECUTIVE – COILS, ARRAY DRIVE, GN_2 UNLOADING
2	EXECUTIVE – POWER MANAGEMENT
1	EXECUTIVE – MEMORY CHECK, INSTRUCTION TEST

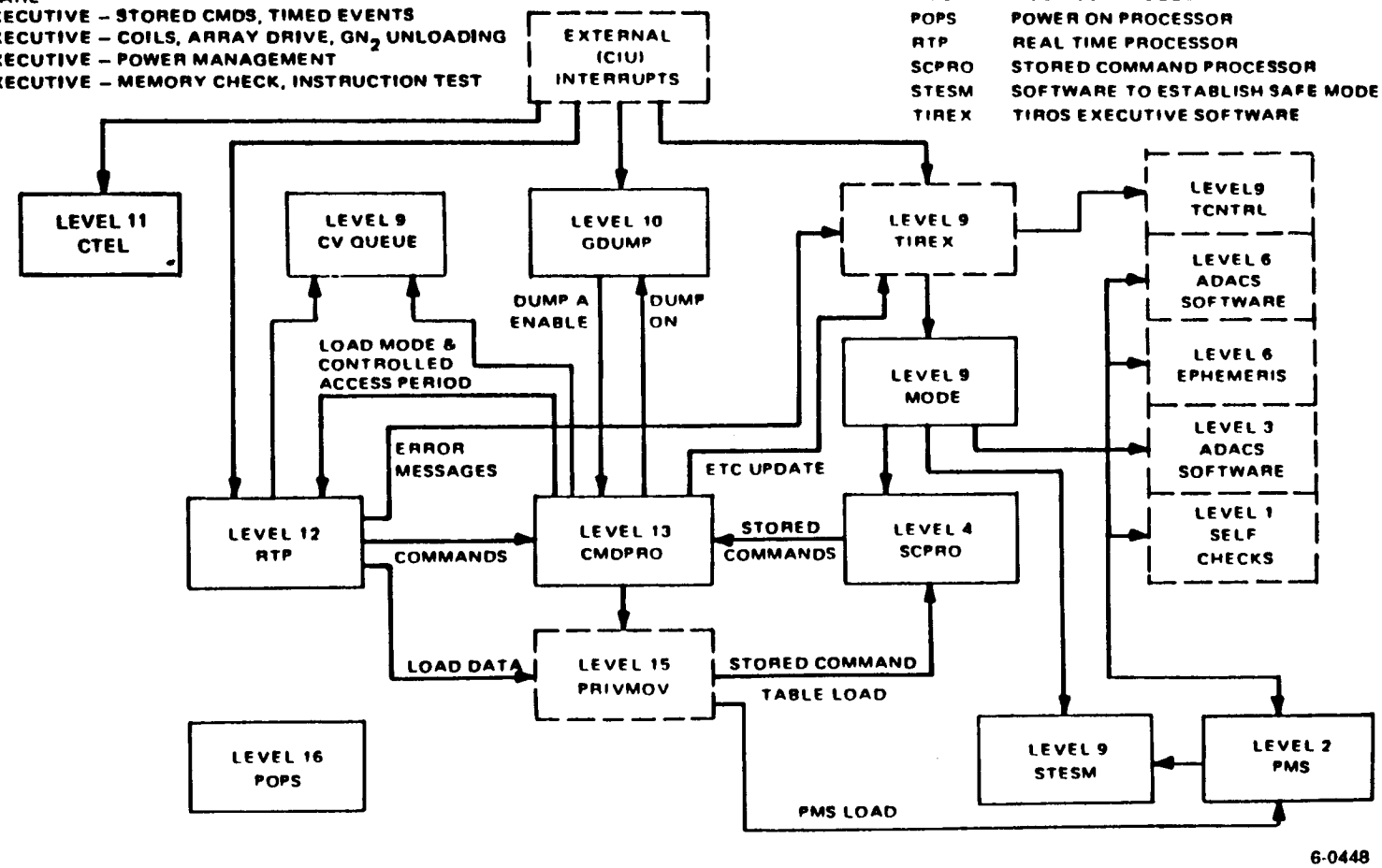


Figure 4.10.5-1. Command & Control Software, Functional Block Diagram

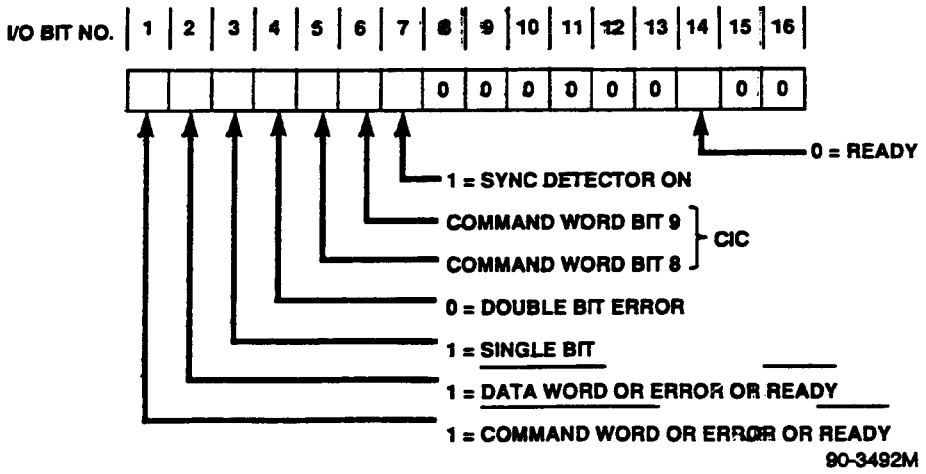


Figure 4.10.5-2. Uplink Processor Status Word

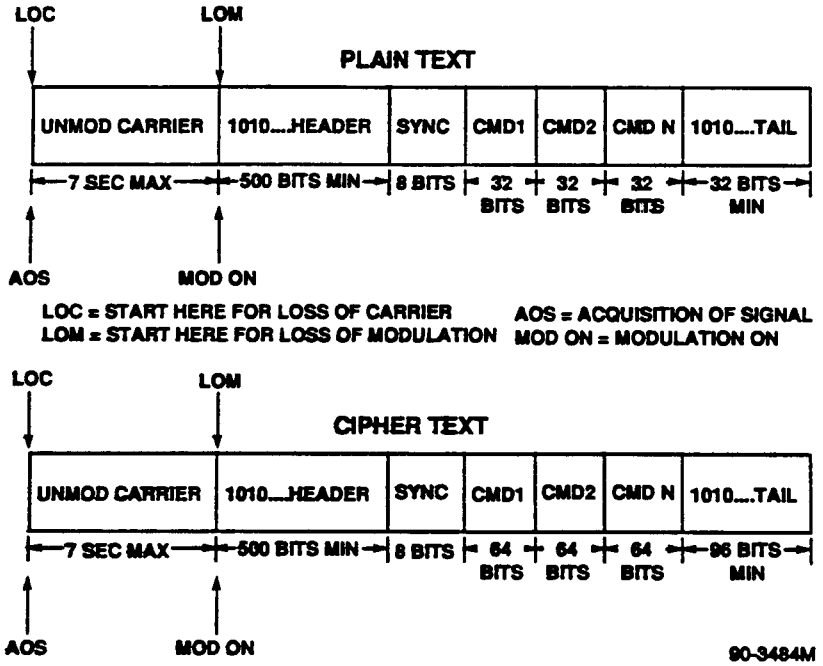


Figure 4.10.5-3. Uplink Word Format

If CMDPRO receives a load command, control flags are set to cause RTP to collect subsequent data words and pass these in blocks of 16 words (whenever 16 or more words remain to be loaded) to PRIMOV for loading into the memory.

Command Processor - The Command Processor (CMDPRO) does the actual decoding of real-time and stored commands not decoded and executed by the CIU hardware. CMDPRO executes the commands or provides error messages for the CV queue when execution is not possible. CMDPRO operates on interrupt level 13 so that once entered, it runs to completion without being interrupted (unless a CPU error occurs).

Figure 4.10.5-4 shows the format of the 16 bit active field of an uplink word when it represents a command. CMDPRO accepts commands from RTP (real-time), SCPRO (stored), and other software modules (internal). The five types of commands are:

- Pulse discrete (Hardware)

  - Separate Bit for each function
  - Set Bit "True" (or "False" for inverted logic) for fixed interval

- Level discretes (Hardware)

  - Single bit has Binary Function (On/Off, True/False)
  - Separate command for function "True" & Function "False"

- Software Discrete

  - Separate "Set" & "Clear" Commands for flags

- Software Procedure (or Load Word)

  - Allows user to replace memory contents with data word included with command

- Distinct Procedures

  - Separate subroutine (Software Procedure) for each

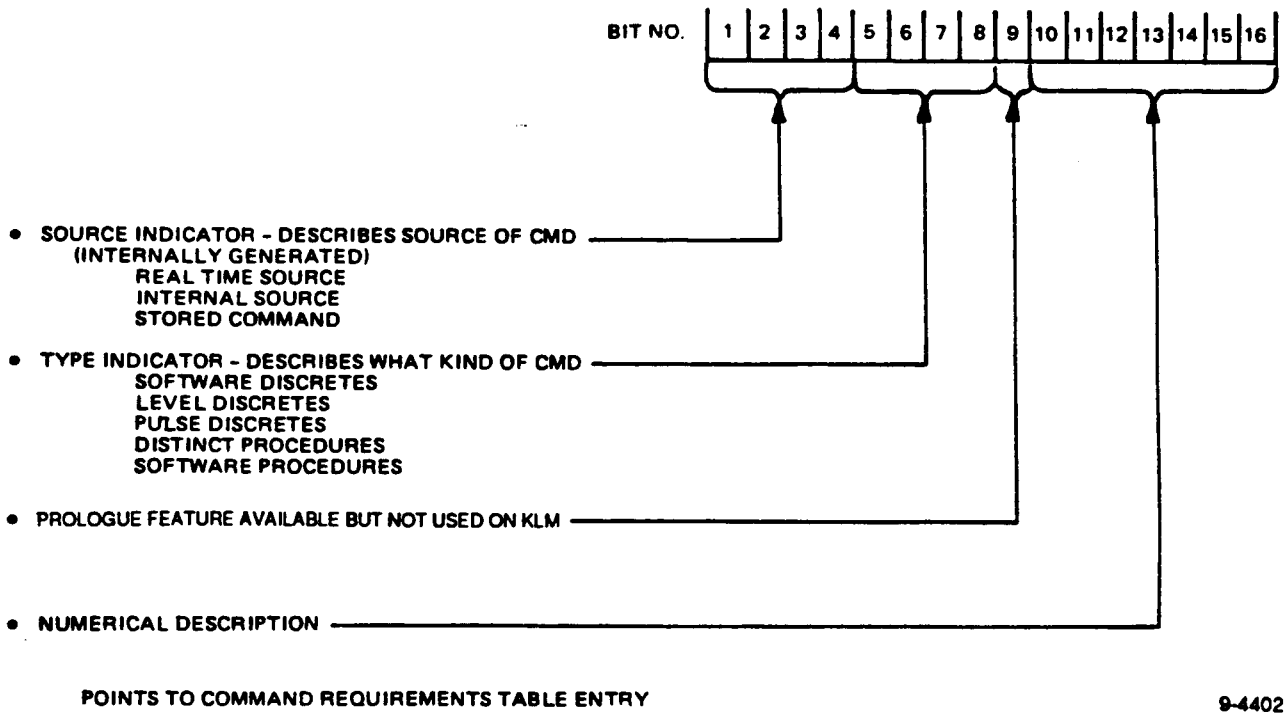


Figure 4.10.5-4. Command Format

CMDRO makes the following basic checks on all commands:

a) Source test - Commands being checked may have been internally generated, come from the stored command table, or been real-time from the ground. If the source field of Figure 4.10.5-4 indicates any other type, this is considered an error.

   Additionally, command processing allows for the ability to specify that some be real-time only, and that an error is present should one of these particular commands be received from anything other than RTP.

b) Type test - Only those command types shown in Figure 4.10.5-4 are considered valid. Receipt of type code indicating any other type is considered an error.

Prologue available but not used in KLM

c) Prologue test - As a measure of safety against accidental execution of some commands, the CMDPRO requires that these commands are preceded by a prologue such that the sequence is in the form:

   Prologue · Execute · Command · Data · Execute

   CMDPRO requires that the second "Execute" be received within 30 seconds of the first "Execute" for the command to be valid if it came as a real time command. Stored commands do not have a time restriction. If a command has been defined as requiring a prologue, the test for its presence within the required time is performed.

d) Command number test - The command number field of Figure 4.10.5-4 allows 128 commands of each type. In the event not all 128 are used, if an unused command is specified, this is considered an error.

e) Data word test - For those commands that require data words, a check is made that the proper number for the particular command are present.

f) Address test - In the event the command involves reading or writing operations, the addresses specified by the command's data words are checked to insure that the operation is possible and allowable.

A module called TIMED TASKS (TIKS) is called by MODE via the level 4 executive but is logically considered an extension of CMDPRO. TIKS consists of a prologue timer, DAU timer, memory load checksum processing and the terminating half of pulse commands. The timers decrement every half second, and appropriate action is taken if either timer decrements to zero. A checksum is performed on memory loads if requested by the ground via flags set by RTP and CMDPRO.

When a CIU pulse command is initiated, CMDPRO forms a pulse terminate command and stores it in a table maintained by TIKS. Every other half second TIKS retrieves any terminate commands and returns them to CMDPRO for execution. A minimum "ON" time of 0.5 second is thus insured.

Two other modules logically associated with CMDPRO are CVQO and CVQI (the Command Verification Queue). These modules receive command verification words

In operation, the time label of stored commands is compared sequentially to a command-time counter maintained in software. If a match does not result, no action is taken. When the command time equals the time label, the command and any associated data words are retrieved from the stored command table (and passed to CMDPRO for execution) and the time tag of the next command down in the table is checked for coincidence with command time.

If the command time exceeds the stored-command time tag, the command is skipped.

If CMDPRO receives a command to change the command time (against which SCPRO compares time tags), SCPRO temporarily stops normal processing until the update has occurred.

SCPRO provides for optional, ground commandable START and STOP control over stored command processing. It is not necessary to stop stored command processing during loading of a portion of the stored command table, although stopping processing may be the practice preferred at times by the CDA station. The START command requires that the ground supply a starting address, specifying where in the table to begin processing. A software discrete command allows processing to begin with the command being checked when "STOP" was issued, as opposed to starting at a new uplinked address.

General Dump - The General Dump (GDUMP) module performs the function of dumping specified portions of the CPU memory upon command.

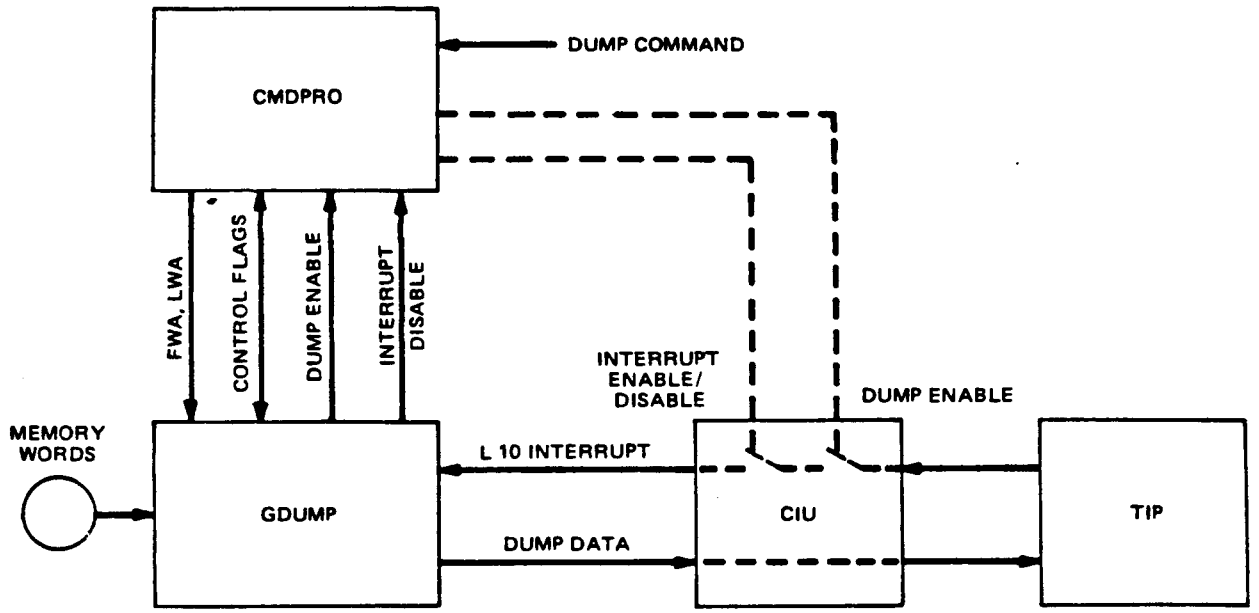
Upon receipt of a real-time or stored DUMP command, the CMDPRO module in the CPU which received the command sets up in preparation for a dump. The "ENABLE CPU DUMP" interrupt signal from the TIP is steered by the CIU to the GDUMP module in the CPU which received the DUMP command.

At each interrupt, three words from memory are output be GDUMP. If the initializing command was for a general (diagnostic) dump, the desired start and stop addresses for the dump are taken (by CMDPRO) from uplinked data words. If a verification dump was requested, CMDPRO uses the start and stop addresses of the last data load to pass to GDUMP for dumping limits.

GDUMP processing during the interrupt at which the contents of the stop address are output, causes the CIU to steer the dump interrupts to the CPU which is not in control. This is done by sending a dump enable command (via CMDPRO) as shown in Figure 4.10.5-6. The CONTROL CPU will grab back the interrupts if it receives another dump command. GDUMP completes processing of the dump and returns to calling routine.

All dumps begin by GDUMP outputting the start and stop addresses followed by the contents of the start address, and continuing until the contents of the stop address have been output.

A DUMP STOP command causes GDUMP to terminate dumping after the current three word transfer. The level 10 interrupt is disabled and the interrupts are steered to the non-control CPU.



6-0453

Figure 4.10.5-6. GDUMP Interfaces

GDUMP (during dumps) responds to spurious interrupts in a manner which leaves the TIP output unaffected. For temporary TIP CIU buffer failures, GDUMP stops at the last word output so that when the buffer becomes ready and OK again, dumping begins where it left off and no words are lost.

GDUMP interfaces with CMDPRO and the CIU are shown in Figure 4.10.5-6.

4.10.6 ATTITUDE DETERMINATION AND CONTROL SUBSYSTEM SOFTWARE

4.10.6.1 System Description

The Earth Sensor Read Software operates under hardware interrupt control and transfers data from the ESA to the CPU via the CIU. The ESRS module inputs, tests for transmission errors and out of range conditions, and scales ESA data for use in the ADS module.

The Digital Filter Software reads data from the IMU every 0.1 second, filters the data, and generates the filtered output every 0.5 sec for use by the ADS module.

The Attitude Determination Software (ADS) performs the attitude error and error rate calculations for use in the Attitude Control Software (ACS) module. In addition, the ADS module examines the ESA, gyro, and SSA data for conditions that determine the attitude control mode and performs a monitoring function for attitude error criteria.

The Geometric Data routine generates ephemeris data. GEODAT computes the solar array drive angle for the array drive control software, computes yaw updates once per orbit, provides magnetic field data for momentum unloading, provides sun/moon warnings, calculates the spacecraft altitude above the reference geoid for ESA data processing and sets an eclipse flag for power management. GEODAT is updated weekly with a table of parameters via ground command.

The Attitude Control Software computes, formats, and transmits the attitude control signals to the RWAs. The determination of the control torques is based upon the spacecraft attitude error angles and error rates, the operating control mode, and which of the RWAs are operational. The ACS is responsible for determining the equivalent three orthogonal wheel speeds of the operating RWAs for momentum unloading, for the issuance of MMU on/off and polarity commands to the coils via the CIU and SCU, and for conducting the Passive Wheel Test on the RWAs.

The Magnetic Momentum Unloading Software controls the operation of the PTC and RYC coils for spacecraft momentum management. Using RWA wheel speed data, the MMUS determines local magnetic latitude, an orbit reference (ascending or descending side) of which coil(s) need to be energized or de-energized, and formulates the command sets for ACS to issue.

Solar Array Drive Control Software contains the logic necessary to command the Solar Array Drive Electronics (ADE). SADCS utilizes inputs from GEODAT and the ADE to provide the necessary speed commands to drive the array.

4.10.6.2 Earth Sensor Read Software

The Earth Sensor Read Software (ESRS) module operates on interrupt level 8. An interrupt is generated by completion of a one-word data transfer from the ESA to the CIU. There are four interrupts for each 0.5 second computational cycle. The MODE module initiates the data transfer at 2Hz time when ESA data is required. ESRS reads three data words each interrupt, tests the data for transmission errors and out of range conditions, and scales the data for use by the ADS module.

ESRS controls the sequence of reading, testing, and scaling the data for use by the ADS module. ESRS reads and stores CIU buffer address 425 (hex) in the quadrant order 1, 2, 3, 4. ESRS and ADS use the buffer indicator ESRABF to determine which of two data buffers ESRBUFA and ESRBUFB is to be filled by ESRS and read by ADS during each cycle. ESRABF is set by the MODE module. Therefore, data area use is as follows:

Cycle	Fill by ESRS	Use in ADS
n-1	A	B
n	B	A
n+1	A	B

A counter, QCNTR, is maintained by MODE and ESRS to indicate the number of entries to ESRS on each computational cycle (0.5 second). This counter is set to 4 by MODE at 2Hz time. ESRS decrements the flag to ensure that ESRS is

collecting data for all four quadrants of the ESA and to aid in control of the data transfer. There are three words for each of the four ESA quadrants transferred in the sensor order V_S, V_B, V_A.

The MODE module issues an 'OPR Begin' at 2Hz time to transfer the first group of sensor readings. ESRS issues the next three 'OPR Begin's' before exiting (Figure 4.10.6-1) to ensure that the data transfer is initiated from the ESA to the CIU buffer. When the buffer is filled, the ESA will generate an interrupt for the next ESRS processing. ESRS clears the interrupt each time upon completion. The expected operation generates four interrupts each 0.5 second. The first will occur 20-40 ms after the MODE module finishes and the others are spaced at 120 msec intervals (Figure 4.10.6-2).

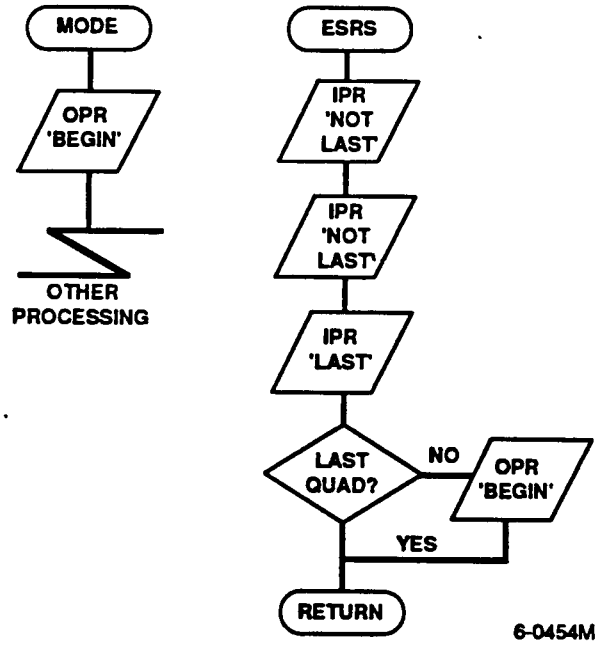


Figure 4.10.6-1. Generalized Flow for Data Transfers Between Buffer 425 and ESRS.

A quadrant failed flag ESRQFFA or ESRQFFB is maintained to indicate the status of the quadrant data in the buffer. Upon exiting, ESRS sets all bits in ESRQFFA or ESRQFFB which are also set in the sun-moon warning word, SMWARN. This action supersedes the clearing of the bit in the absence of failure.

ESRS exits by clearing the level 8 interrupt.

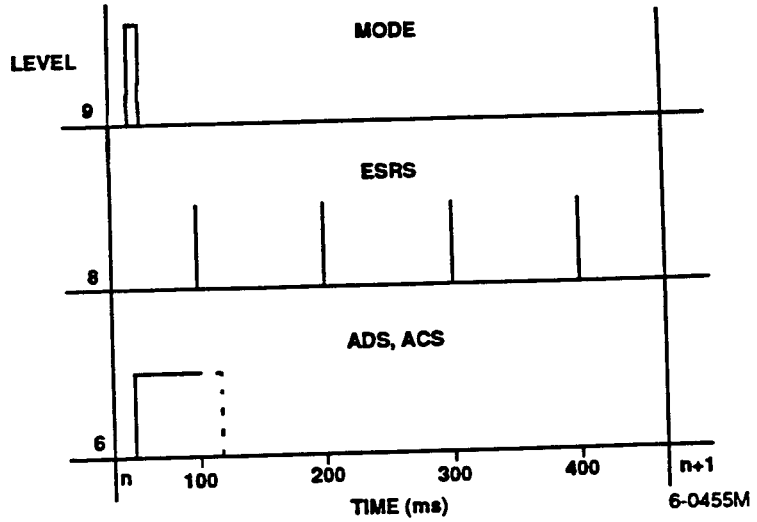


Figure 4.10.6-2. Relative Timing of MODE, ESRS, ADS and ACS

ESRS performs a status test on the CIU buffer between the first and second, and the second and third data transfers within a quadrant group. A nominal delay of 160 μsec is expected for the buffer to become ready. A delay of 250 μsec or more is considered excessive and ESRS does the following:

1. Sets ESRED equal to QCNTR.

2. Issues an 'IPR LAST' to shut down the interface.

3. Does not clear the quadrant bit in the QUAD failed word (ESRQFFA or ESRQFFB) for the present data.

ESRS tests the overrange bit 4 and the not used bits 2 and 3 to see if they are set to 1. These conditions constitute a transmission error and therefore ESRS does not clear the quad failed bit for that quadrant in the quad failed flag (ESRQFFA or ESRQFFB).

When bits 2, 3, and 4 are not set to 1, then ESRS clears the quad failed bit for that quadrant.

The ADS module sets the four quad bits in each flag (ESRQFFA or ESRQFFB) after using the corresponding data area. Therefore, the burden of clearing the quad bits is with ESRS.

ESRS converts the ESA data from sign magnitude form to two's complement form for internal use in the CPU. Data words found to be in error are not converted. After each word is tested and converted to two's complement it is

collecting data for all four quadrants of the ESA and to aid in control of the data transfer. There are three words for each of the four ESA quadrants transferred in the sensor order V_S, V_B, V_A.

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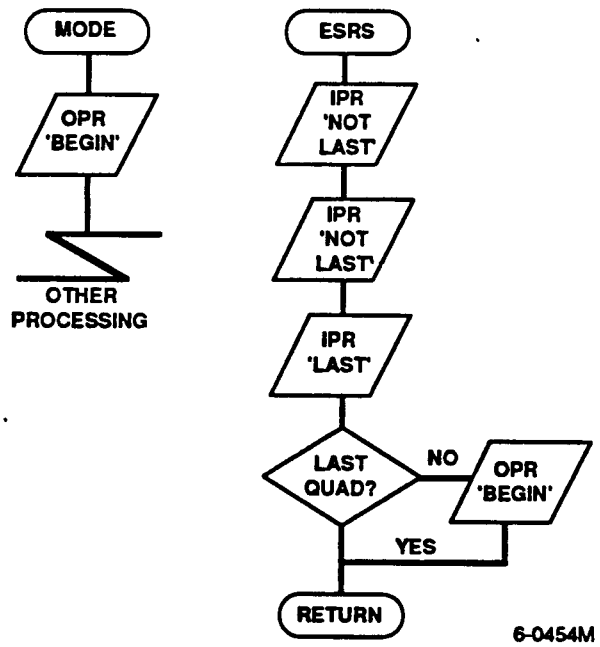

Figure 4.10.6-1. Generalized Flow for Data Transfers Between Buffer 425 and ESRS.

A quadrant failed flag ESRQFFA or ESRQFFB is maintained to indicate the status of the quadrant data in the buffer. Upon exiting, ESRS sets all bits in ESRQFFA or ESRQFFB which are also set in the sun-moon warning word, SMWARN. This action supersedes the clearing of the bit in the absence of failure.

ESRS exits by clearing the level 8 interrupt.

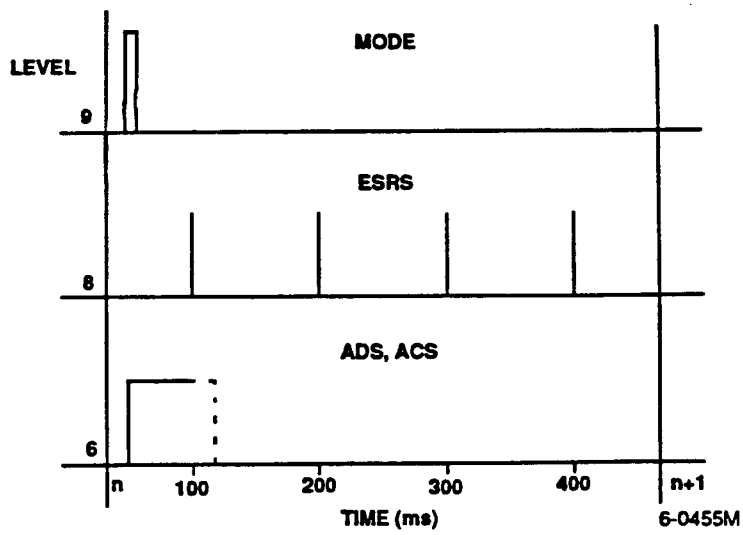

Figure 4.10.6-2. Relative Timing of MODE, ESRS, ADS and ACS

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ESRS converts the ESA data from sign magnitude form to two's complement form for internal use in the CPU. Data words found to be in error are not converted. After each word is tested and converted to two's complement it is

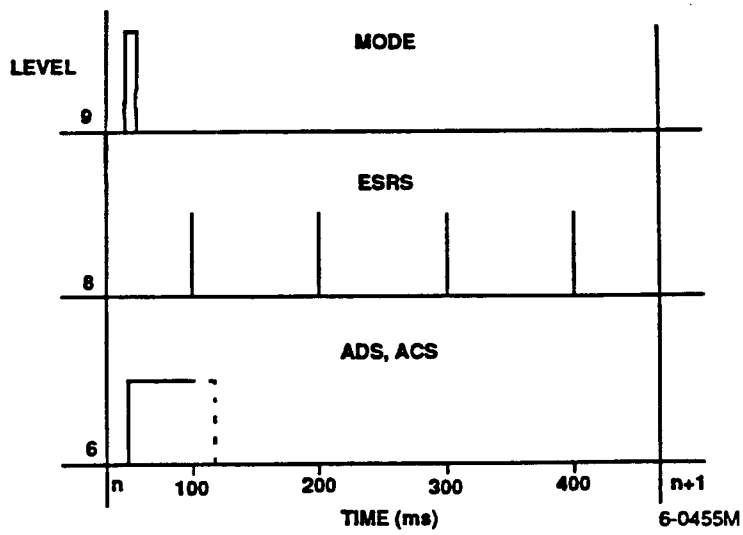

Figure 4.10.6-2. Relative Timing of MODE, ESRS, ADS and ACS

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The ADS module sets the four quad bits in each flag (ESRQFFA or ESRQFFB) after using the corresponding data area. Therefore, the burden of clearing the quad bits is with ESRS.

ESRS converts the ESA data from sign magnitude form to two's complement form for internal use in the CPU. Data words found to be in error are not converted. After each word is tested and converted to two's complement it is

adjusted by the measured bias correction term (one element in the MBARY array) and then scaled by the appropriate multiplicative constant K_{ij} as follows:

$$V_{ij} = K_{ij} * [U_{ij} - MBARY(1)]$$

i = A, B, or S sensor

j = 1, 2, 3, 4 quadrant

l = 0. ESA primary, 'S' positive
1. ESA primary, 'S' negative
2. ESA backup, 'S' positive
3. ESA backup, 'S' negative

V_{ij} is then placed in the buffer area for ADS. U_{ij} is the converted data read from the CIU buffer. The measured Bias has a nominal value of 200 when 'S' is positive and 100 when 'S' is negative; 'S' is the space detector output. The scale factors K_{ij} have a nominal value of 1.0 and are supplied with each separate ESA at delivery.

ESRS Input/Output Parameter

The ESRS input/output requirements are shown in Figure 4.10.6-3 and defined as follows:

Symbol	Source	Description
QCNTR	MODE/ESRS	Quadrant - Interrupt Counter
ESRABF	MODE	Buffer Use Flag
ESRBUFA/B	ESRS	Redundant Buffers for ESRS and ADS Use
ESRQFFA/B	ESRS/ADS	Redundant Quad Fail Flags
ESRED	ESRS	Excessive Time for Read Flag
SMWARN	GEODAT	Sun/Moon Warning Flag
ESASTATE	MODE	ESA Electronic State

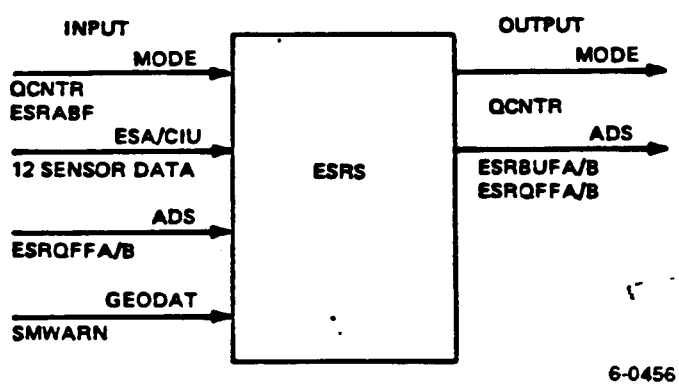

Figure 4.10.6-3. ESRS Input/Output Requirements

ESRS Telemetry Parameters

The ESRS Telemetry parameter requirements are as follows:

Symbol	Parameter
V_A	RAW ESA A Detector Readings (4 words)
V_B	RAW ESA B Detector Readings (4 words)
V_S	RAW ESA S Detector Readings (4 words)
FTRAD	Triad Data word error flag
FSRED	Excessive Time for read flag
ESRQFFA/B	Redundant quadrant failure flags

4.10.6.3 Digital Filter Software (DFS)

The Digital Filter Software Module (DFS) is called as a subroutine by the TIREX module. DFS reads the gyro data from the IMU via the CIU buffer every 0.1 second subcycle. The values are collected and filtered and the IMU status word is recorded. When read errors occur, the last value read is used for the filtering process. Every 0.5 second, DFS outputs the sum of the filtered values and the last filtered value for each gyro. DFS also outputs the IMU status word for use by the ADS module.

DFS provides the control for reading and filtering the gyro data from the IMU, checking for read errors and outputting the filtered data at 2Hz time.

DFS reads a data sequence of eight words from the IMU through the CIU buffer 483 (hex). Upon entry, DFS issues an 'OPR Begin' to initiate the data transfer from the IMU to the CIU buffer.

Each word is read with an 'IPR NOT LAST' until the eighth word which is read with an 'IPR LAST'. All eight words must be read to allow the other CPU to read the same data sequence, but the control CPU will get eight new words at the next interrupt whether or not the standby CPU reads any or all of the words.

The first word of the data sequence is the gyro status word. The last IMU status word read at 2-Hz time is saved for use by other ADACS modules.

The second through seventh words of the data sequence are the gyro data in the order X_A Y_A Z_A X_B Y_B Z_B.

The last word of the data sequence is not applicable to DFS and is discarded after reading.

DFS calls a subroutine named BUSY and checks for previous error conditions and times the wait period for the buffer status to become READY.

Subroutine BUSY has two wait times to allow up to a 50 msec delay for the IMU/CIU buffer to initially become ready. After the initial READ, a maximum delay time of 250 msec is allowed.

BUSY sets the error flag DFSIERR when the wait time is exceeded, preventing use of the word to be read.

DFS filters the data each 0.1 second subcycle for each gyro as follows:

Given the filtered values from the previous cycles, and the current and past four gyro values, the current second derivative is computed as follows:

$$\Delta^2 F_o = a_1 F_1 + b_1 \Delta F_1 + h_1 \Delta^2 F_1 + h_2 \Delta^2 F_2 + \sum_0^4 e_i G_i$$

where, for i = X_A Y_A Z_A X_B Y_B Z_B channels

G_i = Current and past four cycles of gyro data
F_{i1} = last cycle, filtered gyro data
ΔF_{i1} = last cycle, first order filtered gyro data
$\Delta^2 F_{i1}$ = last cycle, second order filtered gyro data
$\Delta^2 F_{i2}$ = 2 cycles past, second order filtered gyro data
ei = coefficients for the current and past gyro values
a_1, b_1, h_1, h2 = Coefficients for the past filtered values

The new filter values for each gyro are formed as follows:

$$\Delta^2 F_{i2} = \Delta^2 F_{i1}$$
$$\Delta^2 F_{i1} = \Delta^2 F_{i0}$$
$$\Delta F_{i1} = \Delta F_1 + \Delta^2 F_1$$
$$F_{1i} = F_{i1} + \Delta F_{i1}$$
$$SUM = SUM + F_1$$

SUM is the sum of the filtered values. SUM is cleared after being stored in VGPC every 2-Hz subcycle.

Whenever a read error occurs (DFSIERR set), DFS uses the last data value read for that gyro in the filter processing.

DFS outputs the sum of the filtered values for each gyro, the last filtered value for each gyro, and the IMU status word at 2-Hz time. TIREX maintains the subcycle indicator, SUBCYC, which is = 0 at 2-Hz time and ≠ 0 otherwise.

DFS Input/Output Parameters

The DFS input/output requirements are shown in Figure 4.10.6-4 and defined as follows:

Symbol	Source	Description
G_i	CIU/IMU	gyro data for i = X_A, Y_A, Z_A, X_B, Y_B, Z_B gyros
STAT	CIU/IMU	IMU status word
SUBCYC	TIREX	cycle indicator (= 0 2-Hz time, ≠ 0 otherwise)
$VGPC_i$	DFS	sum of filtered values for i = X_A, Y_A, Z_A, X_B, Y_B, Z_B gyros
SIMU	DFS	latest IMU status word read
SUM	DFS	last filtered value for i = X_A, Y_A, Z_A, X_B, Y_B, Z_B gyros
DFSIERR	DFS	excessive read error indicator flag

DFS Telemetry Parameters

The DFS telemetry parameter requirements are as follows:

Symbol	Parameter
VGPC	Filtered gyro pulse count over 0.5 sec period for X_A, Y_A, Z_A, X_B, Y_B, Z_B gyros
SIMU	IMU Status at 2 Hz-time

4.10.6.4 Attitude Determination Software (ADS)

The Attitude Determination Software module is called as a subroutine once each 0.5 second computational cycle. ADS receives attitude data from the ESRS, DFS and GEODAT modules every half second. ADS tests and processes the data to determine error-angles, body error-rates and attitude control submode for ACS. ADS also provides the MODE module with indicators of the ADS software status and ESA system.

The ADS module is defined functionally in Figure 4.10.6-5.

ESA Status (ESAST)

ESAST tests and processes the data from the ESA which was collected and scaled by the module ESRS. The data collected on cycle n-1 by ESRS is used by ESAST on cycle n. ESRS has placed the data alternately into one of two data buffers (ESRBUFA or ESRBUFB). The buffer use flag ESRABF is used to choose the proper buffer.

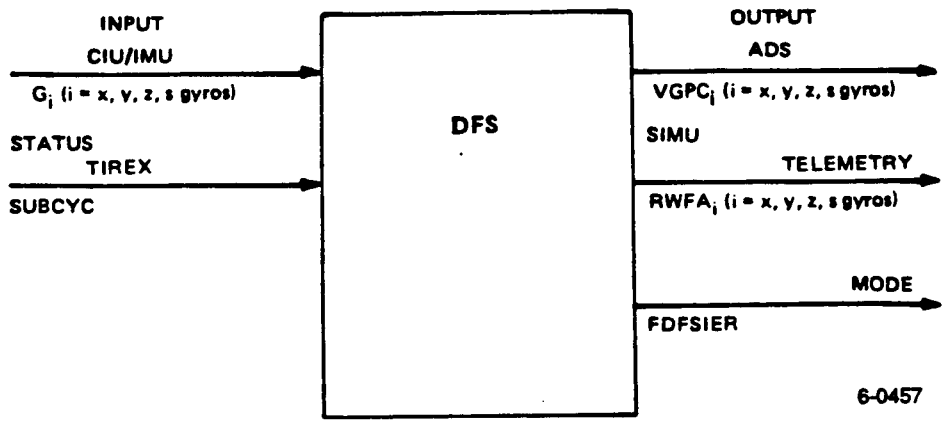

Figure 4.10.6-4. DFS Input/Output Requirements

ESRS maintains two quantities, ESRQFFA and ESRQFFB, which are identical in function to the Quad Use Word (QUW) maintained in ADS. Upon entry to ESAST, QUW is set equal to ESRQFFA or ESRQFFB, corresponding to the buffer used. ESAST then sets the four quad bits of the current quad failed flag ESRQFFA or ESRQFFB. This ensures that they are set if ESRS does not get called before the next ADS cycle.

An additional word GQUW provides ground control of the use of quadrants. Each bit set in GQUW is also set in QUW.

When the QUW shows that a quadrant has failed, the following test of the ESA data and computation of penetration parameters from the data is ignored.

The order of the ESA data in the buffers ESRBUFA and ESRBUFB is V_S, V_B, V_A for quadrants 1, 2, 3, 4.

Three tests are performed to determine usableness of the data for each quadrant. If the data passes each test, then a penetration parameter X_n is computed for each quadrant as follows:

$$X_n = \frac{2[K_{An}V_{An} - K_{Sn}V_{Sn}]}{[K_{An}V_{An} + K_{Bn}V_{Bn} - 2K_{Sn}V_{Sn}]}$$

where $K_{S,B,A}$ = ESA quadrant scale factors (ESA dependent) nominally 1
$V_{S,B,A}$ = ESA data from a given quadrant
n = ESA quadrant number, 1, 2, 3, 4

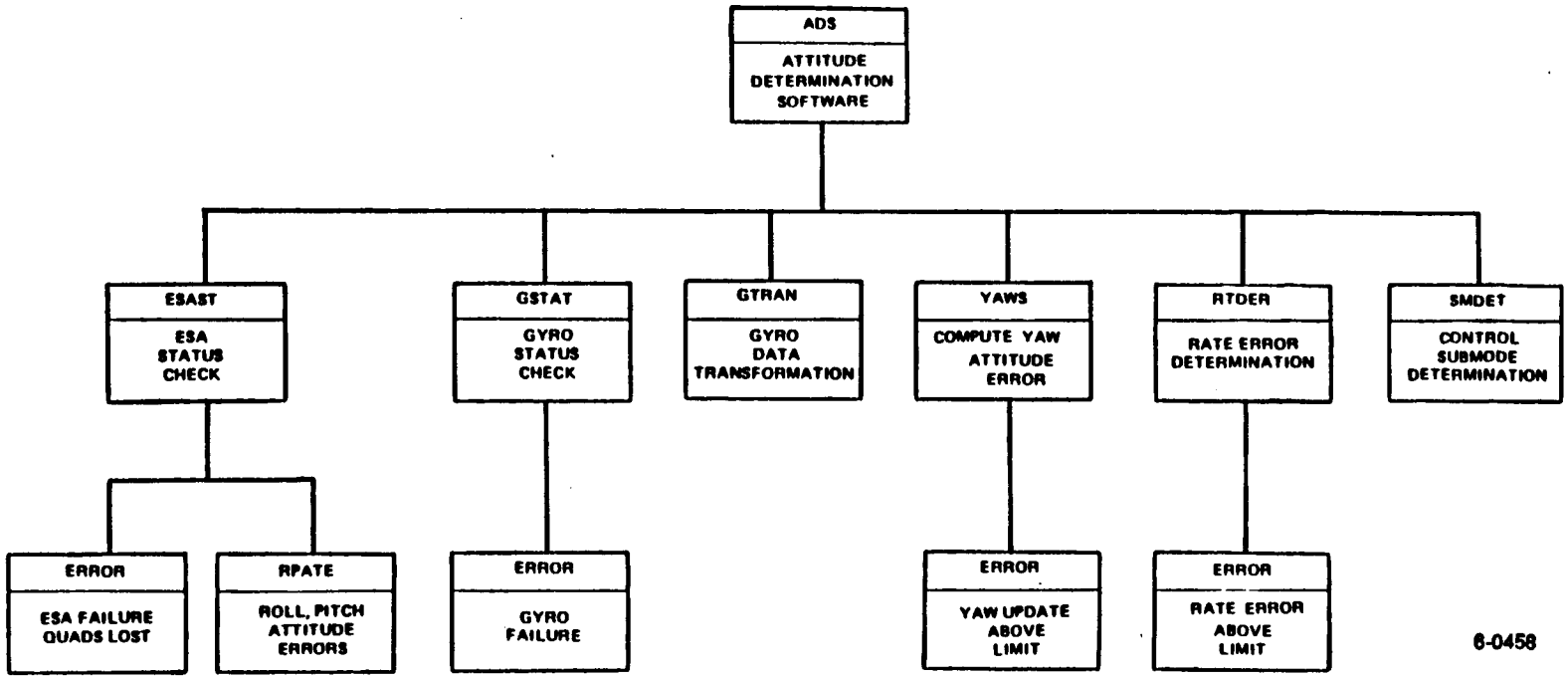

Figure 4.10.6-5. ADS Functional Diagram

the three tests on the ESA data are as follows:

1. If V_{Sn} > SLIM then X_n is set to one for that quadrant.

2. If $V_{Bn} - V_{Sn}$ < BLIM then for this quadrant X_n is set to zero and the quad bit in QLW is set.

3. If $V_{An} - V_{Sn}$ < ALIM then for this quadrant X_n is set to zero and the quad bit in QLW is set.

An additional test shall be made when the last control submode was not Nominal. The term T_2 is tested for the limits:

$$KLIM > T_2 > 0 \qquad (T_2 = V_{AN} + V_{BN} - 2V_{SN})$$

If T_2 is outside the limits, then the quad bit is set in QUW to indicate unusability.

If T_2 is within the limits, then X_n is calculated as follows:

$$X_n = 2\ (T_2/KLIM)$$

In order to minimize the effects of thermal transients (which are the result of acquisition and/or requisition environments) on the ESA output, an alternate ESA quadrant penetration algorithm has been included in the ADS. Algorithm selection, normal or alternate, is controlled by a software flag (FESAALT) which is set for the alternate algorithm. Control of the flag can be accomplished by ground command only. The alternate method of calculating quadrant penetration is

$$X_n = [K_{An}VA_n + K_{Bn}\ VB_n - 2\ K_{Sn}\ VS_n] * KCNTS$$

where KCNTS = a constant, nominally 0.00025

The Quad Use Word is used to control the alternative processing schemes when error or warning conditions exist for some quadrants. When QUW is not zero, then action is taken (Table 4.10.6-1), based on the value of QUW, to replace a parameter or to indicate an ESA failure (FESAOUT set).

If the bit is set for a single quadrant, its parameter Xn shall be recalculated by the following method:

$$X_{\substack{1\\2}} = X_3 + X_4 - X_{\substack{2\\1}} \qquad X_{\substack{3\\4}} = X_1 + X_2 - X_{\substack{4\\3}},$$

where the upper or lower indices are used throughout the expression.

The ESA availability flag, FESAOUT, indicates the usability of the ESA derived data. When insufficient quadrant data is available to provide an estimate of the roll and pitch angles, then FESAOUT is set. If bits from two opposite (1-2 or 3-4) quadrants, or more than two, are set in QUW, the angle computations cannot be carried out and FESAOUT must be set. FESAOUT shall be a double-precision integer.

TABLE 4.10.6-1. DECISION TABLE - QUADRANT USE

Condition Value of QUW	(Quad Use Word) State of Quadrant 4	3	2	1	Action Replace X Parameter As Shown
0	0	0	0	0	Use Nominal X's
1	0	0	0	1	X1 = (X3 + X4 - X2)
2	0	0	1	0	X2 = (X3 + X4 - X1)
3	0	0	1	1	ESA Failure Mode
4	0	1	0	0	X3 = (X1 + X2 - X4)
5	0	1	0	1	X3 = 2X (h) - X4, X1 = 2X (h) - X2
6	0	1	1	0	X3 = 2X (h) - X4, X2 = 2X (h) - X1
7	0	1	1	1	ESA Failure Mode
8	1	0	0	0	X4 = (X1 + X2 - X3)
9	1	0	0	1	X4 = 2X(h) - X3, X1 = 2X (h) - X2
10	1	0	1	0	X4 = 2X(h) - X3, X2 = 2X (h) - X1
11	1	0	1	1	
12	1	1	0	0	ESA Failure Mode
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

Where QUW indicates that two adjacent quadrants cannot be used, each of the values is replaced using the average penetration XAVE for the altitude of the satellite, computed as follows:

$$XAVE = K_1 * ALTITUD + K_2$$

K_1 and K_2 = constants
ALTITUD = spacecraft altitude

Roll, Pitch Attitude Errors (RPATE)

RPATE computes a set of Euler angles in the control frame for the roll and pitch axes. RPATE uses the four penetration parameters X_n previously computed. However, if FESAOUT was set, X_n parameters cannot be calculated, and RPATE processing shall be ignored.

RPATE computes the indicated angles in the ESA frame as follows:

$$A_{12} = KRAD * (X_1 - X_2)$$
$$A_{34} = KRAD * (X_3 - X_4)$$

where KRAD is a constant which converts the data to radians. The angles A_{12} and A_{34} are transformed to the P-frame using the following relationship:

$$APITCH = T_{PE}(2,2) \quad T_{PE}(2,3) \cdot A_{12} + T_{PE}(2,1)$$
$$AROLL = T_{PE}(3,2) \quad T_{PE}(3,3) \cdot A_{34} + T_{PE}(3,1)$$

The transformation matrix T_{PE} from the ESA frame to the Payload frame is determined by measurement of the installed ESA.

The attitude errors shall be AROLL and APITCH for the roll and pitch errors, respectively. These two variables shall be passed to ACS, and are available for CPU telemetry.

Gyro Status Determination (GSTAT)

GSTAT chooses the proper gyro to P-frame transformation based on the gyro status word (either IMU or ground supplied) and the gyro data consistency check defined herein.

GSTAT shall test bit 13 of SIMF (the IMU status word) "Logic", to determine if the primary or backup Pulse Weight logic is used. See Figure 4.10.6-6 for the format of the IMU status word. The flag FSPW shall be set based on this test and will later be used by GTRAN to select the appropriate pulse weight values.

GSTAT shall determine the available gyro channels by the following method:

1. Each cycle, GSTAT shall test the reasonableness of the data for each gyro channel. Reasonableness is based on the torque generated by a runaway RWA. If VGPCi (n) for a channel is greater than GLIM, or if VGPCi (n) -VGPCLi (n - 1) is greater than TOLER, then GRCNT(i) for that channel is incremented by one (where n is the present cycle value of VGPC, n-1 is the last cycle value, and i stands for X_a, Y_a, Z_a, X_b, Y_b, Z_b: the gyro channels).

   If the reasonableness test fails for four consecutive cycles for any given channel, indicated by GRCNT(i), then that channel shall be considered failed and "not available." GSTAT shall set the corresponding bit in the word GRFAIL to indicate this failure.

2. GSTAT shall examine the test and spin motor fail bits of the IMU status word for each channel and gyro respectively.

   If a gyro channel is "in test," then that channel is considered "not available" and the appropriate channel bit in NAVL is set.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

(MSB) BIT	DESCRIPTION	VALUE
1	DC POWER	0: = PRIMARY, 1: = BACKUP
2	AC POWER	0: = PRIMARY, 1: = BACKUP
3	TRIAD B	0: = ON, 1: = OFF
4	TRIAD A	0: = ON, 1: = OFF
5	CS TEST	0: = OFF, 1: = ON
6	ORBIT/ASCENT	0: = ORBIT, 1: = ASCENT
7	Zb TEST	0: = OFF, 1: = "IN TEST"
8	Za TEST	
9	Yb TEST	
10	Ya TEST	
11	Xb TEST	
12	Xa TEST	
13	LOGIC (PULSE WEIGHT)	0: = PRIMARY, 1: = BACKUP
14	GYRO 3 SPIN MOTOR	0: = "FAILED", 1: = "ON AND OK"
15	GYRO 2 SPIN MOTOR	
16	GYRO 1 SPIN MOTOR	

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Figure 4.10.6-6. Format of IMU Status Word

If a gyro spin motor has "failed," then the bits for both channels associated with that gyro will be set to indicate "not available."

3. GSTAT shall examine NAVL by the channel pairs associated with each of the three axes. If both channels for each axis are available, NAVL shall then be modified to show unavailable channels indicated in GFAIL. GFAIL and NAVL are shown in Figure 4.10.6-7

(MSB) 1		11	12	13	14	15	16

BIT	DESCRIPTION	VALUE
11	Zb GYRO CHANNEL	0: = AVAILABLE
12	Za GYRO CHANNEL	
13	Yb GYRO CHANNEL	
14	Ya GYRO CHANNEL	1: = NOT AVAILABLE
15	Xb GYRO CHANNEL	
16	Xa GYRO CHANNEL	

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Figure 4.10.6-7. Format of GRFAIL and NAVL

GSTAT shall then examine NAVL to select the appropriate channels to use in determining the three payload axis (P-frame) body rates. This is accomplished by assigning a value to the index TPIND which will point to one of eight transformation matrices of the array TPG (Transformation - Payload/Gyro). This array is specified in Figure 4.10.6-8.

TPIND	Available Channels	TP Subset
000	X_A Y_A Z_A	TP0
001	X_A Y_A Z_B	TP1
010	X_A Y_B Z_A	TP2
011	X_A Y_B Z_B	TP3
100	X_B Y_A Z_A	TP4
101	X_B Y_A Z_B	TP5
110	X_B Y_B Z_A	TP6
111	X_B Y_B Z_B	TP7

Figure 4.10.6-8. Gyro to Payload Transformation

Each TP Subset is comprised of a 3 x 3, gyro channel to body rate, transformation matrix. The TP Subset element values shall be adjusted for gyro alignment. In the case of perfect alignment, the matrix would look like the following:

$$TP(0\text{-}7) = \begin{array}{ccc} X(A/B) & Y(A/B) & Z(A/B) \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{array} \quad \begin{array}{l} \\ PX \text{ (yaw)} \\ PY \text{ (roll)} \\ PZ \text{ (pitch)} \end{array}$$

Each TPIND bit represents a payload axis, a 0 indicates the selection of the A channel for a given axis while a 1 indicates the B channel. GSTAT shall select the transformation subset index (TPIND) using the following method:

1. The channel selection for each payload axis shall be determined independently.

2. The ground override flag FGORD shall be tested. If FGORD is set, and the appropriate "force" bit of the ground supplied word GTPIND is set, then the A/B bit for this axis, also in GTPIND, shall override the same bit in TPIND. The bit positions for GTPIND are shown in Figure 4.10.6-9.

3. If FGORD has not been set, NAVL shall be examined. If both channels for the axis under test are not available, and channel A is not available (and selected), channel B shall be selected.

4. If both NAVL channels are available, this is the yaw axis, and the Yaw Update Limit flag is set, GSTAT will exclude the last yaw channel selected.

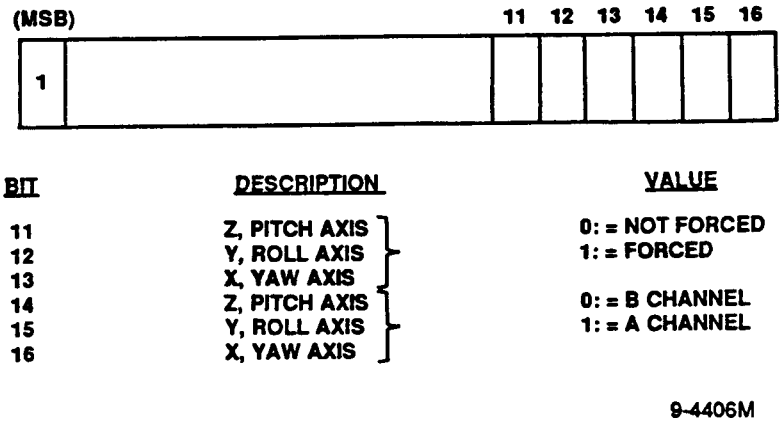


Figure 4.10.6-9. Format of GTPIND

5. If both channels remain available, FGORD shall be examined again. If FGORD is set, the A/B bit from GTPIND shall be used.

6. If TPIND has not been modified by the above process, the channel used during the previous cycle shall again be used.

Gyro Transform (GTRAN)

GTRAN transforms gyro-frame data, available from DFS, into satellite body rates as follows:

1. Convert pulse counts to radians and remove gyro drift which is determined before launch for the gyro channels used. The incremental angular rotations in the gyro becomes:

$$DLTHG_{(i)} = PWGT_{(FSPWti)} \cdot VGPC_{(i)} - BEGIN_{(i)}$$

where DLTHG (i) = scaled gyro output (gyro angular change: "DELTA Theta-Gyro")

PWGT (i) = channel pulse weight (channel dependent)

BGIN (i) = gyro bias (initial gyro drift rate in angular rotation drift per 0.5-second cycle)

FSPW is the primary/backup pulse weight switch

2. Transform to the payload frame:

$$DLTHP\ (i) = DLTHG\ (i) \cdot TPIND\ (j)$$

following method shall be used to compute the latest incremental bias rate correction:

$$b = \delta/T_o \quad \text{where } T_o = \Delta t * \text{ORBIT} * 2\pi$$

where δ is the difference in measured and integrated yaw position and the term, T_o, is the time between updates.

A filter reset flag (FLRST) shall be used to initiate filter values upon initial startup or to reset filter values whenever unusual conditions (e.g., control system mode changes) occur. The flag may be set from the ground or from other modules.

This flag shall be tested by YAWS to see if reset is required. When FLRST = SET then the yaw axis rates bias and filter values are set from the bias rate correction b:

B4 = B3 = B2 = B1 = b, and
Byaw = b

Upon completing a reset YAWS shall CLEAR (:= 0) the flag, FLRST.

If FLRST = CLEAR when tested by YAWS, then the yaw axis bias rate is computed by averaging four filter values based on past values and updated value as follows:

B4 = B3
B3 = B2
B2 = B1
B1 = b + BYAW (old value)
Byaw = (B4 + B3 + B2 + B1)/4

<u>Rate Derivations (RTDER)</u>

DLTHP(z), (Pitch); DLTHP(y), (Roll) := incremental rotation in the payload frame (rad)

$\Delta\alpha$ yaw	:=	incremental rotation out of the orbit plane
YAWB	:=	spacecraft orientation nominally := -1
$\Omega(t)$	:=	average pitch rate of vehicle over orbit period
αyaw	:=	total yaw angle

At each call to RTDER, the module shall compute the body rates using the following equation for all 3 components. RTDER shall make the following substitution $\Delta\alpha yaw$ for $\Delta\theta yaw$ in the equation for Δyaw.

$$W(n) = \frac{3\Delta\theta\ p(n) - \Delta\theta\ p(n-1)}{2\Delta t}$$

where n refers to the value at this sample and n-1 to the value at the last sample interval. This technique is a second order differentiation method.

The control rates shall be formed from the body rates as follows:

$\dot{\alpha}roll := W\ roll + YAWB * \Omega\ (t)\ Sin\ (\phi yaw)$

$\dot{\alpha}yaw := \Delta\alpha\ yaw/\Delta t$

$\dot{\alpha}pitch := W\ pitch + YAWB * \Omega\ (t)\ Cos\ (\phi yaw)$

Submode Determination (SMDET)

Based on the last control submode, the yaw angle ϕyaw, shall be defined for the control rate determination as follows:

Submode	Value of ϕ yaw
NOM	αyaw
COAST	αyaw
RN	0
SEARCH	0
YGC	0

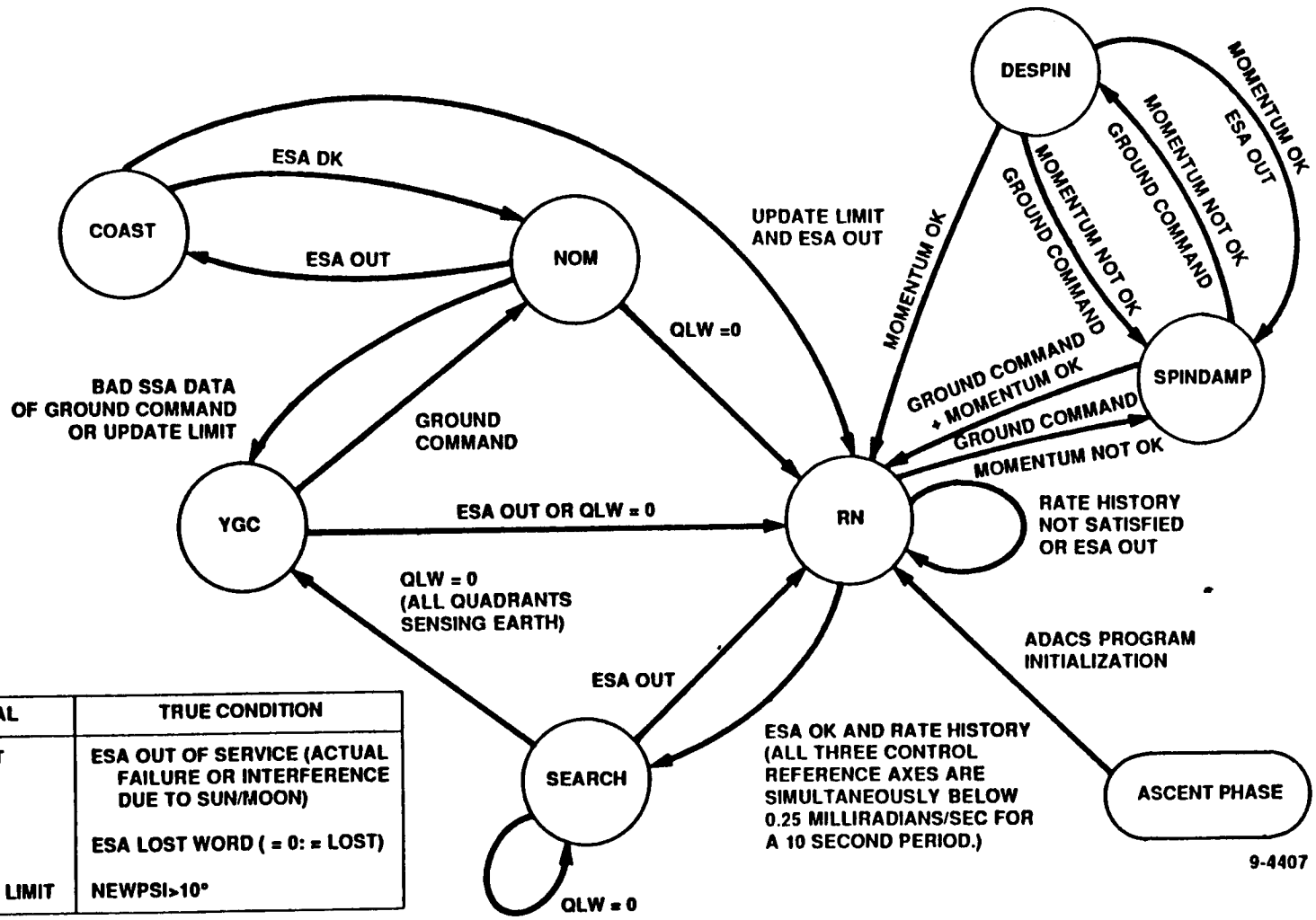
After the three body error-rates are computed, RTDER shall perform the following test to determine rate history for submode determination by SMDET:

1. If all α_i's < RTLM, then
   a. CNTR = CNTR + 1
   b. If CNTR > 20 then FRTERR = CLEAR and CNTR = 20

2. If any α_i > RTLM then
   a. FRTERR = SET
   b. CNTR = 0

   where: RTLM is the rate limit magnitude.

The FRTERR flag shall be set if any error-rate exceeds the limits and will be cleared if the error-rates remain within the limits for 20 consecutive cycles. FRTERR shall be initially set.



SIGNAL	TRUE CONDITION
ESA OUT	ESA OUT OF SERVICE (ACTUAL FAILURE OR INTERFERENCE DUE TO SUN/MOON)
QLW	ESA LOST WORD (= 0: = LOST)
UPDATE LIMIT	NEWPSI>10°

Figure 4.10.6-10. Attitude Control Mode Switching

FRTERR := rate error history
:= SET if any rate limit exceeded
:= CLEAR if all rate limit met for 10 seconds (10 consecutive cycles)

FLRST := reset filter flag

FUPLIM := update limit exceeded flag

FYGC := YGC Flag
Set := Commanded to YGC submode by MODE
Clear := Not commanded to YGC submode by MODE

SMDET shall determine the submode control based on past submode, ESA out of service, ESA quadrant lost, rate history and update limit as defined in Table 4.10.6-2.

SMDET shall save the previous submode, word SMODEL, from the submode word, SMODE, before determining the new submode word.

<u>NOM Decisions</u> - When SMODEL is set to NOM,

1. if FESAOUT = CLEAR, QLW = 0, and FUPLIM = CLEAR then SMODE shall be set to NOM.

2. if FESAOUT = SET then SMODE shall be set to COAST.

3. if FESAOUT = CLEAR, and QLW ≠ 0, then SMODE shall be set to RN

4. if FESAOUT = CLEAR, QLW = 0, and (FUPLIM = SET or FYGC = SET) then SMODE shall be set to YGC and for ATN the integral term of the YGC control law shall be set to YINTINTL which is nominally zero.

<u>COAST Decisions</u> - When SMODEL is set to COAST,

1. if FESAOUT = SET and FUPLIM = CLEAR then SMODE shall be set to COAST.

2. if FESAOUT = SET and FUPLIM = SET then SMODE shall be set to RN.

3. if FESAOUT = CLEAR then SMODE shall be set to NOM.

<u>RN Decisions</u> - When SMODEL is set to RN,

1. if FRTERR = SET then SMODE shall be set to RN.

2. if FESAOUT = SET then SMODE shall be set to RN.

3. if FESAOUT = CLEAR and FRTERR = CLEAR then SMODE shall be set to SEARCH.

TABLE 4.10.6-2. DECISION TABLE - SUBMODE DETERMINATION

SUBMODE ON LAST CYCLE	NOM	NOM	NOM	NOM	NOM	CST	CST	CST	RN	RN	RN	RN	SRCH	SRCH	SRCH	YGC	YGC	YGC	YGC	SDMP	SDMP	DSPN	DSPN	DSPN
ESAOUT	NO	YES	NO	NO	NO	YES	YES	NO	NO	YES	—	NO	NO	YES	NO	NO	YES	NO	NO	NO	NO	—	NO	YES
QLW (NOT ZERO IS QUAD LOST)	0	—	NOT 0	0	0	—	—	—	—	—	—	—	NOT 0	—	0	0	—	NOT 0	0	—	—	—	—	—
RATES KILLED	—	—	—	—	—	—	—	—	NO	—	YES	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUND COMMAND	—	—	—	—	—	—	—	—	—	—	—	YES	—	—	—	NO	—	—	YES	YES	YES	—	YES	—
UPDATE LIMIT	NO	—	—	YES	NO	NO	YES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	..
FYGC	—	—	—	—	SET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
MOMENTUM OK	—	—	—	—	—	—	—	—	—	—	—	NO	—	—	—	—	—	—	—	YES	NO	YES	NO	YES
SUBMODE SHALL BE	NOM	CST	RN	YGC	YGC	CST	RN	NOM	RN	RN	SRCH	SDMP	SRCH	RN	YGC	YGC	RN	RN	NOM	RN	DSPN	RN	SDMP	SDMP

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SYMBOL	DEFINITION
—	DO NOT CARE
NOM	NOMINAL MODE
CST	COAST MODE
RN	RATE NULLING MODE
SRCH	SEARCH MODE
YGC	YAW GYROCOMPASSING MODE
SDMP	SPINDAMPING MODE
DSPN	DESPIN MODE
FYCG	FORCED YGC CONDITION

SEARCH Decisions - When SMODEL is set to SEARCH,

1. if FESAOUT = Clear and QLW ≠ 0 then SMODE shall be set to SEARCH.

2. if FESAOUT = SET then SMODE shall be set to RN.

3. if FESAOUT = CLEAR, and QLW = 0 then SMODE shall be set to YGC and for ATN the integral term of the YGC control law shall be set to YINTINTL which is nominally zero.

YGC Decisions - When SMODEL is set to YGC,

1. if FESAOUT = CLEAR and QLW = 0 then SMODE shall be set to YGC.

2. if FESAOUT = SET then SMODE shall be set to RN.

3. if FESAOUT = CLEAR and QLW ≠ 0 then SMODE shall be set to RN.

4. if FESAOUT = CLEAR, QLW = 0 and FCMDNM = SET then SMODE shall be set to NOM.

Inputs and outputs are described below (see Figure 4.10.6-11).

Symbol	Source Module	Description
VGPC (6)	DFS	Gyro pulse count vectors
SIMU	DFS	IMU status word
FYAWUP	GEODAT	YAW update flag
NEWPSI	GEODAT	YAW angle update
SINB	GEODAT	Sine of orbit anomaly
ALTITUD	GEODAT	Attitude of spacecraft (h)
SMWARN	GEODAT	Sun/moon warning word
FYGC	MODE	YGC flag
ESRABF	MODE	ESA buffer use flag
SGIMU	GROUND	Ground override of IMU status
AROLL	ADS	Roll Attitude Error
APITCH	ADS	Pitch Attitude Error
AYAW	ADS	Yaw Attitude Error
SMODE	ADS	Submode control word
QLW	ADS	Quad lost word
QUW	ADS	Quad use word
FRTERR	ADS	Rate error flag
GRFAIL	ADS	Gyro failure word
GRCNT(4)	ADS	Count of each gyro failure
FESAOUT	ADS	ESA failure or sun moon interface
FCMDNM	Ground	Flag to switch from YGC to Nominal Submode
FGORD	Ground	Flag Ground override to IMU status
GQUW	Ground	Ground override of Quad use Word

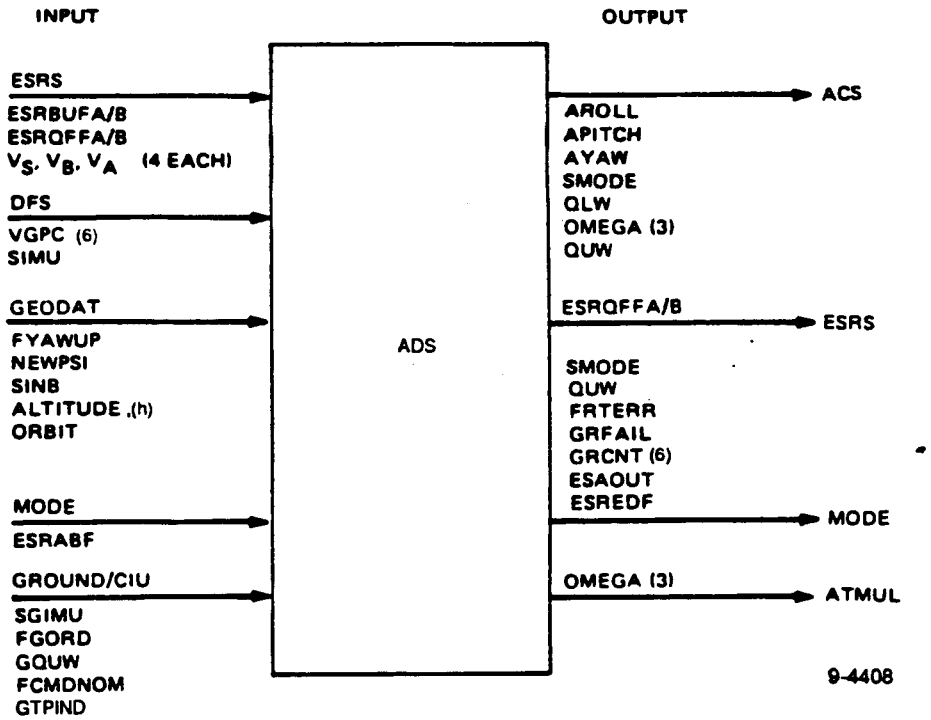

Figure 4.10.6-11. ADS Input/Output Requirements

ADS Telemetry Parameters

The ADS words available for telemetry are defined as follows:

Symbol	Parameter
XAVG	Average Penetration
QLW	Quad Lost Word
FSPW	Switch Pulse Weight Flag
QUW	Quad Use
DLTH	3 x 1 P-Frame Vector
FESAOUT	ESA Failure Flag
DLTHL	Last 3 x 1 P-Frame Vector
TPIND	Gyro Configuration Index
B0, B1, B2, B3	Past/Updated Filter Valves to Determine BYAW
XN(4)	ESA Quadrant Computed Penetration
FLRST	Filter Reset Flag
NEWPSI	Yaw Attitude Update
TPINDL	Last TPIND Word
BYAW	Yaw Gyro Bias
CNTR	Rate Limit Exceeded Counter
AYAW	Yaw Attitude Error
VGPCL (6)	Last Cycle IMU Data
AROLL	Roll Attitude Error
APITCH	Pitch Attitude Error
OMEGA(3)	Body Rate Errors
SMODE	ADACS Control Mode
SMODEL	Last SMODE Word

4.10.6.5 Attitude Control Software (ACS)

The Attitude Control Software module is called as a subroutine once each 0.5 second computational cycle.

The prime function of ACS is to compute, format, and transmit the attitude control signals to the reaction wheels. ACS receives a set of Euler error-angles, body rates, and the attitude control submode to compute the torque commands for reaction wheels.

ACS determines which RWAs are available, chooses three RWAs for use, and tests the RWAs when required. ACS also extracts the three equivalent orthogonal wheel speeds from the four RWA status words. ACS terminates MMU coil pulse discretes and issues MMU coil commands via CMDPRO as requested. The condition of the MMU coils is available to ACS and it utilizes this information to effect corrections to the torque commands. The ACS module is defined functionally in Figure 4.10.6-12.

RWA Speeds and Status (RWASS)

Each time ACS is entered the four RWA status words are examined and the wheel speeds and power status are extracted by RWASS. One RWA status word is updated by TIREX each computational cycle (0.5 second).

RWASS converts the sign-magnitude speeds as given in the status word array WFW(4) to two's-complement form for use in the CPU. The speeds are stored in the array WWH(4).

RWASS computes the three equivalent orthogonal speeds components from the four speed components. These are stored in WOR(3) as follows:

$$WOR(1) = WWH(X) + WWH(S)/\sqrt{3}$$
$$WOR(2) = WWH(Y) + WWH(S)/\sqrt{3}$$
$$WOR(3) = WWH(Z) + WWH(S)/\sqrt{3}$$

RWASS also stores the absolute value of the orthogonal components in WMAG(3) for all three orthogonal speeds.

The power status bits (i.e., power on/off), as given in the four RWA status words, are combined into a single word RWAS.

RWA Sufficiency Test (RWAST)

RWAST assures that three wheels are powered on each time ACS is entered.

1. If at least three wheels are powered 'on' then no action is needed.

2. If less than three wheels are powered 'on' then RWAST issues the commands via CMDPRO to turn on the three orthogonal wheels and turn off the skew wheel.

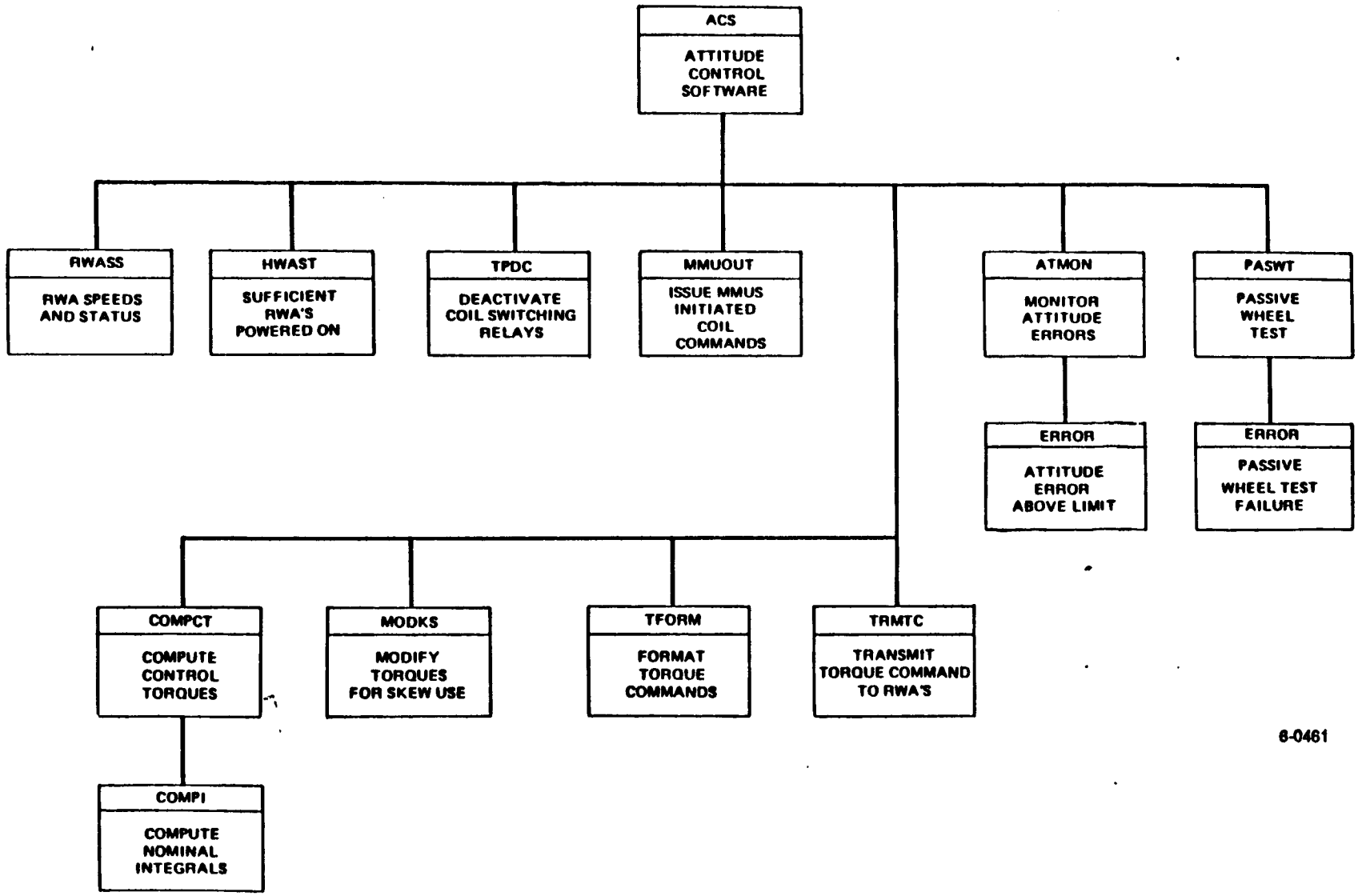

Figure 4.10.6-12. ACS Functional Diagram

Terminate Pulse Discretes to Coils (DRLAY)

DRLAY issues the command for deactivating the latching relays of the Magnetic Momentum Unloading (MMU) coils via the CMDPRO module for the MMUS module.

The switching of the MMU coils is effected by latching relays. The pulses necessary to latch these relays are generated by issuing two separate commands approximately 0.5 second apart.

MMUS formats and requests ACS to issue the first command. DRLAY automatically formats and issues the second command upon entry to ACS.

DRLAY issues the appropriate commands for the selected bus.

MMU Initiated Coil Commands (MMUOUT)

Upon each entry to ACS, MMUOUT issues MMUS initiated coil commands via the CMDPRO module. MMUS signals ACS to issue coil commands by setting NCMD to the number of commands in the command table, MMUCMD. Otherwise, NCMD is set to zero.

All coil commands have been formatted for both buses. Therefore, ACS tests the connected bus indicator, FBUS, and the buffer image index to determine which coil commands to use.

After all coil commands are examined and pertinent commands issued, NCMD is set to zero. Also the torque compensation terms are saved for use in the control torque computations to be made from this cycle until the next set of coil commands are received.

Computation of Control Torques (COMPCT)

Input to COMPCT

COMPCT shall require the following inputs:

αx, αy, αz:= Euler error-angles

$\dot{\alpha} x$, $\dot{\alpha} y$, $\dot{\alpha} z$: = body error-rates
ANTREQ(3): = anticipatory torque requests
UC1, UC2, UC3: = MMU compensation terms
SMODE: = submode code
YAWB: = yaw orientation
INT (N): = value of the integral at present time t
: = YINT, RINT, PINT

COMPCT shall examine the submode (SMODE) to determine the processing branch. The submodes are NOM, COAST, RN, SEARCH, and YGC. The control law dependence on submode is summarized in Table 4.10.6-3. The control torque computation is described below:

1. FMMUIN shall be cleared, to be set as required.

2. If SMODE is set to NOM then

   a. When SMODEL is not set to NOM, then the axis integrals shall continue with past values, INT (n-1), as computed from previous submodes.

      The integrals shall be numerically evaluated by the method in COMPI providing the axis is not inhibited by being in a non-linear region of the wheel.

   b. FMMUIN shall remain cleared.

   c. control torques shall be computed by the generic form of the control law.

   d. control torques for NOM submode or generic form of the control laws shall be computed in two steps as follows:

      d.1 Torque due to acceleration,

      $$T_{Ai} = K_{1i} * \alpha_i = K_{2i}\ \dot{\alpha}_i$$

      The T_A's shall be saved for use in PASWT.

      d.2 Control torque

      $$T_{Ci} = T_{Ai} + INT_i - K_{5i}\delta_i$$

3. If SMODE is set to COAST then

   a. FMMUIN shall remain cleared

   b. yaw axis shall be computed by generic form of the control law as in NOM.

   c. roll and pitch torques shall be computed as follows:

      $$T_{cy} = -\ (K_{7y} * \dot{\alpha}_y + RINT)$$

      $$T_{cz} = -\ (K_{7z} * \dot{\alpha}_z + PINT)$$

   where the integrals are to be numerically evaluated by the method in Paragraph 7, and no limiting shall be applied to these integrals.

TABLE 4.10.6-3. ATTITUDE CONTROL LAWS

Submode	Axis	Control Law	Integral Term Limit TRN	Integral Term Limit ATN	Notes
NOMINAL SMODE = 0	Yaw	$\pm(K_{1x}\,\alpha_x + K_{2x}\,\dot{\alpha}_x\,[-K_{5x}\,\delta_x] + \int_T^t (K_{3x}\alpha_x\ [-K_{6x}\delta_x])\,(1-STP_x)\,dt + C_x(T))$	±60	±60	
	Roll	$\pm(K_{1y}\,\alpha_y + K_{2y}\,\dot{\alpha}_y\,[-K_{5y}\,\delta_y] + \int_T^t (K_{3y}\alpha_y\ [-K_{6y}\delta_y])\,(1-STP_y)\,dt + C_y(T))$	±60	±60	
	Pitch	$\pm(K_{1z}\,\alpha_z + K_{2z}\,\dot{\alpha}_z\,[-K_{5z}\,\delta_z] + \int_T^t (K_{3z}\alpha_z\ [-K_{6z}\delta_z])\,(1-STP_z)\,dt + C_z(T))$	±60	±60	
RATE NULLING SMODE = 1	Yaw	$K_{7x}\dot{\alpha}_x + K_{8x}\int_T^t \dot{\alpha}_x dt + C_x(T)$		±500	
	Roll	$-(K_{7y}\dot{\alpha}_y + K_{8y}\int_T^t \dot{\alpha}_y dt + C_y(T))$		±500	
	Pitch	$-(K_{7z}\dot{\alpha}_z + K_{8z}\int_T^t \dot{\alpha}_z dt + C_z(T))$		±500	
YAW GYRO COMPASSING SMODE = 2	Yaw	$KG2\dot{\alpha}_x - YAWB\ KG1\ \dot{\bar{\alpha}}_y + \begin{cases} C_x(T) & \text{TIROS-N} \\ YINTINTL & \text{ATN} \end{cases}$			YINTINTL is a constant which may be altered by the ground
	Roll	$\pm(K_{1y}\,\alpha_y + K_{2y}\,\dot{\alpha}_y\,[-K_{5y}\,\delta_y] + \int_T^t (K_{3y}\alpha_y\ [-K_{6y}\delta_y])\,(1-STP_y)\,dt + C_y(T))$	±60	±60	$\dot{\bar{\alpha}}_y = MIN\,(1, MAX\,(-1, \dot{\alpha}_y))$
	Pitch	$\pm(K_{1z}\,\alpha_z + K_{2z}\,\dot{\alpha}_z\,[-K_{5z}\,\delta_z] + \int_T^t (K_{3z}\alpha_z\ [-K_{6y}\delta_y])\,(1-STP_z)\,dt + C_z(T))$	±60	±60	
SEARCH SMODE = 3	Yaw	$K_{7x}\,\dot{\alpha}_x + K_{8x}\int_T^t \dot{\alpha}_x dt + C_x(T))$		±500	
	Roll	$-(K_{7y}\,\dot{\alpha}'_y + K_{8y}\int_T^t \dot{\alpha}'_y dt + C_y(T))$		±500	$\dot{\alpha}'_y = \dot{\alpha}_y - \omega_{cy}$
	Pitch	$-(K_{7z}\,\dot{\alpha}'_z + K_{8z}\int_T^t \dot{\alpha}'_z dt + C_z(T))$		±500	$\dot{\alpha}'_z = \dot{\alpha}_z - \omega_{cz}$
COAST SMODE = 4	Yaw	$\pm(K_{1x}\,\alpha_x + K_{2x}\,\dot{\alpha}_x\,[-K_{5x}\delta_x] + \int_T^t (K_{3x}\alpha_x\ [-K_{6x}\delta_x])\,(1-STP_x)\,dt + C_x(T)$	±60	±60	
	Roll	$-(K_{7y}\,\dot{\alpha}_y + K_{8y}\int_T^t \dot{\alpha}_y + C_y(T))$		±500	
	Pitch	$-(K_{7z}\,\dot{\alpha}_z + K_{8z}\int_T^t \dot{\alpha}_z + C_z(T))$		±500	

For $i = x,y,z$: $C_i(T)$ is the value of the integral term INT (i) at time T = time of last transition to this submode. STP(i) are flags indicating whether (=0) or not (=1) the integration for Axis i is to be performed.
Non-limited integral terms are subject to overflow and consequent sign reversal.
[·] are terms which are used only during unloading by MMUS.

4. If SMODE is set to RN then

   a. the control torques shall be computed as follows:

      $Tcx = K_{7x}*\dot{\alpha}_x + YINT$

      $Tcy = -(K_{7y}*(\dot{\alpha}_y) + RINT)$

      $Tcz = -(K_{7z}*(\dot{\alpha}_z) + PINT)$

   b. integrals are to be numerically evaluated by the method in Paragraph 7, and no limiting shall be applied to these integrals.

   c. FMMUIN shall be set.

5. If SMODE is set to SEARCH, then the control torques shall be computed as follows:

   a. $Tcx = K_{7x}*\dot{\alpha}_x + YINT$

      $Tcy = -(K_{7y}*(\dot{\alpha}_y) + RINT);\ \dot{\alpha}_y' = \dot{\alpha}_y - \omega_{cy}$

      $Tcz = -(K_{7z}*(\dot{\alpha}_z) + PINT);\ \dot{\alpha}_z' = \dot{\alpha}_z - \omega_{cz}$

      The rates used in the roll and pitch integral and torque calculations are corrected by the terms W_{cy} and W_{cz} which are commanded search rates determined from Table 8 using the quad lost word, QLW, and quad use word, QUW, as follows (see Figure 4.10.6-13):

      a.1 QSW = QLW.
      a.2 If QUW $\neq$ 0

      then

      a) if (QLW 'and' QUW) $\neq$ 3, 12, or 15 then
      QSW = QSW 'or' QUW

      a.3 Search rates can be found in Table 4.10.6-4 based on QSW.

   b. normally this submode is entered from the RN submode; therefore, the integrals shall have the same values that they had on the last computational cycle in the RN submode.

   c. the integrals for SEARCH submode shall be computed as in Paragraph 7.

   d. FMMUIN shall be set.

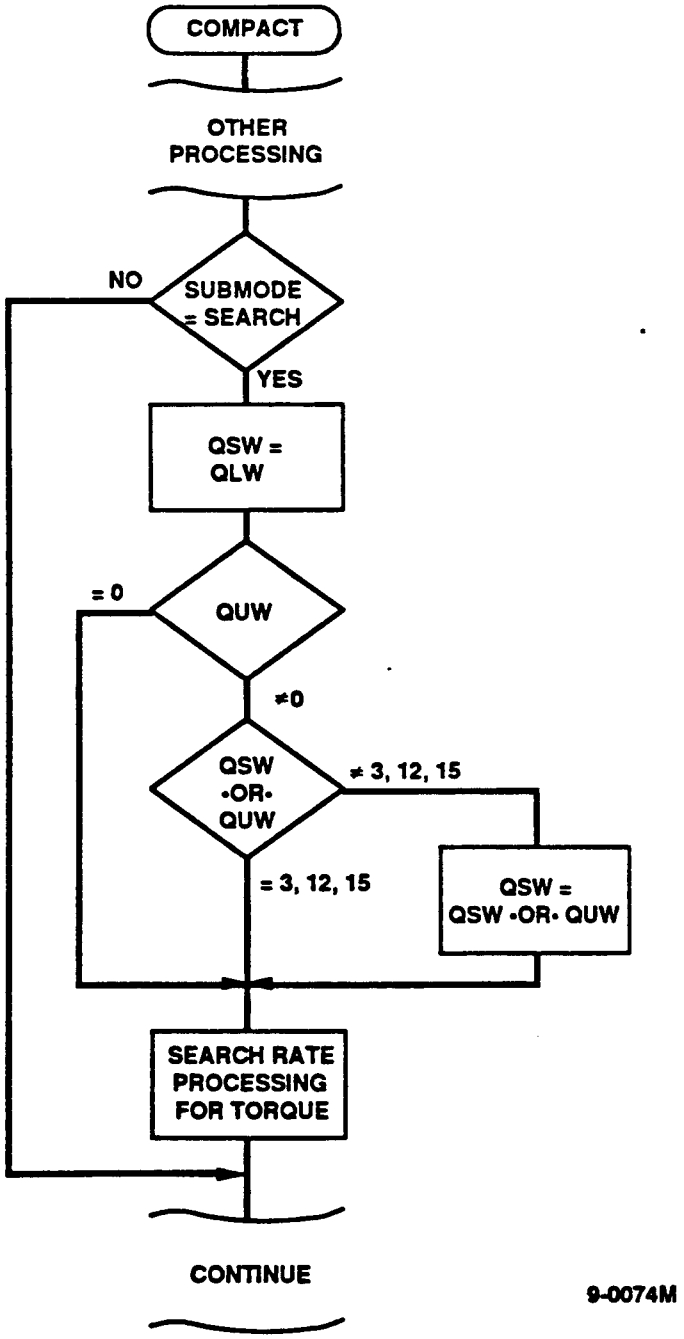

Figure 4.10.6-13. Search Mode Processing Using QUW and QLW

TABLE 4.10.6-4. SEARCH RATE DECISION TABLE

Condition							Action
QLW (Magnitude)	Quadrant State				Command Rate		Notes
	4	3	2	1	Pitch (W_{Sz})	Roll (W_{Sy})	
0	0	0	0	0	Normal	Control	Locked on Earth
1	0	0	0	1	+B	+C	
2	0	0	1	0	-B	-C	
3	0	0	1	1	-	-	Geometrically excluded
4	0	1	0	0	-B	+C	
5	0	1	0	1	0	+C	
6	0	1	1	0	-B	0	
7	0	1	1	1	-B	+C	
8	1	0	0	0	+B	-C	
9	1	0	0	1	+B	0	
10	1	0	1	0	0	-C	
11	1	0	1	1	+B	-C	
12	1	1	0	0	-	-	Geometrically excluded
13	1	1	0	1	+B	+C	
14	1	1	1	0	-B	-C	
15	1	1	1	1	±A	0	Sign of A depends on pitch axis, RWA speed, i.e., + for + speed.

Logical 0: = Normal (on Earth)
Logical 1: = Quadrant off Earth

A=2B
B=0.002618 rad/sec
C=0.001571 rad/sec

6. If SMODE is set to YGC then

   a. the control torques for roll and pitch axes shall be computed by the generic form of the control law as in NOM.

   b. the control torques for yaw axes shall be computed as follows:

      $Tcx = K2g*\dot{\alpha}_x - YAWB * K1g*\dot{\alpha}y + YINT\ (n-1)$

      where $\dot{\alpha}_y$ is limited to a magnitude of RRL
      where K1g and K2g are constants

   c. if $\dot{\alpha}y$ exceeds the limiting value YRL, then FMMUIN shall be set; else FMMUIN shall remain cleared.

d. when SMODE was not YGC the previous cycle, then the roll and pitch integrals shall be computed using past integrals from RN or SEARCH submodes.

7. If SMODE is set to Rate Nulling, Search, or Coast, Integral calculation with no limiting and speed reversal corrections is as follows (see Table 4.10.6-4:

$INT_i\ (n) = INT\ (n-1) + K8_i*(\dot{\alpha}_i'(n) + \dot{\alpha}_i'(n-1))$

$\dot{\alpha}_i'\ (n) = \dot{\alpha}_i(n) - (\omega_{cy}$ or $\omega_{cz})$ for Search mode

$\dot{\alpha}_i'\ (n) = {}_i(n)$ for Rate Nulling and Coast

8. After the desired torques have been computed, ANTREQ shall be examined for each axis i: = 1 to 3.

   a. If ANTREQ(i) = 0, then the previously computed torque value shall be used for axis i.

   b. In ANTREQ(i) ≠0, then the value of ANTREQ shall determine the torque for axis i, resulting in a positive or negative maximum torque according to the axis sign convention in ATMUL.

Compute Integrals (COMPI)

COMPI computes nominal integral terms using the trapezoidal rule as follows:

A. the integral

$$Y(T) = \int_0^t f[x(t)]\ dt \text{ is replaced by}$$

$$SUM(n) = SUM(n-1) + \frac{(f(X_n) + F(X_{n-1}))\Delta t}{2}$$

where SUM(n) is the value of the integral at $t = n\Delta t$. Specifically $f(x) = \alpha$(Euler error-angles)

B. Initially all past values [i.e., SUM(n-1) are set to zero

C. When the integration is to be reset, then the past value [SUM(n-1)] is set to zero.

Whenever the RWA associated with a given axis is in the non-linear region, as indicated by bit 5 of the status word, the integrations associated with the torque computations on that axis are inhibited.

The integral terms are held fixed until the RWA goes back into the linear mode of operation at which time integration is resumed.

When the skew wheel replaces any of the three orthogonal wheels, its mode of operation governs the integration on the axis of the wheel that is replaced.

When momentum unloading is initiated on an axis, COMPI modifies the integral term for that axis by the terms $(-K_6xUC1)$, $(-K_{6y}UC2)$, or $-K_{6z}UC3)$.

When the speed count on the ith wheel approaches zero; i.e., when $|WWH(i)| >$ FPLM, the sign of the integral term in the control law is reversed for the axis for which the wheel is utilized. (The index i = 0, 1, 2, or 3 for the yaw, roll, pitch, and skew wheels, respectively, and FPLM = 1 count). For the roll and yaw axes, a correction term is added also to the respective control law. To inhibit unnecessary switching, a separate flag in software inhibits sign reversal, etc., until $|WWH(i)| >$ FPLM again.

Yaw Axis Control Law Modifications:

When $|WWH(X)| <$FPLM,
$[K_{3X}\int\alpha_X dt]_{NEW} = -[K_{3X}\int\alpha_X dt]_{OLD} - YAWB*CPL*WOR(Y)$
where YAWB = -1, CPL = a constant,
and WOR(Y) = roll axis wheel speed component in RPM (algebraic value)

Roll Axis Control Law Modifications:

When $|WWH(Y)| <$ FPLM
$[K_{3Y}\int\alpha_Y dt]_{NEW} = -[K_{3Y}\int\alpha_Y dt]_{OLD} + YAWB*CPL*WOR(X)$
where WOR(X) = yaw axis wheel speed component in RPM (algebraic value)

Pitch Axis Control Law Modifications:

When $|WWH(Z) <$ FPLM
$[K_{3Z}\int\alpha_Z dt]_{NEW} = -[K_{3Z}\int\alpha_Z dt]_{OLD}$

The contribution of the integral term to the control torque for any axis is listed in Table 4.10.6-3.

If the ADACS control mode is NOM, YGC or COAST when GN_2 unloading is required, then ATMUL will override the torque command with a torque command that will reduce the wheel speeds on the affected axes in anticipation of a thruster firing.

Modify Torque for Skew Wheel (MODSK)

The control torques formulated apply to the control axes and not directly to the RWA wheels used unless the three orthogonal wheels are used for those axes. When the skew wheel replaces one of the orthogonal wheels, the MODSK reformulates the commands to account for skew geometry.

MODSK tests the power status word, RWAS, for each RWA for "not powered" status.

MODSK tests AWTIP for each RWA for "under test" status.

1. If any RWA meets either condition, then that wheel is not "available" and the skew wheel is to be substituted for the out-of-service wheel.

2. If all three orthogonal RWAs are "available," then torque commands shall be used as generated, even if the skew wheel is also available.

3. If the skew wheel is substituted for an orthogonal wheel, the torque commands shall be adjusted as follows:

   T_i = min(Ti,C255/√3)

   T_s (skew wheel): = √3 T_i

   T_k (other orthogonal): = $T_K - T_i$

   where i = y, r, or p "as failed"

   k = whichever axes have not failed

   ACS shall issue commands only to the three RWAs which are available. The torque command to the fourth unit shall be issued only if it is in test.

Torque Formatting (TFORM)

TFORM formats the control torques for sign-magnitude, and rounds and limits the control torques for formatting as torque commands.

Rounding the control torques is accomplished by adding a dither term, dn, to the magnitude of each torque and truncating the result to the largest integer less than the value. The elements of dn are used in sequence on sequential computational cycles. When all four values have been used they are repeated. dn has the values 0.125, 0.625, 0.375, 0.875.

TFORM also limits the torque magnitude to 255 counts.

Transmission of Commands (TRMTC)

When all three control torque commands have been computed and quantized, TRMTC converts them to a 16-bit format and transmits them to the RWA D/A converter.

Each command contains the command torque in sign magnitude form and a wheel selection code for the command torque, as in Figure 4.10.6-14.

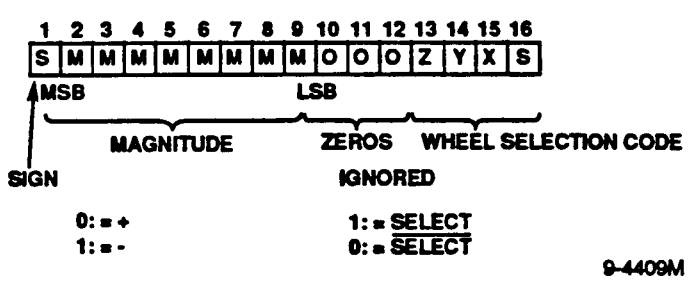

Figure 4.10.6-14. Structure of RWA Command Word

TRMTC waits for the RWA D/A converter to become ready before issuing the last two commands.

Attitude Error Monitor (ATMON)

ATMON monitors the attitude error for each axis when the control submode is set to NOM. When the attitude error for any axis is above the limit for two consecutive cycles, then the attitude error flag, FATEER, is set to alert the MODE module. Also ATMON initiates a passive wheel test request on that axis.

ATMON shall require the following inputs:

AROLL = αroll:= roll attitude error

AYAW = αyaw:= yaw attitude error

APITCH = αpitch:= pitch attitude error

AWTIP = Active wheel test in progress flag

ATMON Processing

ATMON shall perform the following computations on each axis:

1. If an active wheel test is in progress, AWTIP $\neq$ 0, or if a passive wheel test is in progress or passive wheel tests requested (PWTIP $\neq$ 0), then ATMON shall not perform its function.

2. If SMODE is set to NOM, then ATMON shall perform the following:

   A. Compare the absolute value of α_i against the limit, ATLIM - if $|\alpha_i| \geq$ ATLIM then increment the error counter for that axis, CNT(i), which shall initially be set to zero.

   B. Test the error counter, CNT(i), for that axis:

      If the error counter for that axis is CNT(i) $\geq$ 2 then

      i FATERR shall be set

      ii Passive wheel test request flag set for that axis (PWTY, PWTR, PWTP)

      iii CNT(i) = zero, count cleared for axis tested.

      If the skew wheel is in use, then the flag set for this axis shall reflect the skew wheel action as well as the orthogonal wheels in use. Otherwise, the passive wheel test shall reflect the orthogonal wheel, only.

   C. Continue test on other axes.

   D. If $|\alpha_i|$ < ATLIM, then clear the error counter for that axis, CNT(i), and continue the test on other axes.

3. If SMODE is not set to NOM, then ATMON shall not perform its function.

Passive Wheel Test (PASWT)

PASWT shall test one axis at a time when a large attitude error exists. A passive wheel test shall not be initiated or completed when an active wheel test is in progress. Torque sufficiency shall be tested before initiating the test on an axis.

This test shall reflect those wheels turned on for that axis. Two failures of the test shall be required to indicate failure on that axis. If the skew wheel is not available for switching failed wheel to skew wheel for that axis, then the failure shall be flagged instead.

PASWT Processing. PASWT shall initiate the passive wheel test on an axis or continue a passive wheel test already in progress as follows:

1. If GN_2 unloading is in progress (NULINP $\neq$ 0), or an active wheel test is in progress (AWTIP $\neq$ 0), then no passive wheel test shall be continued or initiated. The following will be reset:

   a. ECNT = 1
   b. NTHC = 0
   c. PWTIP = 0

   When the active wheel test has cleared, then the ATMON function shall be allowed to resume and PASWT as needed.

2. If a passive wheel test is not in progress (PWTIP $\leq$ 0), then PASWT shall test the request flags.

   a. If more than one request (PWTR, PWTP, PWTY = 1), then they shall be honored consecutively in that order and ATMON will be locked out until these requests are honored (PWTIP = -1).

   b. When a request is honored on an axis, the request flag shall be cleared.

   c. The test in progress flag, PWTIP, shall reflect the axis test being conducted (PWTIP = 1, yaw; = 2, roll; = 3, pitch).

   d. When all requests have been honored, then ATMON will resume (PWTIP = 0).

3. PASWT shall use the entry counter (ECNT) to indicate the state of the test. This counter shall be initially set to 1 and thereafter reset to 1 whenever a test is completed.

PASWT shall perform testing in the following phases:

Initiate Phase - If the entry counter (ECNT) equals 1 then

a. Test the magnitude of the torque due to acceleration, Ta(I), for axis being tested.

If $|Ta(I)| \geq TLIM$

then a.1 increment entry counter ECNT = ECNT+1

a.2 reset "do nothing" counter NTHC = 0

a.3 save present value, WI, of wheel velocity $|WOR(I)|$ for axis under test

a.4 Return from PASWT

b. If Ta is insufficient to initiate testing, $|Ta(I)| < TLIM$, then increment the "do nothing" counter (initially set to zero) - NTHC = NTHC+1.

c. Test the "do nothing" counter for five attempts to initiate test. If NTHC <5, then RETURN from PASWT else

c.1 reset the counter, NTHC = 0
c.2 clear the test in progress flag PWTIP = -1
c.3 RETURN from PASWT

<u>Delay Phase</u> - If the entry counter (ECNT) equals 2, 3, or 4, then

a. Increment entry counter, ECNT = ECNT + 1
b. RETURN from PASWT

PASWT must wait five cycles for a new wheel speed on the axis.

<u>Test Phase</u> - If the entry counter equals 5, ECNT = 5, then complete the test phase and reset ECNT to 1.

a. Obtain the latest value, WF, of WOR(I) for the axis under test: $\Delta W = WF - WI$.

b. If Ta(I) is negative, then $\Delta W = -\Delta W$.

c. If the yaw axis is being tested, then $\Delta W = -\Delta W$.

d. If $WMIN \leq \Delta W \leq WMAX$, then the axis passed the test so go to step (g) to clear the test on this axis.

e. If ΔW outside the limits, $\Delta W < WMIN$ or $\Delta W > MAX$, then the axis has failed the test. PASWT shall set entry counter ECNT = 1 to test the axis again during the next cycle and increment WFCT, the wheel failure count. If WFCT is less then KPWTF$AC, PASWT shall return.

f. If WFCT reaches KPWTF$AC, the allowed failure limit, then

f.1 test for skew wheel available for switching wheels if RWAS >1 then set the wheel failure flag, FRWAF = 1 to indicate failure and no switching possible.

f.2 if RWAS $\leq$1 then turn skew on for replacing failed wheel and turn off the failed axis wheel.

These commands shall be issued via CMDPRO as specified in the CMDPRO Issuance Procedure (Paragraph 3.1.7).

g. Clear wheel test in progress flag (PWTIP = -1) of axis test.

h. Clear wheel failure count, WFCT = 0.

ACS Input/Output Variables

The ACS input/output requirements are shown in Figure 4.10.6-15 and defined as follows:

Symbol	Source	Description
MMUTAB (12)	MMUS	MMU CMD Table containing NCMD, MMUCMD (8), UC1, UC2, UC3
NCMD	MMUS	Number of commands in MMUTAB to be issued by ACS
MMUCMD (8)	MMUS	MMU Command Table
UC1, UC2, UC3	MMUS	Torque compensations due to MMU torques
FBUS	CMDPRO	Flag to indicate CPU on bus selection
QUW	ADS	Quad Use Word
QLW	ADS	Quad Lost Word for Search Table Use
WOR (3)	ADS	Orthogonal wheel speeds for YAW, ROLL and PITCH axes
AROLL	ADS	Roll
APITCH	ADS	Pitch EULER Error-Angle
AYAW	ADS	Yaw
WMAG (3)	ADS	Magnitude of wheel speeds for YAW, ROLL and PITCH axes
SMODE	ADS	Submode Definition Word
FMMUIN	ADS	MMUS execution inhibited flag
OMEGA (3)	ADS	Vector of Error Rates

Symbol	Source	Description
TORQUE CMDS	ADS	Control torque commands to RWA wheels
YINT	ADS	(Re-Initialized) Yaw Control Law Integral Term
COIL CMDS	ADS	Coil commands issued for bus selected
WFW	TIREX	RWA Status Array
RWAY, RWAR, RWAP, RWASK	TIREX	RWA Status Word
NULINP	ATMUL	Nitrogen Loading in Progress
ANTREQ (3)	ATMUL	Anticipating Torque Request
ANTREQ (3)	ATMUL	Anticipating Torque Commands
NULINP	ATMUL	Nitrogen Unloading in Progress Flag

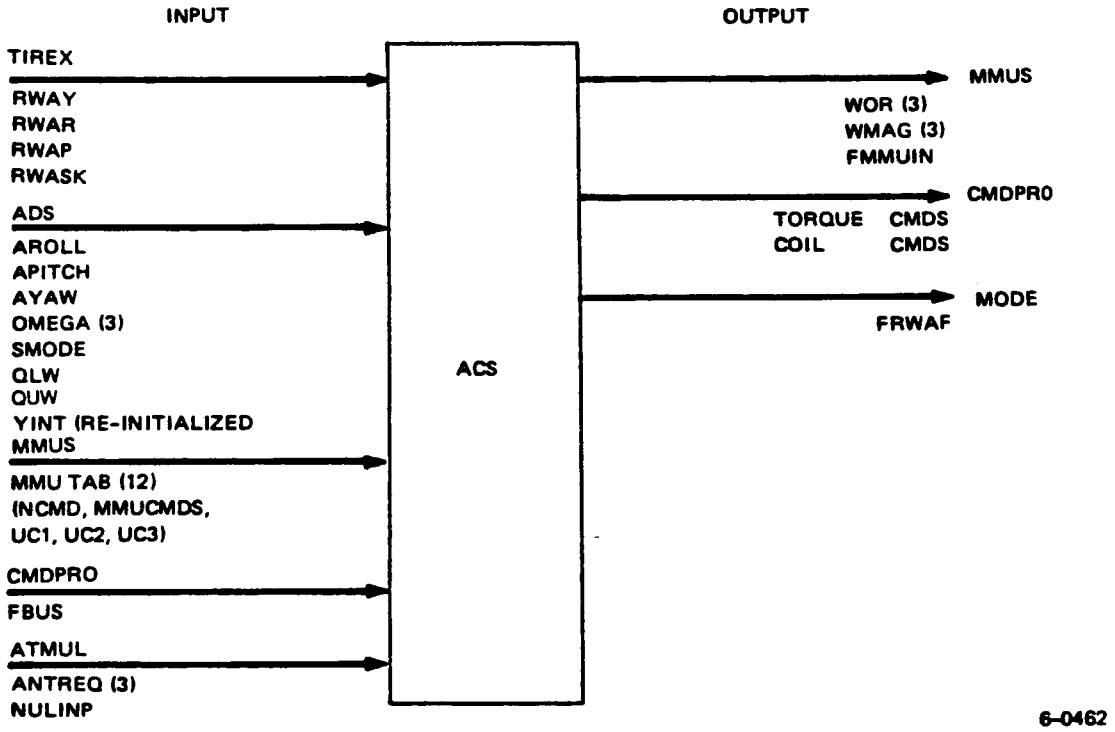

Figure 4.10.6-15. ACS Input/Output Requirements

ACS Telemetry Parameters

The ACS telemetry parameter requirements are as follows:

Symbol	Parameter
FATERR	Attitude Error Flag
CNT (3)	Attitude Error Count for Each Axis
WOR (3)	Equivalent axis RWA wheel speed
RWAS	RWA power status word term
YINT	Yaw control law integral term (unformatted)
RINT	Roll control law integral term (unformatted)
PINT	Pitch control law integral term (unformatted)
TCD (3) [Cx, Cy, Cz]	Axis torque commands (formatted)
TCD (3) [TCx, TCy, TCz]	Axis torque commands (unformatted)
WI	Wheel speed at start of test
PWTIP	Passive wheel test in progress plan
WF	Wheel speed at end of test
AWTIP	Active wheel test in progress
FMMUIN	MMU inhibit flag
WWH (4)	Wheel speeds for each wheel
PWTY	Request for yaw axis RWA passive wheel test
PWTR	Request for roll axis RWA passive wheel test
PWTP	Request for pitch axis RWA passive wheel test
NULINP	Nitrogen Unloading in Progress Flag

4.10.6.6 Magnetic Momentum Unloading Software (MMUS)

The Magnetic Momentum Unloading Software module (MMUS) is called as a subroutine once each 0.5 second computational cycle but is allowed to take as long as 4.0 seconds to complete its processing.

The MMUS module generates output to control the operation of the PTC and RYC air-core coils to unload the momentum buildup on the reaction wheels. MMUS determines from threshold conditions which coils need to be energized or de-energized, and selects a set of commands for ACS to issue to the CMDPRO module. MMUS also generates signals to allow ACS to compensate for the effect of the coil torque on satellite pointing.

On entry, MMUS examines conditions that inhibit MMUS from performing any of its functions. The conditions are as follows:

1. Check MMUS inhibit flag, FMMUIN.

   a) If FMMUIN was clear on the previous cycle and is set on the current cycle, MMUS performs a general coil turnoff.

   b) If FMMUIN is set, MMUS performs none of its functions.

2. Check number of commands, NCMD.

If NCMD is not equal to zero, MMUS performs none of its functions because ACS has not finished issuing the last MMUS commands.

3. Check for unloading regions (Figure 4.10.6-16)

   a) If $|SMAG| > SMPO$ then the satellite is in a Polar region. Where SMPO is equal to the polar unloading region boundary.

   b) If $SEWL \leq SMAG \leq SEWU$ then the satellite is in an East/West region. Where SEWL is the E/W unloading region lower boundary and SEWU is the E/W unloading region upper boundary.

   c) If the satellite is in none of the unloading regions then MMUS performs none of its functions.

Threshold determination computations shall be accurate to ± 0.006 in the units of SMAG.

MMUS determines from the RWA speed components which axes need to be unloaded or have been unloaded and initiates the commands to be formatted. MMUS also checks status of the coils to prevent redundant commands. The regional test criteria is specified in Table 4.10.6-5.

The polarity of the orthogonal set of RWA speed components, WOR (3), whose magnitudes are given by WMAG (3) is represented in the algebraic sign of WOR (3) as follows:

Component	Direction of Positive Reading in the P-Frame
WOR (0) (yaw)	- Xp
WOR (1) (roll)	+ Yp
WOR (2) (pitch)	+ Zp

MMUS does not initiate 'turn on' when it believes the corresponding coil is already on, nor does MMUS initiate 'turn off' when it believes the corresponding coil is already off. Threshold determination calculations shall be accurate to ± 0.1 counts.

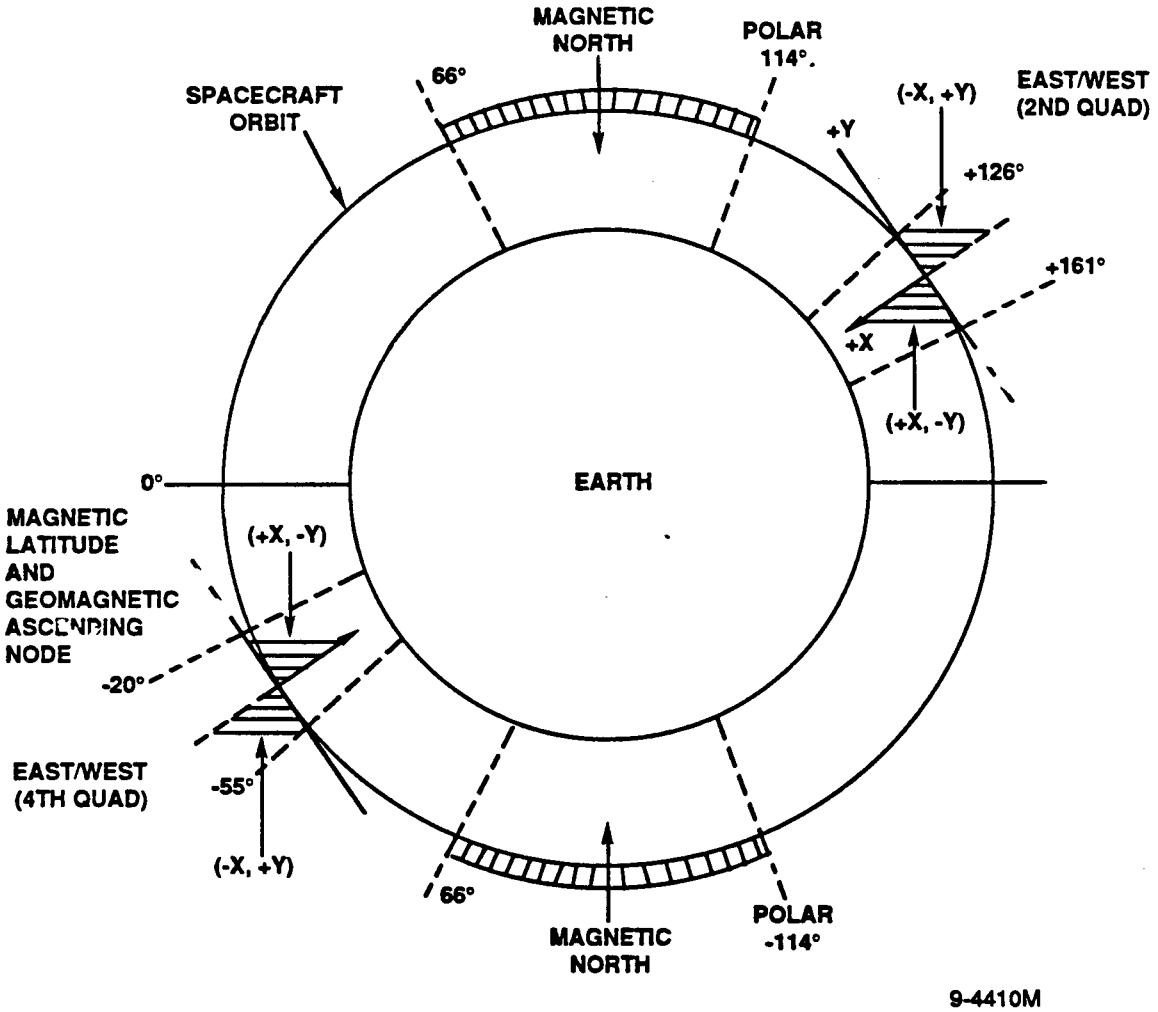

Figure 4.10.6-16. Momentum Polarity Criteria Spacecraft

TABLE 4.10.6-5. MMUS TURN ON/OFF CRITERIA

Region	Axis Unloaded	Coil	Turn On Conditions	Turn Off Conditions
EAST/WEST	YAW ROLL	RYC	WMAG(Y) > WTON(Y) WMAG(R) > WTON(R) YAWB = -1 WOR(Y) = + WOR(R) = +	WMAG(R) < WTOF(R)
EAST/WEST	YAW ROLL	RYC	WMAG(Y) > WTON(Y) WMAG(R) > WTON(R) YAWB = -1 WOR(Y) = - WOR(R) = -	WMAG(R) < WTOF(R)
POLAR	ROLL	RYC	WMAG(R) > WTON(R)	WMAG(R) < WTOF(R)
POLAR	PITCH	RYC	WMAG(P) > WTON(P)	WMAG(P) < WTOF(P)

TURN ON VALUES	TURN OFF VALUES
WTON(Y) = 200 RPM WTON(R) = 525 RPM WTON(P) = 775 RPM	WTOF(Y) = 175 RPM WTOF(R) = 500 RPM WTOF(P) = 750 RPM

Roll Axis (Polar Region)

Wheel Speed	Magnetic Pole (Sign of SMAG)	Dipole Polarity	CLSN
+	North (+)	-	0
-	North (+)	+	2
+	South (-)	+	2
-	South (-)	-	0

Pitch Axis (Polar Region)

Wheel Speed	Magnetic Pole (Sign of SMAG)	Dipole Polarity	CLSN
+	North (+)	+	2
-	North (+)	-	0
+	South (-)	-	0
-	South (-)	+	2

When MMUS has determined that a given axis is to be unloaded, MMUS determines the polarity of the required magnetic dipole from the corresponding coil in accordance with the following:

Yaw/Roll Axes (East/West Region)

YAWB	Polarity WOR(0)	WOR(1)	Quad 1 SMAG, + FASCDES=0	Quad 2 SMAG, + FASCDES=1	Quad 3 SMAG, - FASCDES=1	Quad 4 SMAG, - FASCDES=0
-1	+	+	No Unloading	-	No Unloading	+
-1	-	-	No Unloading	+	No Unloading	-
-1	-	+	-	No Unloading	+	No Unloading
-1	+	-	+	No Unloading	-	No Unloading

MMUS generates a set of three numbers MCOM (3) to facilitate ACS compensating for the torques exerted on the satellite when the coils are energized. MMUS contains a set of four constants MCOMP (4) representing the magnitude of the compensation offset. MMUS shall generate the terms MCOM(3) in two's complement form based on magnitude of MCMP and sign of WOR as shown in Table 4.10.6-6.

TABLE 4.10.6-6. COMPENSATION TERM TABLE

Region	Coil	Turn On/Off	Effected Compensation Term (Two's Complement)	Magnitude Term Used	Term Sign Same As
EAST/WEST	RYC	ON	MCOM (0)	MCOMP (0)	WOR (0)
EAST/WEST	RYC	ON	MCOM (1)	MCOMP (3)	WOR (1)
EAST/WEST	RYC	OFF	MCOM (0)	0	
EAST/WEST	RYCOFF	OFF	MCOM (1)	0	
POLAR	RYC	ON	MCOM (1)	MCOMP (1)	WOR (1)
POLAR	RYC	OFF	MCOM (1)	0	
POLAR	PTC	ON	MCOM (2)	MCOMP (2)	WOR (2)
POLAR	PTC	OFF	MCOM (2)	0	

MMUS assembles coil control commands in the format required by CMDPRO and passes these commands to ACS for recognition and further passing to CMDPRO for execution. MMUS provides for passing up to four commands at one time. Coil commands are inverted pulse discretes. However, MMUS only generates the 'on' portion of the pulse. ACS generates the 'off' portion of the pulse.

MMUS maintains a record of the number (0 to 4) of commands to be passed. When it is clear that all commands to be assembled on a given cycle have been assembled, and all changes to compensation signals MCOM have been completed, then MMUS enables ACS to accept the commands and compensation signals by transferring the number of commands to the location NCMD.

MMUS arranges the formatted commands, compensation terms and number of commands in the output table MMUCMD as defined in Table 4.10.6-7.

Each coil is addressable via either I/O bus A or I/O bus B of the CIU. MMUS addresses all coil commands to the appropriate CIU buffers on both I/O bus A and I/O bus B. There is a total of four buffers in the CIU which interface with the coils. ACS determines which commands to issue for the selected bus.

Upon determining that a particular coil is to be turned on with a particular polarity, MMUS assembles two commands. Each of these commands is formatted to simultaneously energize both the 'on' and '+' or '-' bits associated with that coil. One of these commands is addressed to the coil via each CIU bus.

TABLE 4.10.6-7. MMUS OUTPUT FORMAT

[MMUCMD (12)]				
MMUTAB Index	Alternate Symbol	No. 1 WD. Elements	Meaning	
0	NCMD	2	NUMBER OF CMDS TO BE EXECUTED IN ORDER 4, 3, 2, 1.	
1	MMUCMD (1)	2	OPCODE AND BUFFER ADD.	COMMAND 1
2	MMUCMD (1)	2	'AND' AND 'XOR' WORDS	
3	MMUCMD (2)	2	OPCODE AND BUFFER ADD.	COMMAND 2
4	MMUCMD (2)	2	'AND' AND 'XOR' WORDS	
5	MMUCMD (3)	2	OPCODE AND BUFFER ADD.	COMMAND 3
6	MMUCMD (3)	2	'AND' AND 'XOR' WORDS	
7	MMUCMD (4)	2	OPCODE AND BUFFER ADD.	COMMAND 4
8	MMUCMD (4)	2	'AND' AND 'XOR' WORDS	
9	MCOM (0) or UC1	2	X_P (YAW)	
10	MCOM (1) or UC2	2	Y_P (ROLL)	AXIS COMPENSATION SIGNALS
11	MCOM (2) or UC3	2	Z_P (PITCH)	

Upon determining that a particular coil is to be turned off, MMUS assembles two commands. Each of these commands is formatted to energize the 'off' bit associated with that coil. One of these commands is addressed to the coil via each CIU bus.

MMUS provides for a general turnoff, to be accomplished by assembling a set of 4 commands, one for each of the CIU buffers interfacing with the coils. Each of these commands is formatted to simultaneously energize the 'off' bits associated with both coils addressable via each CIU buffer.

MMUS performs a general turn off upon leaving an unloading region when FCLTS = set. MMUS does not repeat the general turnoff, until entering and again leaving an unloading region, unless general turnoff is required for other reasons as specified below. Upon assembling a general turnoff, MMUS clears all components of MCOM to zero, and also clears the turn-off flag, FCLTS = clear.

MMUS shall use the coil pair code, CLPR, to determine whether the primary or backup coil is being used for unloading momentum on the axes.

MMUS test the performance of the unloading system by checking the wheel speeds for each axis. MMUS switches coil pairs when the wheel speeds for an axis do not respond to unloading attempts on that axis, and switching is not inhibited from the ground.

The flags FPTCB and FRYCB can be set by ground command to inhibit automatic switching of the pitch and roll/yaw coils respectively.

MMUS does not repeat the coil test until entering and again leaving an unloading region.

MMUS maintains an index, CLPR, to identify which coil pair is being used (RYC-1, PTC-2, or RYC-2, PTC-1) and directs all turn on commands and all individual turn off commands to the appropriate member of the set.

MMUS Input/Output Parameters

The MMUS input/output requirements are shown in Figure 4.10.6-17 and defined as follows:

Symbol	Source	Description
FMMUIN	ACS	MMUS inhibit flag
NCMD	MMUS/ACS	Number of MMUS commands set by MMUS cleared by ACS
WOR (3)	ACS	Orthogonal Wheel Speeds
WMAG (3)	ACS	Magnitude of Orthogonal Wheel Speeds
SMAG	GEODAT	Sine of magnetic latitude
FASCDES	GEODAT	Ascending/Descending flag

Symbol	Source	Description
MMUCMD	MMUS	MMU Command Table Formatted for I/O buses A and B contains number of commands, MMU commands, MMU compensations
FPTCB	GROUND	PTC switch to backup inhibit flag
FRYCB	GROUND	RYC switch to backup inhibit flag

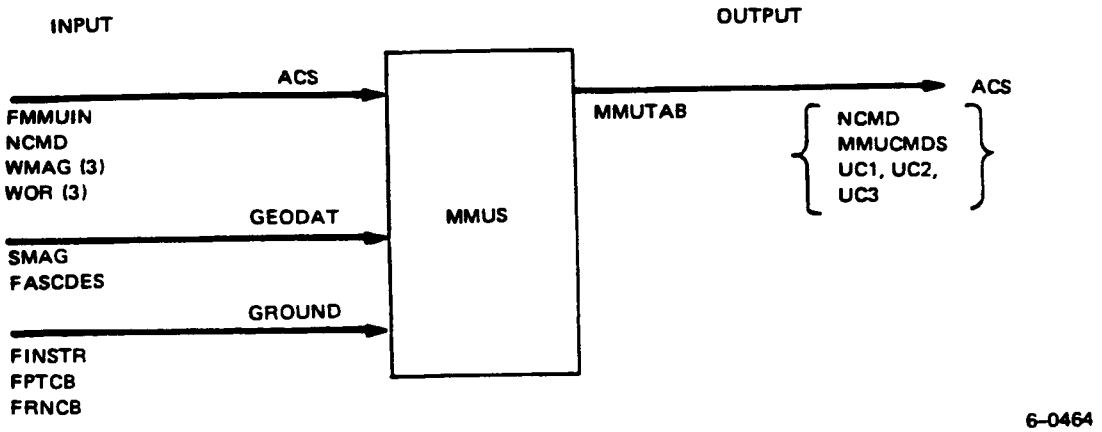

Figure 4.10.6-17. MMUS Input/Output Requirements

MMUS Telemetry Parameters

The MMUS telemetry parameter requirements are as follows:

Symbol	Parameter
FMMUIN	1: = Inhibit MMU Functions
CLTST	0: = No Test, 1: = Test Coils
CLPR	0: = RYC-1, PTC-2, 1:RYC-2, PTC-1

4.10.6.7 Solar Array Drive Control Software (SADCS)

Solar Array Drive Control Software module is called as a subroutine once each 0.5 second computational cycle but is allowed to take as long as 40 seconds to complete its processing.

The SADCS module generates an output to command the Array Drive Electronics (ADE) which in turn provides the drive signals for the Solar Array Drive (SAD).

SADCS monitors the array position relative to the sun line and maintains the array position to within 5° of the sun line by commanding different rates based on the error.

The SAD status word, SADSTATI, contains position and status data. The lower weight bits represent the SAD position and are saved as ANGLE$SA.

The upper eight bits represent the SAD power status, speed and direction. It is saved as STAT$SA.

The reported status is checked for agreement with the expected status. The expected status is predicted from the previous command issued to the ADE. The relation between the status and the commanded mode is shown in Table 4.10.6-8.

If the status and the previous command do not agree, SADCS increments an error counter.

On the seventh consecutive failure, SADCS:

1. Clears the error counter
2. Sets the error flag (FERRNC) to 1

If the error count is 6 or less then SADCS operates on the complement flag (FCOMP$SA) as follows:

1. If FCOMP$SA is set, then clear it.
2. If FCOMP$SA is clear, then set it.

If the status and the previous command agree, SADCS clears the error count and does not change the value of FCOMP$SA.

TABLE 4.10.6-8. ADE STATUS WORD AND SAD MODES

Status Word	Speed	Direction
1 1 0 0	Slow	Reverse
1 2 0 0	Normal	Reverse
1 4 0 0	Fast	Reverse
1 8 0 0	Slew	Reverse
0 1 0 0	Slow	Forward
0 2 0 0	Normal	Forward
0 4 0 0	Fast	Forward
0 8 0 0	Slew	Forward

SADCS computes the error angle, in π-scaled form, as the difference between the corrected SAD position and the SUN position in array coordinates.

error angle = ANGLE$SA + HRWBIAS - SOLANG

This computation is performed by first converting the SAD position to π-scaled form. The hardware bias (HRWBIAS) and the sun angle (SOLANG) will be in that form.

The error angle (ERANG$SA) is converted to a signed integer which represents the error in slots.

The command to be issued to the ADE is based on the error (ERANG) and the status as represented by the complement flag (FCOMP).

The speed and direction commands are as specified in Table 4.10.6-9.

The command regime is divided into two sections: array previously in slew and array not in slew on previous command cycle.

Once the array has been commanded into slew speed it continues to be commanded into slew, until the absolute error is less than two slots.

If the SAD command on the previous cycle was not slew then the command shall be determined from the sign and magnitude of the error.

When the array is placed in the slew mode a test is initiated to test for a positive error closure rate. This consists of the following steps:

1. Record value of |ERANG$SA|

2. Wait 20 seconds and compare present value of |ERANG$SA| to that recorded in Step 1.

3. If the absolute value of the error has not decreased set FERRNC to 1.

This test shall be repeated until the array is commanded out of the slew mode. If the array is commanded out of slew mode before the 20 seconds have elapsed, the test shall be terminated.

The command is formed in accordance with Table 4.10.6-10, based on the desired rate and the use of the complement or swap function.

The use of the complemented form (swap bit set) allows the system to accommodate stuck hardware bits. Complementing is controlled by the two flags FCOMP$SA and FSADC.

The command will be complemented if and only if FCOMP$SA is set and FSADC is clear. FSADC is under control of the ground controller, and is used to inhibit complementing.

TABLE 4.10.6-9. SAD DIRECTION AND SPEED COMMANDS AS A FUNCTION OF ERROR

A. Array in Slew Mode on Previous Cycle		
Error	Command	
Mag	≥2	<2
Sign		
+	Slew Reverse	Fast Reverse
-	Slew Forward	Slow Reverse

B. Array not in Slew on Previous Cycle			
Error	Command		
Mag	0,1	2 - 5	>5
Sign			
+	NC	Fast Reverse	Slew Reverse
-	NC	Slow Reverse	Slew Forward

NC: = No change from previous command.

TABLE 4.10.6-10. SAD COMMAND WORD

	Formatted Command			
	Forward Direction		Reverse Direction	
Speed	Normal	Complement	Normal	Complement
Slew	0080	0070	0000	00F0
Slow	00A0	0050	0020	00D0
Fast	00C0	0030	0040	00B0
Normal	00E0	0010	0060	0090

SADCS calls CMDPRO to actually output the command to the ADE. A command is issued on every entry to SADCS. This includes those cases where the command has not changed from the last entry.

SADCS monitors the state of the hardware liftoff flag in buffer 149. If this flag is clear, indicating operation prior to liftoff, SADCS calls subroutine SADTEST to provide test input data.

SADCS Input/Output Parameters

The SADCS input/output requirements are shown in Figure 4.10.6-18 and defined as follows:

Symbol	Source	Description
PREV	SADCS	Last cycle command rate bit configuration
SADSTATI	CIU/ADE	SAD status word
ANGLE	CIU/SAD	Angle position of SAD
FERRNC	SADCS	Electronic error not correcting flag
CMAND	SADCS	SAD command
SOLANG	GEODAT	Relative position of sun to spacecraft

SADCS Telemetry Parameters

The SADCS telemetry parameter requirements are as follows:

Symbol	Parameter
ANGLE	SAD angle input from SAD
CMAND	SAD command rate to ADE

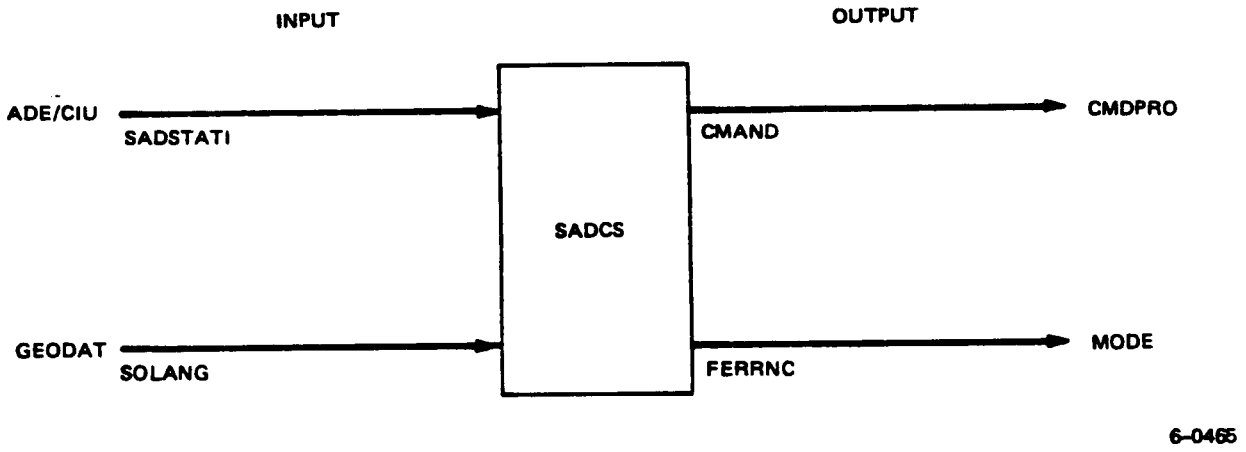

Figure 4.10.6-18. SADCS Input/Output Requirements

4.10.6.8 Geometric Data Software (GEODAT)

The Geometric Data Software:

(a) Computes the sine of the spacecraft orbit anomaly (SINB) and the orbit rate (ORBIT).

(b) Computes the solar array drive reference angle (SOLANG).

(c) Computes a yaw update (NEWPSI) once per orbit and furnishes a flag (FYAWUP) to indicate when this update is available.

(d) Provides a sun/moon warning word (SMWARN), which indicates which quadrants of the Earth Sensor Assembly (ESA) will encounter sun/moon interference.

(e) Computes the sine of the magnetic latitude (SMAG) and furnishes a flag (FASCDES) to indicate whether the spacecraft is on the ascending or descending side of its orbit.

(f) Computes the spacecraft altitude above the Earth's surface (ALTITUD).

GEODAT is called as a subroutine during each 0.5 second processing cycle and generates its outputs on each call with a minimum reliance on the results of previous calls. It operates on Level 5 and runs in both the primary and backup CPUs continuously. GEODAT is called by MODE after all other ADACS modules that use GEODAT outputs have been called. Thus GEODAT shall complete its functions for use by ADACS modules on the next processing cycle.

Ephemeris Servicing

GEODAT requires a set of basic parameters which are uplinked at least once per week (see Table 4.10.6-11).

Two tables of these parameters are stored in the on-board computer simultaneously, with one table available for GEODAT's current use and the other table available for uplink of a new parameter set. Upon command, GEODAT moves in the new table.

GEODAT shall never modify the contents of this table.

At the same time, GEODAT initiates an update to the Ephemeris Clock (GDTIME) maintained by the TIREX software module. This is achieved by adding the value of GDCKU$GE, found in the new parameter table, to GDTIME. There is no provision for clock word overflow because the available dynamic range in GDTIME is considerably longer than the time between Ephemeris Loads. It should also be noted that the value of GDCKU$GE is in fact a negative number which, when added to GDTIME, resets the clock to a small (or even negative) value.

GEODAT computes

DELT = GDTIME - TEPOC + 0.5 seconds

where

GDTIME = the current spacecraft clock time

TEPOC = Epoch Time of GDITAB

TABLE 4.10.6-11. UPLINKED INPUTS TO GEODAT

Symbol	GEODAT Local SPL Tag	Description	Type	Scaling	Units	Nominal Magnitude
Δt_{ck}	GDCKU$GE	Increment for Ephemeris Clock @ Epoch	DP	+21	Seconds	-2^{21}
t_o	TEPOC$GE	Epoch Time	DP	+21	Seconds	-0
RAG_o	RAGZ$GE	Right Ascension of Greenwich @ Epoch	DP	+0	π Radians	$-\pi$ to $-\pi$
R_{sc}	RMNSC$GE	Mean Radius (Semimajor Axis) of S/C Orbit	DP	+13	km	7200-7300
$e_{10,sc}$	EC1Z$GE	Eccentricity (1st harmonic) of S/C Orbit @ Epoch	DP	+0	Non-Dim	0 to -.006
$\dot{e}_{1,sc}$	EC1D$GE	First Derivative of Eccentricity (1st harmonic) of S/C Orbit	DP	-21	1/sec	-10^{-8} to $+10^{-8}$
$\omega_{10,sc}$	W1ZSC$CE	S/C argument of perigee (1st harmonic) @ Epoch	DP	+0	π Radians	$-\pi$ to $+\pi$
$\dot{\omega}_{1,sc}$	W1DSC$GE	First derivative of S/C argument of perigee (1st harmonic)	DP	-18	π Radians/sec	-10^{-5} π/sec to $+10^{-5}$ π/sec
$e_{20,sc}$	EC2Z$GE	Eccentricity (2nd harmonic) of S/C Orbit @ Epoch	DP	-9	Non-Dim	<.001
$\dot{e}_{2,sc}$	EC2D$GE	First derivative of eccentricity (2nd harmonic) of S/C Orbit	DP	-30	1/sec	-10^{-10} to $+10^{-10}$
$\omega_{20,sc}$	W2ZSC$GE	S/C argument of perigee (2nd harmonic) @ Epoch	DP	+0	π Radians	$-\pi$ to $+\pi$
$\dot{\omega}_{2,sc}$	W2DSC$GE	First derivative of S/C argument of perigee (2nd harmonic)	DP	-19	π Radians/sec	-10^{-6} π/sec to $+10^{-6}$ π/sec
i_{sc}	INSC$GE	Inclination of S/C Orbit	DP	+0	π Radians	.5483 π (98.7°)
$\Omega_{o,sc}$	OMZSC$GE	Longitude of Ascending Node, S/C, at Epoch	DP	+0	π Radians	$-\pi$ to $+\pi$
$\dot{\Omega}_{sc}$	OMDSC$GE	Rate of Longitude of Ascending Node, S/C	DP	-21	π Radians/sec	-6×10^{-8} π/sec
$M_{o,sc}$	MZSC$GE	Mean Anomaly of S/C @ Epoch	DP	+0	π Radians	$-\pi$ to $+\pi$
n_{sc}	NSC$GE	Mean Motion of S/C @ Epoch	DP	-11	π Radians/sec	-3.3×10^{-4} π/sec
$\frac{\dot{n}}{2}_{sc}$	NDSC$GE	First Derivative of S/C Mean Motion	DP	-34	π Radians/sec^2	-10^{-11} π/sec^2 to $+10^{-11}$ π/sec^2
$\frac{\ddot{n}}{6}_{sc}$	NDDS$GE	Second Derivative of S/C Mean Motion	DP	-55	π Radians/sec^3	-10^{-17} π/sec^3 to $+10^{-17}$ π/sec^3
$\vec{S}_o$	SZX$GE SZY$GE SZZ$GE	Sun Position Unit Vector @ Epoch (Inertial Frame)	DP	+1	Non-Dim	-1 to +1 for each component
$\dot{\vec{S}}$	SDX$GE SDY$GE SDZ$GE	Sun Vector Rate	DP	-16	1/sec	-10^{-5} to $+10^{-5}$
η_o	ETAZ$GE	Sun Cone Angle @ Epoch	DP	+0	π Radians	$-\pi$ to $-\pi$
$\dot{\eta}$	ETAD$GE	Sun Cone Angle Rate	DP	-20	π Radians/sec	-10^{-6} π/sec to $+10^{-6}$ π/sec
i_M	INM$GE	Inclination of Moon Orbit (Inertial Frame)	DP	+0	π Radians	-.161 π to +.161 π
Ω_M	OMM$GE	Longitude of Moon Orbit Ascending Node @ Epoch	DP	+0	π Radians	$-\pi$ to $+\pi$
$M_{o,M}$	MZM$GE	Mean Anomaly of Moon @ Epoch	DP	+0	π Radians	$-\pi$ to $+\pi$
n_M	NM$GE	Mean Motion of the Moon	DP	-19	π Radians/sec	8×10^{-7} π/sec
$\frac{\dot{n}}{2}_M$	NDM$GE	First Derivative of Moon Mean Motion	DP	-40	π Radians/sec^2	-10^{-11} π/sec to $+10^{-11}$ π/sec

Note that 0.5 seconds is added because GEODAT is called after all the other ADACS modules which utilize the GEODAT outputs; thus, GEODAT must compute its results for ADAC's use during the next processing cycle.

Current Ephemeris Parameter (CEP) Computations

The ephemeris table contains the parameters from which the basic ephemeris information is constructed as a function of DELT. Before continuing, however, one should note that the parameters of the ephemeris table bear names which have definite connotations in the astronautics literature. The implementation of these terms in this document is for convenience only; the actual value of an uplinked parameter will not necessarily be precisely the same as that dictated by the classical meaning of the term. In effect, the table parameters are estimates of their scientifically-defined counterparts, ie., estimates which have been scientifically modified for GEODAT's needs and which (when implemented in GEODAT's algorithms) will yield results of sufficient accuracy to meet ADAC's requirements.

Current Spacecraft Orbit Parameters

Six Keplerian elements for the spacecraft are obtained by GEODAT:

(a) R_{sc}, the semi-major axis of the spacecraft orbit, obtained directly from the ephemeris table and does not vary with Δt.

(b) $el_{,sc}$, the eccentricity of the spacecraft orbit, is obtained directly from the ephemeris table and does not vary with Δt.

(c) i_{sc}, the inclination of the spacecraft orbit, obtained directly from the ephemeris table and does not vary with Δt.

(d) Ω_{sc}, the current longitude of ascending node of the spacecraft orbit, is obtained by:

$$\Omega_{sc} = \Omega_{o,sc} + \dot{\Omega}_{sc}\,\Delta t$$

where

$\Omega_{o,sc}$ = the longitude of ascending node of the spacecraft at Epoch.

$\dot{\Omega}_{sc}$ = the rate of the longitude of the ascending node.

Both $\Omega_{o,sc}$ and Ω_{sc} are obtained from the ephemeris table.

(e) $\omega_{1,sc}$, the current argument of perigee of the spacecraft orbit, is obtained by:

$$\Omega_{sc} = \omega_{o,sc} + \dot{\omega}_{sc}\,\Delta t$$

where

$\omega_{10,sc}$ = the argument of perigee of the spacecraft at Epoch.

$\dot{\omega}_{1,sc}$ = the rate of argument of perigee.

Both $\omega_{10,sc}$ and $\dot{\omega}_{1,sc}$ are obtained from the ephemeris table.

(f) M_{sc}, the current mean anomaly of the spacecraft, is obtained by:

$$M_{sc} = M_o, sc + \Delta t \quad n_{sc} + \Delta t \quad \frac{\dot{n}}{2}_{sc} + \frac{\ddot{n}}{6}_{sc} \Delta t$$

where

$M_{o,sc}$ = the mean anomaly of the spacecraft at Epoch.

n_{sc} = the mean motion of the spacecraft.

$\frac{\dot{n}}{2}_{sc}$ = first derivative of the mean motion.

$\frac{\ddot{n}}{6}_{sc}$ = second derivative of the mean motion.

M_o,sc, n_{sc}, $\frac{\dot{n}}{2}_{sc}$; and $\frac{\ddot{n}}{6}_{sc}$ are obtained from the ephemeris table.

Current Sun Parameters

The nominal current sun vector is constructed by:

$$\vec{S} = \vec{S}_o + \dot{\vec{S}} Wt$$

where

$\vec{S}_o$ = the sun vector at Epoch.

$\dot{\vec{S}}$ = the sun vector rate.

Both $\vec{S}_o$ and $\dot{\vec{S}}$ are obtained from the ephemeris table.

The two fundamental sun-orientation angles required by ADACS are the sun cone angle and the sun clock angle (see Figures 4.10.6-19 and 4.10.6-20).

The sun clock (also referred to as the solar array drive angle) is obtained from the current nominal sun vector (see below). However, the sun cone angle (ETAP) is obtained by:

$$ETAP = \eta_o + \dot{\eta} \Delta t$$

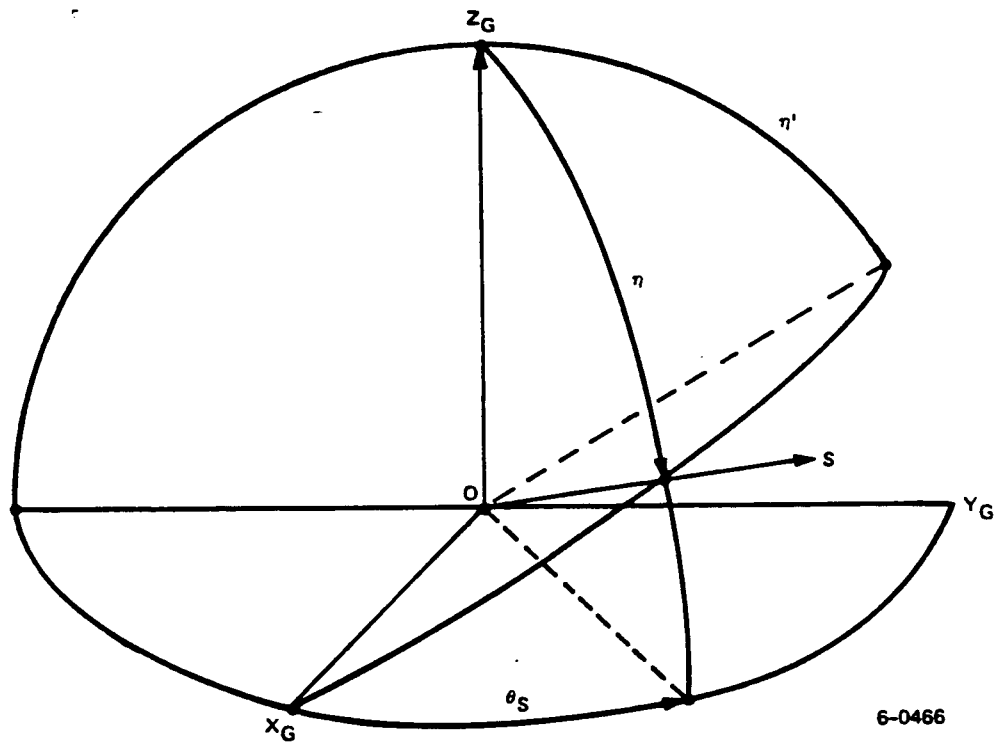

Figure 4.10.6-19. Sun Cone and Clock Angles

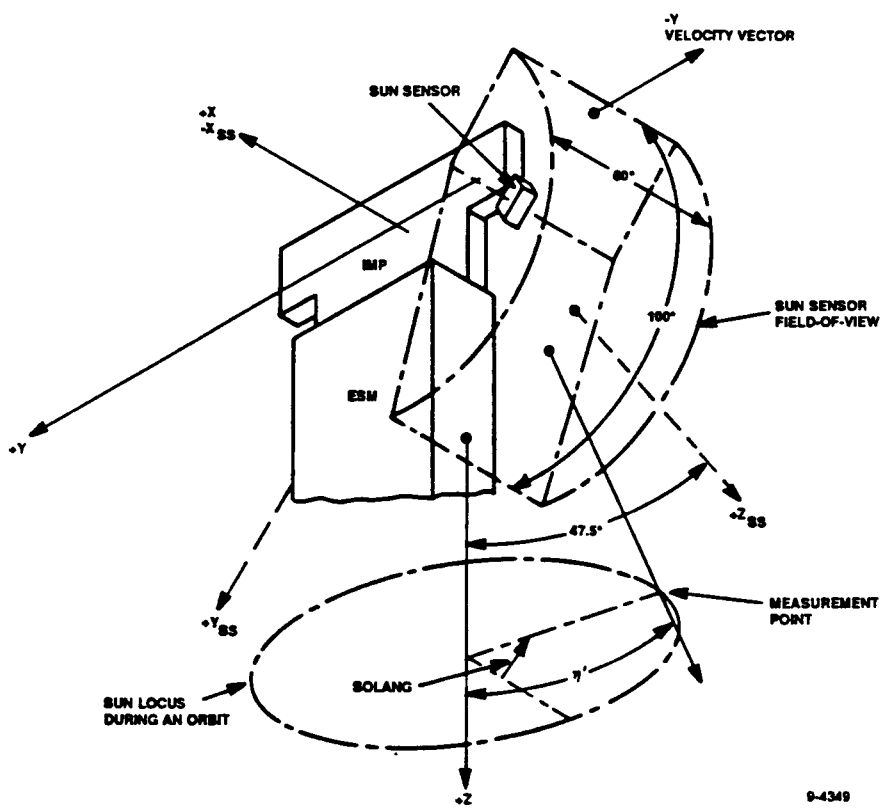

Figure 4.10.6-20. Sun Sensor Geometry

η_o = sun cone angle at Epoch.

$\dot{\eta}$ = rate of sun cone angle.

η_o and $\dot{\eta}$ are obtained from the ephemeris table.

Current Moon Parameters

The eccentricity of the Moon's orbit is sufficiently small to have a negligible effect on parallax corrections. Therefore, in Keplerian terms, the elements of the Moon's orbit are:

(a) R_M, the mean earth-moon distance, is a program constant (See Table 4.10.6-12).

(b) e_M, the eccentricity, is set equal to zero.

(c) i_M, the inclination of the Moon's orbit with respect to the Earth, is obtained directly from the ephemeris table.

(d) Ω_M, the longitude of the Moon's ascending node, is obtained from the ephemeris table.

(e) ω_M, the Moon's argument of perigee, is set equal to zero.

(f) M_M, the mean anomaly of the Moon, is obtained as:

$$M_M = M_{o,M} + \Delta t \quad n_m + \frac{\dot{n}}{2} M \Delta t$$

where

$M_{o,M}$ = mean anomaly of the Moon at Epoch.

n_M = mean motion of the moon.

$\frac{\dot{n}}{2}_M$ = first derivative of the mean motion.

M_o, M, n_M and $\frac{\dot{n}}{2}_M$ are obtained from the ephemeris table.

Current Magnetic Dipole Parameters

The current Right Ascension of Greenwich constructed by:

$$RAG = RAGo + \omega_e \Delta t$$

where

RAGo = Right Ascension of Greenwich at Epoch.
ω_e = Earth rotation rate.
RAGo shall be obtained from the ephemeris table.
ω_e shall be a program constant.

TABLE 4.10.6-12. GEODAT PROGRAM CONSTANTS

Symbol	SPL Tag	Description	Scaling	Type	Units	Nominal Magnitude
R_M	RMNM	Moon Earth - Moon Distance		DP	km	384,400
B_D	BETAD	Cant Angle of the Earth's Magnetic Dipole	+1	DP	πRadians	0.6333 π (11.4°)
λ_D	LAMBDAD	Longitude of ascending mode of earth's magnetic dipole, referred to Greenwich	+1	DP	πRadians	0.11056 π (19.9°)
	SALW	Lower limit of sun clock angle window	+1	DP	πRadians	1.49444 π (269°)
	SAHG	Upper limit of sun clock angle window	+1	DP	πRadians	1.50556 π (271°)
b_E		Earth's polar radius	+13	DP	km	6356.7598
$e_E{}^2$		Earth's eccentricity squared	-3	DP	Non-Dim	0.0066945419
COS T_S		Sun interference window	0	DP	Non-Dim	COS 12.1° = 977783
COS T_M		Moon interference window	0	DP	Non-Dim	COS 10.0° = 984808

Spacecraft Frame (S Frame)

The X_S, Y_S and Z_S axes of the Spacecraft Frame are a mutually-perpendicular right-hand triad. These axes will be nominally controlled to coincide with the corresponding axes of the Geodetic Frame and thus this document treats the G Frame and the S Frame as being identical.

Construction of the T_{GI} Matrix (CTGI). The transformation from inertial (I Frame) to geodetic (G Frame) coordinates shall be accomplished with the T_{GI} matrix (see Boxes 1, 2, and 3). This matrix shall be generated as a procedure which entails the three rotations expressed in Box 3. For this purpose, this procedure shall utilize appropriate calls of the coordinate rotation library function (FROT).

The first two angles of rotation, Ω_{sc} and i_{sc}, shall be available from the CEP submodule of GEODAT.

For the purposes of GEODAT, there is a negligible difference between the orbit anomaly (the in-orbit angle) and the argument of latitude. This common quantity, β_{sc}, shall be obtained by the procedure:

$$v_{sc} = M_{sc} = 2\ e_{sc}\ \text{Sin}\ M_{sc}\ \text{(= true anomaly of spacecraft)}$$

$$\beta_{sc} = v_{sc} = \omega_{sc}$$

where

M_{sc}, e_{sc} and ω_{sc} shall be available from CEP.

Thus, the final angle of rotation in the T_{GI} matrix shall be the value of $\beta_{sc} + \pi$ (see Box 3).

Box 1

Inertial Frame (I Frame)

The I Frame referred to in this document is defined such that the mean equinox at Epoch lies along the + X_I axis. The Z_I axis is normal to the mean equator of the same Epoch and is nominally in the direction of the north celestial pole. The Y_I axis lies in the plane of the mean equator of the same Epoch and is mutually perpendicular to the X_I and Z_I axes and completes a right-hand triad.

Box 2

Geodetic Frame (G Frame)

The G Frame referred to in this document is defined such that the X_G axis is a line through the spacecraft payload, normal to the earth facing side from the spacecraft, with the positive sense being directed toward the earth.

The Z_G axis shall be normal to the orbit plane, positive in the direction of $\vec{r}_{sc} \cdot \vec{V}_{sc}$, where $\vec{r}_{sc}$ is the radius vector from the earth center to the spacecraft and $\vec{V}sc$ is the spacecraft velocity vector.

The Y_G axis shall be mutually perpendicular to the X_G and Z_G axes and completes a right-hand triad.

The origin of the G Frame shall be located at the center of mass of the spacecraft.

Box 3

Transformation from the I Frame to the G Frame (The T_{IG} Matrix)

The transformation of vectors from the I Frame to the G Frame shall be accomplished with the T_{IG} matrix. The latter shall be generated by a series of rotations (see Figure 4.10.6-21):

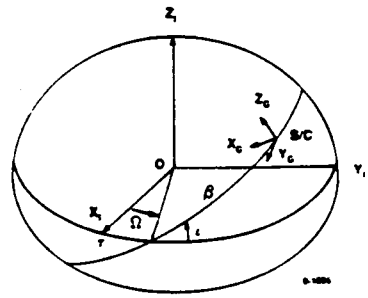

Figure 4.10.6-21. Transformation from the I Frame to the G Frame

(a) Rotation about the Z_I axis by the angle Ω_{sc}. Ω_{sc} is the longitude of the ascending node of the spacecraft orbit.

$$\begin{matrix} X_1 \\ Y_1 \\ Z_1 \end{matrix} = \begin{matrix} \cos\Omega_{sc} & \sin\Omega_{sc} & 0 \\ -\sin\Omega_{sc} & \cos\Omega_{sc} & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X_I \\ Y_I \\ Z_I \end{matrix}$$

(b) Rotation about the X_1 axis by the angle i_{sc}, the inclination of the spacecraft orbit.

$$\begin{matrix} X_2 \\ Y_2 \\ Z_2 \end{matrix} = \begin{matrix} 1 & 0 & 0 \\ 0 & \cos i_{sc} & \sin i_{sc} \\ 0 & -\sin i_{sc} & \cos i_{sc} \end{matrix} \begin{matrix} X_1 \\ Y_1 \\ Z_1 \end{matrix}$$

(c) Rotation about the Z_2 by the angle β_{sc}, the spacecraft argument of latitude (in-orbit anomaly).

$$\begin{matrix} X_3 \\ Y_3 \\ Z_3 \end{matrix} = \begin{matrix} \cos\beta_{sc} & \sin\beta_{sc} & 0 \\ -\sin\beta_{sc} & \cos\beta_{sc} & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X_2 \\ Y_2 \\ Z_2 \end{matrix}$$

(d) A change of parity to conform with the definition of the G Frame (see Paragraph A.2 of this document). This entails a rotation about the Z_3 by π radians to change the sense of the X and Y coordinates.

$$\begin{matrix} X_G \\ Y_G \\ Z_G \end{matrix} = \begin{matrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X_3 \\ Y_3 \\ Z_3 \end{matrix}$$

Since the Z_3 axis is identical to the Z_2 axis, this final rotation shall be incorporated by GEODAT into the preceding rotation:

$$\begin{matrix} X_G \\ Y_G \\ Z_G \end{matrix} = \begin{matrix} \cos(\beta_{sc}+\pi) & \sin(\beta_{sc}+\pi) & 0 \\ -\sin(\beta_{sc}+\pi) & \cos(\beta_{sc}+\pi) & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X_2 \\ Y_2 \\ Z_2 \end{matrix}$$

Construction of the T_{ID} Matrix (CTID). The transformation from dipole (D FRAME) to inertial (I Frame) coordinates shall be accomplished with the T_{ID} matrix (see Boxes 1, 4, and 5). This matrix shall be generated as a procedure which entails the two rotations expressed in Box 5. For this purpose, this procedure shall utilise appropriate calls of the coordinate rotation library function (FROT).

The rotation angles of β_D and λ_D (see Box 5) shall be software constants.

The rotation angle Ω_D is equal to λ_D plus the current Right Ascension of Greenwich (RAG) as computed in GEODAT.

Box 4

Earth's Magnetic Dipole Frame (D Frame)

The D Frame referred to in this document is defined such that the positive Z_D axis is aligned along the direction of the Earth's north magnetic pole.

The X_D axis lies along the intersection of the Earth's geographic and magnetic equatorial planes, with the positive direction toward the ascending node of the magnetic equator. The position of the ascending node is the sum of an initial longitude relative to the Prime Meridian at Greenwich, plus the Right Ascension of Greenwich (RAG) at Epoch time, plus the elapsed angle of earth rotation occurring since Epoch.

The Y_D axis is mutually perpendicular to the X_D and Z_D axes and completes a right-hand triad.

Box 5

Transformation from the D Frame to the I Frame (The T_{ID} Matrix)

The Earth's magnetic field shall be represented as a dipole canted at an angle β_D to the Earth's geographic polar axis.

The transformation of vectors from the D Frame to the I Frame shall be accomplished with the T_{ID} matrix. The latter shall be generated by a series of rotations (see Figure 4.10.6-22).

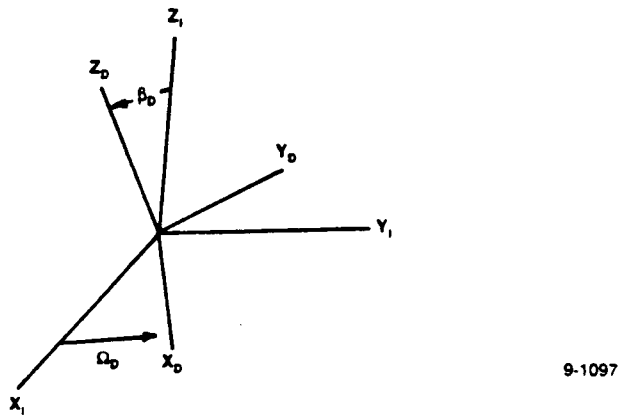

Figure 4.10.6-22. Transformation from the D Frame to the I Frame

(a) Rotation about the X_D axis by the angle $-\beta_D$

$$\begin{matrix} X' \\ Y' \\ Z' \end{matrix} = \begin{matrix} 1 & 0 & 0 \\ 0 & \cos\beta_D & -\sin\beta_D \\ 0 & \sin\beta_D & \cos\beta_D \end{matrix} \begin{matrix} X_D \\ Y_D \\ Z_D \end{matrix}$$

(b) Rotation about the Z' axis by the angle $-\Omega_D$, where $\lambda_D = W_D + RAG$ and RAG = current Right Ascension of Greenwich

$$\begin{matrix} X_I \\ Y_I \\ Z_I \end{matrix} = \begin{matrix} \cos\Omega_D & -\sin\Omega_D & 0 \\ \sin\Omega_D & \mathrm{COS}\,\Omega_D & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X' \\ Y' \\ Z' \end{matrix}$$

Construction of the T_{IM} Matrix (CTIM). The transformation from the Moon Frame (M Frame) to the I Frame shall be accomplished with the T_{IM} matrix (see Boxes 1, 6, and 7). This matrix shall be generated as a procedure which entail the three rotations expressed in Box 7. For this purpose, this procedure shall utilize appropriate calls of the coordinate rotation library function (FROT).

The rotation angles Ω_M, i_M and β_M ($=M_M$) shall be available from CEP.

Box 6
Moon Frame

The Moon Frame (M Frame) referred to in this document is defined such that the X_M axis is a line which is positive from the center of the Earth to the center of the Moon. The $+Y_M$ axis is in the direction of the Moon's instantaneous velocity vector, and the Z_M axis is mutually perpendicular to the X_M and Y_M axes and completes a right-hand triad.

Box 7
Transformation from the M Frame to the I Frame (The T_{IM} Matrix)

The transformation of vector from the M Frame to the I Frame shall be accomplished with the T_{IM} matrix.

The latter shall be generated by a series of rotations. With the exception of the parity change, the rotations here for the Moon are similar to the inverse of the transformation presented in Box 3 for the G Frame.

(a) Rotation about the Z_M axis by the angle $-\beta_M$. β_M is the Moon's in-orbit angle:

$$\begin{matrix} X' \\ Y' \\ Z' \end{matrix} = \begin{matrix} \cos\beta_M & -\sin\beta_M & 0 \\ \sin\beta_M & \cos\beta_M & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X_M \\ Y_M \\ Z_M \end{matrix}$$

(b) Rotation about the X' axis by the angle $-i_M$. i_M is the inclination of the Moon's orbit with respect to the I Frame.

$$\begin{matrix} X'' \\ Y'' \\ Z'' \end{matrix} = \begin{matrix} 1 & 0 & 0 \\ 0 & \cos i_M & -\sin i_M \\ 0 & \sin i_M & \cos i_M \end{matrix} \begin{matrix} X' \\ Y' \\ Z' \end{matrix}$$

(c) Rotation about the Z' axis by the angle $-\Omega_M$. Ω_M is the longitude of the ascending node of the Moon's orbit with respect to the I Frame.

$$\begin{matrix} X_I \\ Y_I \\ Z_I \end{matrix} = \begin{matrix} \cos\Omega_M & -\sin\Omega_M & 0 \\ \sin\Omega_M & \mathrm{COS}\,\Omega_M & 0 \\ 0 & 0 & 1 \end{matrix} \begin{matrix} X'' \\ Y'' \\ Z'' \end{matrix}$$

Transformation of Vectors to the Geodetic Frame (TVGF)

The spacecraft, sun, moon and magnetic dipole vectors shall be transformed to the G Frame where the fundamental vector calculations shall be performed.

Spacecraft Position Vector

The current spacecraft position vector is expressed in the G-Frame as $r_{sc,G} = (-r_{sc}, 0, 0)^t$

where

$$r_{sc} = \frac{R_{sc}\ (1 - e^2)_{sc}}{1 + e_{sc} \cos v_{sc}}$$

Sun Vector

The unit sun vector in the G Frame is obtained by:

$$\vec{S}_G = T_{GI}\ \vec{S}$$

$$\hat{S}_G = \frac{\vec{S}_G}{|\vec{S}_G|}$$

Moon Vector

The Moon vector in the G Frame is obtained by operation on the column vector $M' = (+ R_M, 0, 0)^T$ in the following manner:

$$\vec{M}_G = T_{GI}\ T_{IM}\ \vec{M}'$$

which transform the vector to the G Frame and

$$\vec{M}_G = \vec{M}_G - \vec{r}_{sc,G}$$

which corrects for parallax.

The unit Moon vector is then obtained as

$$\hat{M}_G = \frac{M_G}{|\vec{M}_G|}$$

Magnetic Dipole Vector

The Magnetic Dipole vector in the G Frame is obtained by operation on the column vector = $\hat{D}_G = T_{GI}\ T_{ID}\ \hat{D}$

Computation of SINB, ORBIT, and SOLANG (CSBSOL)

The sine of the spacecraft orbit anomaly is computed as:

$$\text{SINB} = \sin \beta_{sc}$$

The orbit rate is computed by the following procedures:

$$\dot{M}_{sc} = n_{sc} + \Delta t \quad 2\,\frac{\dot{n}}{2}_{sc} + 3\,\frac{\ddot{n}}{6}_{sc} \quad \Delta t$$

$$\dot{v}_{sc} = \dot{M}_{sc} \quad 1 + 2\,e_{sc}\ \text{COS}\ M_{sc}$$

$$\text{ORBIT} = \dot{\beta} = \dot{v}_{sc} + \dot{\omega}_{sc}$$

where

$$\dot{\omega}_{sc},\ M_{sc},\ n_{sc},\ \frac{\dot{n}}{2}_{sc},\ \text{and}\ \frac{\ddot{n}}{6}_{sc}$$

are available from the CEP submodule.

The solar array drive reference angle is computed as:

$$\text{SOLANG} = \tan^{-1} \frac{\hat{S}_{G,Y}}{S_{G,X}}$$

where $S_{G,Y}$ and $S_{G,X}$ are the y- and x- components of the unit Sun vector in the G Frame respectively.

A special case of the solar array drive reference angle computation occurs when the sun vector lies along the orbit normal. In this case, the equation for computing the solar array reference angle becomes indeterminate. This is a transient condition which may arise for dawn or dusk orbits twice each year, and whose onset can be predicted on the ground. This case of indeterminacy is avoided by testing the Y and X components for a value of zero. If that is true, no attempt is made to compute this angle, allowing the value from the previous cycle to remain.

Computation of Yaw Update

Acquisition of SSA Readings

Interaction with the SSA. Each time it is executed, CYAWUP shall test the status of the SSA buffer in the CIU. If the buffer is not ready, a bypass condition is implemented with the setting of flag FBDRD$GE=1.

If the buffer is ready, CYAWUP shall issue IPR DATA LAST to the SSA buffer to read the data word. A reasonableness test shall follow to check whether or not the 14 most significant bits of the data word are all zeros or all ones; if the data word fulfills either of these conditions, it shall be bypassed (FBDRD$GE set equal to one) and shall not count as a valid SSA reading for yaw update purposes.

After the above tests, an OPR BEGIN shall be issued to the SSA buffer of the CIU to initiate data transfer. The data word generated with this OPR BEGIN shall be read by CYAWUP during the next CPU processing cycle. (See SSA transfer function, Figure 4.10.6-23).

Interaction with MODE. The MODE software module will ensure that a new yaw update is available after 21 cycles after CYAWUP initiates FSSA = 1. It will do this by resetting a cycle counter after CYAWUP sets FSSA = 1. When a new yaw update is available, CYAWUP shall set FYAWUP = 1 to alert ADS to this fact and signal MODE of a successful yaw update acquisition within the required number of cycles. GEODAT shall never clear FYAWUP, but rather, it is assumed that ADS will clear this flag upon utilization of the yaw update.

If a yaw update has not appeared within the required number of cycles, MODE will initiate a switch to the secondary SSA I/O bus. At this point, MODE will also reset its counter and set KSSAOB=0 and FSSA=0, thus permitting CYAWUP to begin again to obtain 10 SSA readings.

To ensure that a yaw update shall be made only once per orbit, CYWAUP shall set a flag FORBIT=1 after setting FSSA = 0 and shall reset this flag (FORBIT) to 0 only after the sun leaves the window.

SOLANG Window Test. CYAWUP shall test SOLANG to see if it falls within the window prescribed by the SSAHIG and SSALOW parameters. If the sun is in the window, then valid SSA readings which pass the reasonableness test shall count toward computing a yaw update. After the window test, CYAWUP shall test whether the FSSA flag is set equal to one and if not, it shall set FSSA=1, KSSAOB=0, and NEWS=0 to re-initialize yaw update calculations.

If the sun is not in the window, CYAWUP shall test whether or not FSSA is equal to zero. If FSSA=0, then CYAWUP shall set FORBIT=0 and exit. If FSSA $\neq$ 0, then a yaw update shall be attempted with any SSA readings which have been accumulated for this purpose.

N = SSA OBSERVATION = CONTENTS OF CIU BUFFER AT ADDRESS 415 (HEXADECIMAL)

MSB																
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$N = 0$, $\eta_K = -50° + A_0$
B1													B14			
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$N = 8{,}192$, $\eta_K = 0° + A_0$
B1													B14			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	$N = 16{,}383$, $\eta_K = +50° + A_0$

SSA TRANSFER FUNCTION FORMULA

$$\eta_K = A_0 + \tan^{-1}(N * A_1 + A_2) \qquad A_0 = 47.5° \quad A_1 = 1.454778 \times 10^{-4} \quad A_2 = 1.191754$$

9-4414M

Figure 4.10.6-23. SSA Transfer Function

SSA Data Word Processing. The format of the reading from the SSA is given in Figure 4.10.6-23. CYAWUP shall right shift this word by one. (logical) to scale it properly, and then the sun angle measurement shall be computed from:

$$ETA = \eta_K = A_0 + \tan^{-1}(N*A_1 + A_2),$$

where N is the scaled reading and A_0, A_1, and A_2 are SSA calibration constants. The reference sun cone angle (ETAPRIM) shall be available from CEP, and thus the yaw measurement shall be computed:

$$YAW = ETA - ETAPRIM$$

Successive readings shall be accumulated for later averaging by means of the AVERAGE software module. The averaging shall commence when 10 valid readings have been achieved or when the accumulation process is interrupted because SOLANG has failed to continue to meet its window test.

Sun/Moon Warnings for the ESA

The ESA consists of four sensor clusters each displaced by an angle of 45° from the payload axes in the Y_G-Z_G plane. Each cluster's optical axis is a generator of a cone (semi-vertex angle,τ) centered on the X_G axis is shown in Figure 4.10.6-24. Unit vectors along the cluster optical axis are expressed as:

$$\hat{W}_K = \cos\alpha\,\hat{X}_G + \sin @ \cos\alpha \quad \frac{(K-1)\pi}{2} + \gamma \quad \hat{Y}_G$$

$$+ \sin @ \cos\alpha \quad \frac{(K-1)\pi}{2} + \gamma \quad \hat{Y}_G$$

for K = 1, 2, 3, 4.

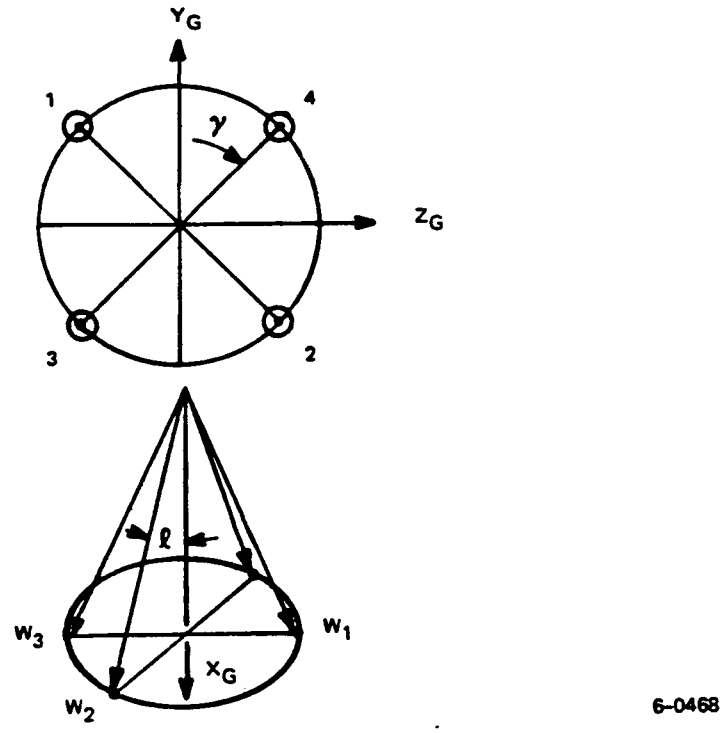

Figure 4.10.6-24. ESA Cluster Geometry

These unit vectors shall be CSMWRN calibration constants (Table 4.10.6-13).

GEODAT generates an output, SMWARN, to indicate sun or moon interference with the ESA.

The test for sun interferences is:

$$\hat{W}_K \cdot \hat{S} \geq \cos T_S$$

The test for moon interference is:

$$\hat{W}_K \cdot \hat{M} \geq \cos T_M$$

where cos T_S and cos T_M are program constants which define the angular interference window for the Sun and Moon, respectively (see Table 4.10.6-12).

The four lower-order bits of SMWARN show the quadrants (if any) in which the sun or moon appear in the earth sensor field of view. The upper 28 bits of this word are always zero-filled. If GEODAT determines that neither the sun nor the moon are in any sensor field of view, the lower order bits (29-32) of

TABLE 4.10.6-13. GEODA CALIBRATION CONSTANTS

Symbol	SPL Tag	Description	Scaling	Type	Units	Nominal Magnitude
A_0	A0CONS	Angle from X_G -Z_G plane to SSA Null	+1	DP	πRadians	0.2638889π (47.5°)
A_1	A1CONS	SSA Bit Weight	-12	DP	$Counts^{-1}$	1.4548×10^{-4}
A_2	A2CONS	Count from Null to start of SSA Pattern	+2	DP	Non-Dim	-1.191854
	WSCONS	X_G Component ESA Quadrants (COS α)	+1	DP	Non-Dim	0.411
	WSNMN1 (4)	Y_G Component of ESA Quadrant #1	+1	DP	Non-Dim	0.645
		Y_G Component of ESA Quadrant #2	+1	DP	Non-Dim	-0.645
		Y_G Component of ESA Quadrant #3	+1	DP	Non-Dim	-0.645
		Y_G Component of ESA Quadrant #4	+1	DP	Non-Dim	0.645
	WSNMN2 (4)	Z_G Component of ESA Quadrant #1	+1	DP	Non-Dim	-0.645
		Z_G Component of ESA Quadrant #2	+1	DP	Non-Dim	0.645
		Z_G Component of ESA Quadrant #3	+1	DP	Non-Dim	-0.645
		Z_G Component of ESA Quadrant #4	+1	DP	Non-Dim	0.645

SMWARN are set to zero. If the sun or moon is in the field of view of the quadrant 1 sensor, bit 32 is set to one. A similar positive test in quadrants 2, 3, and 4 sets bits 31, 30 and 29 respectively.

Magnetic Latitude Calculations

The sine of the spacecraft magnetic latitude is determined as SMAG = -x component of the magnetic dipole vector in the G Frame (D_G).

The ascending/descending flag (FASCDES) is set directly from the in-orbit angle β_{sc}:

$$0 \leq \beta_{sc} \leq \frac{\pi}{2} \qquad \text{ascending (FASCDES = 0)}$$

$$\frac{\pi}{2} < \beta_{sc} < \frac{3\pi}{2} \qquad \text{descending (FASCDES = 1)}$$

$$\frac{3\pi}{2} \leq \beta_{sc} \leq 2\pi \qquad \text{ascending (FASCDES = 0)}$$

Computation of Spacecraft Altitude (CALT)

CALT computes the spacecraft altitude, taking the ellipsoidal shape of the earth and space orbit eccentricity into account, by the following procedure:

$$\delta = \tan^{-1} \frac{\sin \beta_{sc} \sin i_{sc}}{\sqrt{\cos^2 \beta_{sc} + \sin^2 \beta_{sc} \cos^2 i_{sc}}}$$

$$\delta' = \frac{e_E^2 \sin \zeta \cos \zeta}{1 - e_E^2 \cos^2 \zeta}$$

$$r_E' = b_E \quad 1 + \frac{e_E^2}{2} \cos^2 \zeta + \frac{3}{8} e_E^4 \cos^4 \zeta$$

$$\zeta = \frac{r_e' \ \delta'}{r_{sc}}$$

$$\text{ALTITUDE} = (r_{sc} - r_E') \frac{(1 - \delta'\zeta)}{2}$$

where e_E^2 and b_E are program constants (see Table 4.10.6-12)

e_E is the eccentricity of the Earth ellipsoid, and

$e_E^2 = 2f - f^2$ where f is the Earth flattening parameter. b_E is the polar radius of the ellipsoidal earth.

GEODAT Interface Requirements

Figure 4.10.6-25 depicts the interface of GEODAT with other software modules. Table 4.10.6-14 lists data words generated by external software which are utilized by GEODAT. This table and the uplinked ephemeris (see Table 4.10.6-11) comprise the data inputs required by GEODAT.

Except for ephemeris clock updates to reset GDTIME, GEODAT does not modify any of the data inputs.

Table 4.10.6-15 lists data words generated by GEODAT which are utilized by external software.

Table 4.10.6-16 lists the control words generated by external software which are utilized by GEODAT.

Table 4.10.6-17 lists the control words generated by GEODAT which are utilized by external software.

With the exception of GDCKU and GE, the GEODAT data outputs of Table 4.10.6-13 are telemetered to ground. In addition, SMWARN, KSSAOB, FORBIT, and GDTAB are telemetered.

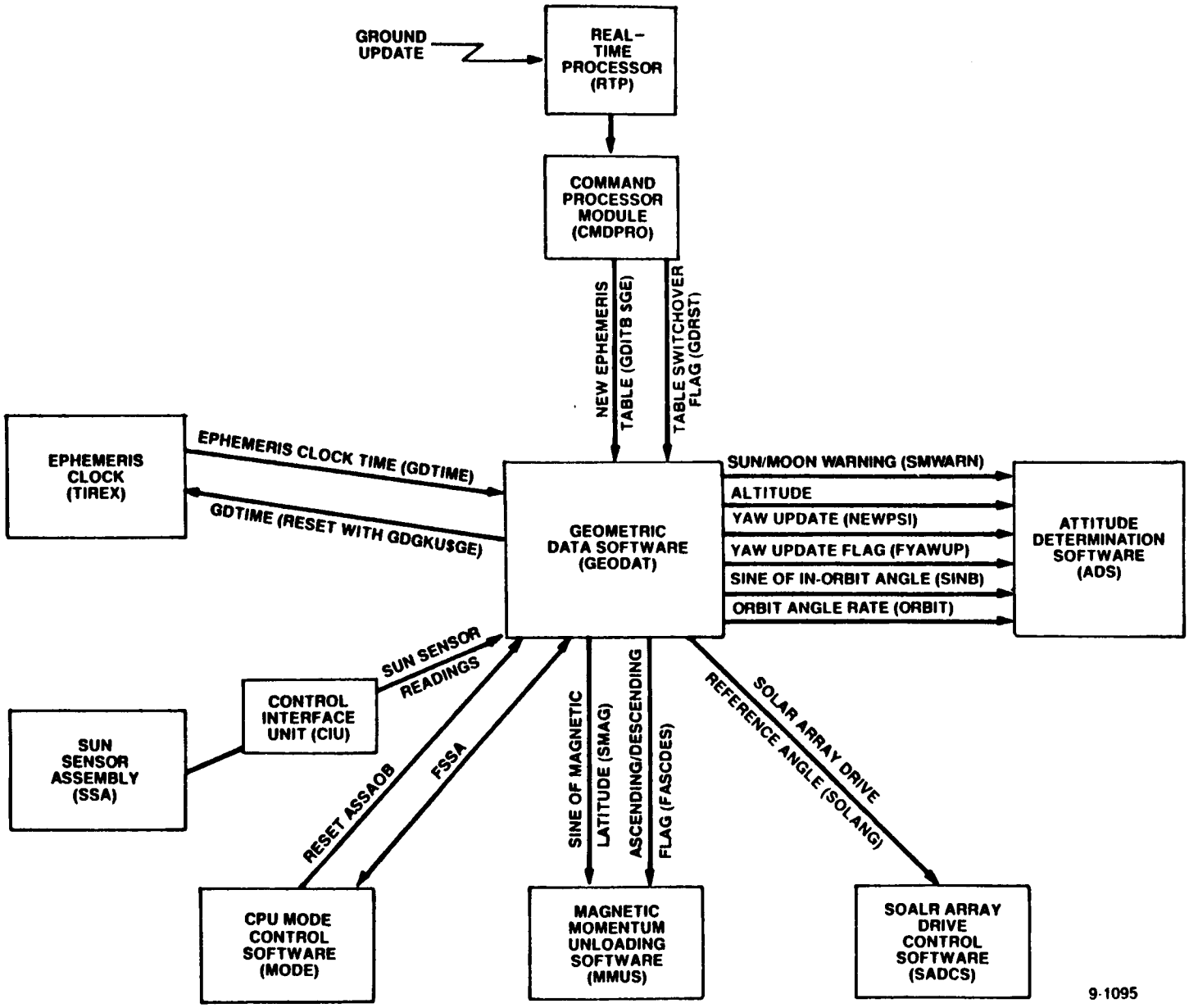

Figure 4.10.6-25. GEODAT Interface Block Diagram

TABLE 4.10.6-14. DATA INPUTS TO GEODAT OTHER THAN THE EPHEMERIS TABLE

Symbol	SPL Tag	Description	Source	Type	Scaling	Units	Nominal Magnitude
t	GDTIME	Ephemeris clock time	TIREX	DP	+21	sec.	-21^{21} to $+2^{21}$
SSA readings - see Table 4.10.6-13							

TABLE 4.10.6-15. DATA OUTPUTS OF GEODAT

Symbol	SPL Tag	Description	Submodule Source	User	Type	Scaling	Units	Nominal Magnitude
	GDCKU	Ephmeris clock update	EUS	CMDPRO, TLREX	DP	+21	sec.	-2^{21}
	SINB	Sine of spacecraft orbit anomaly (in-orbit angle)	CSBSOL	ADS	DP	+1	Non-Dim	-1. to +1.
θS	SOLANG	Solar array drive reference angle (sun clock angle)	CSBSOL	SADCS	DP	+1	πRadians	0-2π
	NEWPSI	Yaw error update	CYAW'P	ADS	DP	+1	πRadians	-0.004 to +0.004
	SMAG	Sine of magnetic latitude	CMAGL	MMUS	DP	+1	Non-Dim	-1. to +1.
	ALTITUD	Spacecraft altitude	CALT	ADS	DP	+10	km	740 - 930
β_{sc}	ORBIT	Spacecraft orbit rate	CSBSOL	ADS	DP	+0	Radians/	.0010

TABLE 4.10.6-16. CONTROL INPUTS OF GEODAT

SPL Tag	Type	Value	Meaning	Set By	Cleared By	Used By
GDRST	DP	0	No table switchover Table switchover cycle	CMDPRO	GEODAT	GEODAT
KSSAOB	DP	0 to 10	Counts valid SSA readings	GEODAT	GEODAT	GEODAT

TABLE 4.10.6-17. CONTROL OUTPUTS OF GEODAT

SPL Tag	Type	Value	Meaning	Set By	Cleared By	Used By
GDTAB	DP	0 1	GDITAB1 in current use GDITAB2 in current use	GEODAT	GEODAT	CMDPRO, GEODAT
FSSA	DP	0 1	SSA Power OFF SSA Power ON	GEODAT	GEODAT, MODE	GEODAT, MODE
FYAWUP	DP	0 1	No yaw update available Yaw update is available	GEODAT	ADS	ADS
SMWARN	DP	Bit = 0 Bit = 1	No sun/moon interface in corresponding ESA quadrant Interference in corresponding quadrant (see 3.2.11)	GEODAT ESA	GEODAT	ESRS
FASCDES	DP	0 1	Ascending part of spacecraft orbit Descending part of spacecraft orbit	GEODAT	GEODAT	MMUS

4.10.7 POWER SYSTEM DESCRIPTION

4.10.7.1 System Description

The PMS module performs, with prior ground consent as appropriate, the routine battery and solar array calculational functions. The battery parameters monitored are the temperature, voltage and charge/discharge currents. The solar array parameters monitored are the current and patch current. On the basis of the battery temperature, voltage and currents, PMS computes the batteries' efficiencies, charge levels and temperature gradients. On the basis of the solar array parameters, PMS determines whether the sun is lost. PMS records

for telemetry, or other ground inspection, battery and solar array data helpful for EPS evaluation and diagnosis. PMS has the capability of triggering the power economization functions of PSSS, CTCES, and the Battery Reconditioning Function (BATREC), with prior ground consent. PSSS activates safestate and inhibits a ground-selected set of Thermal Control Elements (TCE). CTCES shall cycle, as necessary, each TCE of a set selected by the ground. This cycling effectively lowers the set point, thus conserving power. The duty cycle of these modules is 2 Hz, when active. This cycling is intended to provide the minimum heat necessary to prevent freezing or other damage in the vicinity of the cycled TCE.

Activation

The power management software is invoked by the priority level two executive at 2 Hz time in the control computer. It operates to completion on Level 2. If FPSS is set then PSSS is invoked in the control computer. If FTCE is set, but FPSS is clear, then CTCES is invoked. If FPSS and FTCE are clear and TRIG$PM indicates battery reconditioning is enabled, then BATREC shall be invoked.

Conceptually each invocation of PMS, CTCES, and BATREC constitutes a separate activation insofar as the only memory of the previous invocation shall be in data accumulated. PSSS on the other hand shall retain a memory of its previous processing and shall deactivate itself.

Data and Control Interfaces

Figure 4.10.7-1 displays the flow of data and control of the PMS software. Table 4.10.7-1 is a summary of pertinent KLM data.

TABLE 4.10.7-1. KLM SUMMARY

Computer Memory Size	32,768
Number of Batteries	3
Unified Load Package (ULP) at Launch	Yes
Input Telemetry Table Size (TSRS Input Area)	357
Number of TCEs (to be provided for)	42

4.10.7.2 Functional Description

Timing Considerations

In addition to being invoked every 2 Hz, there are additional timing requirements, in the areas of allowable time, for completion of processing and functions to be performed at a slower than 2-Hz rate.

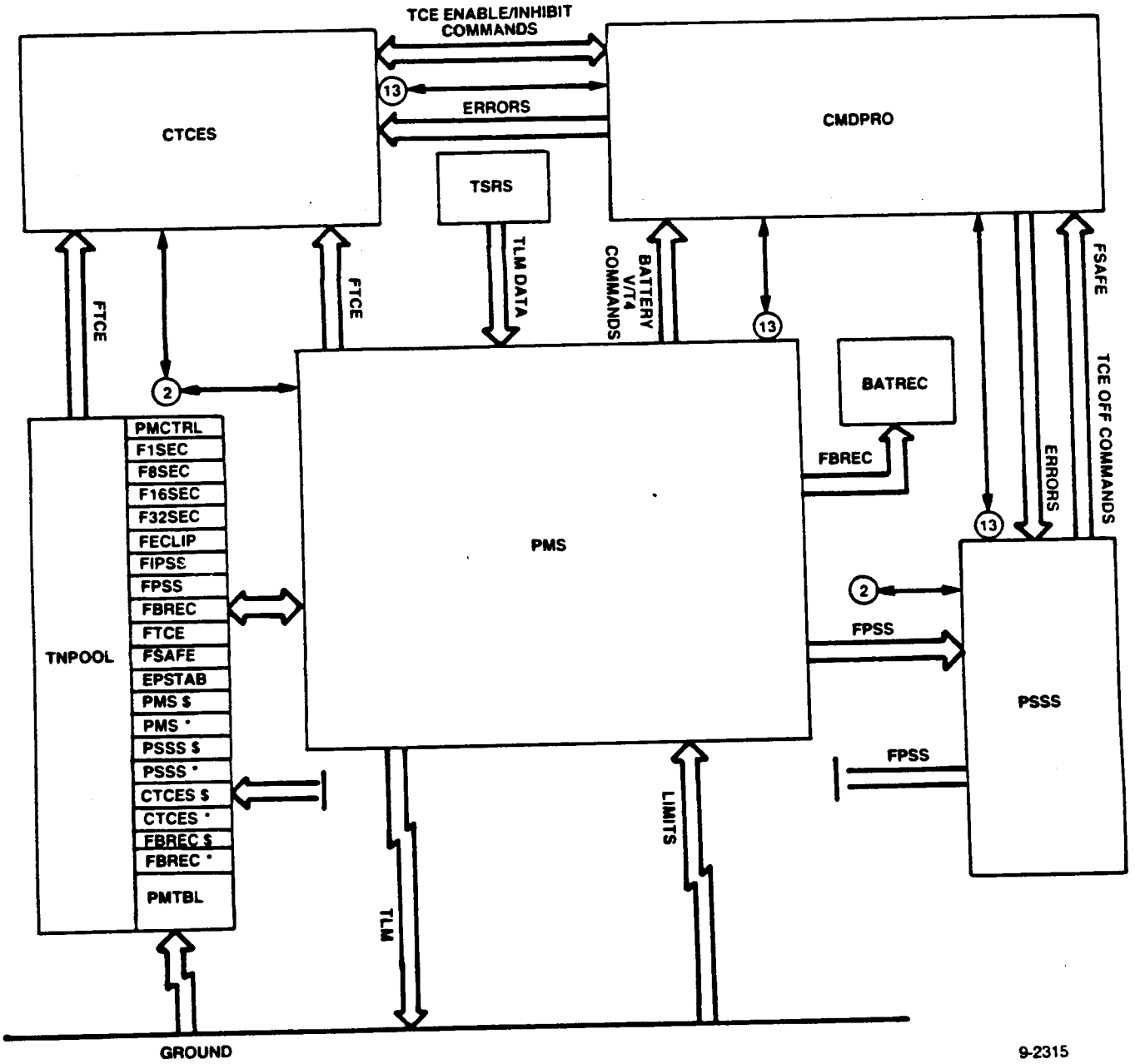

Figure 4.10.7-1. PMS Interface Block Diagram

Time Allowance for Processing

The power management software is allowed up to one hundred seconds to complete the processing of any one invocation. Failures to complete processing are handled by the level two manager.

PSSS Timing

Once activated, PSSS, during its first invocation, activates STESM. PSSS just returns during subsequent invocations while STESM is active. During the first invocation of PSSS after STESM has completed, PSSS performs its TCE inhibit functions. Then PSSS prevents re-activation of itself due to the present cause.

Telemetry-Driven Timing

Certain PMS functions require telemetry. These functions use the latest available value. These functions run at the same rate as their required telemetry. Thus functions requiring 1.0 second telemetry are activated at a 1-Hz rate.

Eight second telemetry consists of two separate sixteen second channels sampling a point with an eight second interval between channels' samples. Similarly some sixteen second telemetry is derived from two thirty-two second channels. The Telemetry Subcom Read Software (TSRS) is not cognizant of sampling by separate channels. TSRS supplies the flags F1SEC, F8SEC, F16SEC, F32SEC. These flags are coherently set prior to PMS activation once every one, eight, sixteen and thirty-two seconds respectively. These flags are cleared by the level two executive after the power management software has completed the processing of the affected 2 Hz cycle. The configuration of F8SEC and F16SEC determines for an eight second telemetry point embodied in two sixteen second channels, which of two channels contains the most recent sample. Similarly the configuration of F16SEC and F32SEC determines which of two thirty-two second channels contains the latest sample of a sixteen second point.

Routine Functions

These functions consist of battery monitoring, sun loss monitoring, filtering and telemetry formatting. All are individually commandable by ground setting of PMCTRL and are telemetry-driven except as noted below. The timing of telemetry driven functions is as specified above. Only commanded functions are performed under telemetry-driven timing.

Functions Performed for Each Battery

The ground commands these functions and supplies limits on a per battery basis.

Charge Level Reset Computation

This function is not telemetry driven. The CLM reset value is converted from ampere hours to ampere seconds and stored in the latest charge level. The commanding bit of PMCTRL is reset to prevent rerunning of this function until next commanded.

Battery Efficiency (CEFF)

This function does not have PMCTRL controlling bits. This function is telemetry driven. The latest Pack A temperature is retrieved and averaged with the previous Pack A temperature. The previous Pack A temperature is then updated. Pack B temperature is processed similarly.

The battery efficiency shall then be computed according to the formula:

$$\text{Efficiency} = EA5 * T^5 + EA4 * T^4 + EA3 * T^3 + EA2 * T^2 + EA1 * T + EA\emptyset$$

where T = Average Pack A and Pack B, with +8 scaling.

Charge Level Monitor (CLM)

The charge (IC) and discharge (ID) currents are retrieved. The Charge Level (CL) is computed according to the formula.

$$CL = CL' + A - B$$

where:

CL' = previous charge level of the battery under consideration

A = EFF * (CA5 * IC^5 + CA4 * IC^4 + CA3 * IC^3 + CA2 * IC^2 + CA1 * IC + CAØ) — If IC ≠ Ø

A = Ø — If IC = Ø

B = DA5 * ID^5 + DA4 * ID^4 + DA3 * ID^3 + DA2 * ID^2 + DA1 * ID + DA0 — If ID = Ø

B = Ø — If ID = Ø

EFF = Efficiency as specified in CEFF.

Failure of the charge level to exceed or equal the ground supplied limit sets the battery's corresponding bit in PSTAT$PM, to record the failure.

Voltage Level Monitor (VLM)

The latest voltage is retrieved and compared against the ground supplied minimum. Occurrences of voltage less than or equal to the minimum are counted. If this condition persists for a ground supplied period, then the failure is recorded in PSTAT$PM and the count is cleared.

PMS will recognize and save the lowest battery voltages within the current orbital period and the previous three orbits.

Temperature Monitor (TEMM)

The latest Pack A and Pack B temperatures are retrieved. Consecutive occurrences of the average of these values exceeding the ground supplied limit are counted. If this count reaches the ground supplied limit, then PSTAT$PM is updated to reflect the failure and the counter is cleared. Maintaining a consecutive failure counter provides protection against poor quality short term telemetry, as the condition has to persist for some ground specified period before the condition is regarded as a failure.

This concept is used to provide four failure 'levels' as follows:

a. For each battery, an index (recording failure levels 1 through 4) and a failure count shall be maintained independently. For each battery and level, a temperature threshold, a count limit, and a command to be issued to CMDPRO shall be independently stored and shall be ground alterable. For each command, enough space shall be allocated for any command supported by CMDPRO. The default commands for levels 1, 2, 3, and 4 shall be to select V/T curve 7, select trickle charge, select the backup charge regulator, and disconnect the charge path for the battery, respectively.

b. The higher of the pack A and Pack B temperatures shall be obtained.

c. If the count of consecutive occurrences of that temperature exceeding the current level's threshold reaches the count limit for the level, the battery shall be deemed to have failed at that level. The corresponding command shall be issued, the count cleared, and the failure level increased by one. A separate bit shall be set in PSTAT$PM for each battery that fails at level 1 and for each battery that fails at level 2.

d. The first battery to fail at level 2 shall inhibit the other two batteries from issuing level 2 or higher commands. Three bits of TRIG$PM shall be used for the latter purpose and shall be resettable only by ground command.

e. If temperature monitoring is disabled for a battery (PMCTRL bit cleared by the user), the variables shall be initialized for the battery to reflect level 1 status with no temperature failures.

Temperature Gradiant Limit Function (TEMM2)

The latest Pack A and Pack B temperatures are retrieved. Consecutive occurrences of the absolute value of the difference between the Pack A and Pack B temperatures exceeding the ground supplied maximum shall be counted. If this count reaches the ground supplied limit, then PSTAT$PM is updated to reflect the failure and the count shall be cleared. If this failure or the failure of TEMM occurs, then the battery V/T7 command is issued.

Sun Loss Monitor (SLM)

SLM maintains a count of consecutive occurrences of solar array current less than or equal to the corresponding ground supplied minimum while the solar array patch current is less than or equal to the corresponding ground supplied limit. If the count reaches the ground supplied limit, then PSTAT$PM is updated to reflect the failure and the count cleared.

One Second Analog Telemetry Filter (FLTR)

Filter Reset

The filtered value and filter gain are reset to the ground supplied values. The commanding bit of PMCTRL (Figure 3) is reset to prevent rerunning this function until recommanded by the ground.

Filter Processing

Either word 0 (a commandable analog channel) or word 2 (the solar cell path short circuit current) of the 1.0 second analog telemetry is filtered as commanded by PMCTRL. Word 2 is filtered if filtering of both Word 0 and Word 2 is commanded. Filtering is according to the formula:

$$F = (V - F') * GAIN + F'$$

where: V is the quantity being filtered
F is the new filtered value
F' is the old filtered value
GAIN is the filter gain.

Telemetry Formatter (TLMF)

This function is not commanded and is not telemetry driven. This function computes the present charge levels of the batteries in ampere hours, maintains the queue of charge levels at day-to-night orbital transitions and the queue of charge levels at night-to-day orbital transitions. Should the present ampere seconds charge level for a given battery exceed a ground supplied maximum at a day-to-night transition then it shall be redefined equal to the maximum.

Trigger Power Survival State (TPSS)

If one of the triggering conditions, defined in PSAT$PM and allowed by the ground supplied trigger (TRIG$PM) exists, then PMS requests the power conservation functions by setting the request flags FPSS and FTCE. PMS then sets the PMS/PSSS request inhibition flag FIPSS to prevent reactivation of PSSS and CTCES in response to the same condition.

Power Conservation Functions (PSS and CTCES)

It is intended that these functions be activated in response to some anomalous in-orbit life-threatening condition. These functions place the spacecraft in

a low power consumption safe state. These functions are activated by ground command or autonomously by PMS with ground consent. In either case their activation provides additional time for ground diagnosis and possible rectification of the anomaly.

Power Survival State Software (PSSS)

This function economizes on power consumption by activating STESM, thus putting the spacecraft in a known state of low power consumption, and by inhibiting a ground selected set of TCES. The processing details follow.

STESM Activation

If this is the first invocating of this activation of PSSS then PSSS will issue the FSAFE command and return.

STESM Non-Concurrency

Having activated STESM PSSS waits until STESM has completed its processing before doing any active processing of its own.

TCE Inhibition

When STESM has completed its processing, PSSS issues a series of TCE inhibit commands. These TCE commands are supplied in the table TCOF$PS. A zero entry in TCOF$PS signifies that there is no command for the corresponding TCE.

PSS maintains a counter, ERRCT$PS, of any TCE inhibit commands which the CMDPRO module failed to execute.

PSS De-Activation

Having completed the TCE inhibition, PSSS clears the PSSS activation request flag FPSS. Thus PSSS is available for re-activation at a later time.

TCE Cycling (CTCES)

The ground can define a set of TCEs to be cycled. For each so selected TCE a temperature telemetry point and dead band are selected. CTCES inhibits any selected TCE whose corresponding telemetry point indicates a temperature above the upper limit of the dead band. CTCES enables any selected TCE whose corresponding telemetry point indicates a temperature below the lower limit of the dead band. CTCES takes no action for unselected TCEs or selected TCEs whose corresponding telemetry point indicates a temperature within the dead band.

A counter ERRCT$CC is maintained by CTCES and contains the number of failed TCE enable/inhibit commands issued to date.

Battery Reconditioning (BATREC)

This function shall be enabled/disabled by ground command, and shall be performed when the reconditioning battery is off-line. A battery shall be

determined to be off-line when CDPATH (charge/discharge path image) indicates the reconditioning battery's charge and discharge paths are disconnected. BATREC shall be enabled by setting two bits in the PMS Trigger Word (TRIG$PM). Those two bits will have the following meaning:

00 No reconditioning
01 Recondition Battery 1
10 Recondition Battery 2
11 Recondition Battery 3

Once BATREC is enabled it shall be called from PMS every 8 seconds until processing is complete.

BATREC shall monitor the reconditioning battery's voltage (BATVOLT), and when it is above the pull-up threshold (PULLUPTHR) the following commands shall be issued to the reconditioning battery:

a. Command Trickle Charge
b. Disconnect pull-up resistor
c. Connect charge path to solar array bus
d. Command primary charge regulator

Once the reconditioning battery's voltage is above the safe threshold (SAFETHR), and it's a day-night transition, trickle charge shall be commanded to the reconditioning battery and 12.5A to the two supporting batteries. At the next daylight period, after the two supporting batteries have been fully charged, all three batteries shall be commanded to 10.0A.

The above process is repeated until the reconditioning battery's state of charge (B$LSTCL) is above the reconditioning threshold (RECCUR). At this time, the reconditioned battery shall be commanded to trickle charge and the two supporting batteries shall be commanded to 12.5A. The BATREC enable flag in TRIG$PM shall be cleared and software control of the reconditioned battery shall be terminated.

4.10.8 MODULE CHARACTERISTICS

(This section is arranged alphabetically by program acronym for ease of reference).

4.10.8.1 ACS (Attitude Control Software)

This module performs the functions specified in PS-3274008. As part of ADACS, it meets the requirements on control processing specified in PS2280431.

ACS is activated once each 0.5 second executive cycle, and there is no requirement to operate at other than once each 0.5 second cycle.

The prime function of ACS is to compute, format, and transmit the attitude controls signals to the reaction wheel system. Upon entry, ACS shall determine the attitude control submode, retrieve the set of error-angles (and error-rates), and compute the torque command for the reaction wheels.

The determination of the control torques is based upon the ADACS control submode, previous state of the ACS program and other software, the RWA configuration at the time of the computation, state of each RWA, and the state of the magnetic momentum unloading system.

ACS transmits the commands to the RWA's via the CIU. It also, as required, tests the spare RWA. This includes formulating and formatting the torque and power switching commands to the wheels.

ACS is responsible for extracting the three equivalent orthogonal wheel speeds (momentum) from the four RWA status words. ACS determines which three wheels are available and switches on those RWAs.

ACS performs an "ultimate" monitoring function. It compares the attitude errors computed to the specified limits and sets the attitude error flag if the error criteria are exceeded. ACS determines which RWA tests are to be performed and initiate those tests requested or required.

ACS terminates MMU coil pulse discretes. ACS issues MMU coil switching as requested. The condition of the MMU coils will be made available to ACS and it utilizes this information to effect corrections to the torque commands.

ACS is responsible for generating and/or transmitting certain commands to the external (to the CPU) equipment. The actual transmission or execution of the commands will be performed by the Command Processor, Module CMDPRO, on interrupt level 13. Two types of command (Preset I/O and Pulse Discrete) will be transmitted but the action required is essentially similar.

The items to be transferred will consist of a 16 bit command and, for Preset I/O only, three associated 16-bit data words.

ACS accepts and processes override torque commands from ATMUL when GN_2 unloading is in progress. It suspends RWA tests which may be invalidated by such activity.

4.10.8.2 <u>ADACTEST (ADACS Test Software)</u>

This module satisfies PS-3274005. It provides simulated nominal orbit and test-specific attitude input data for use in ground testing. ADACTEST saves the actual hardware attitude inputs for CPU telemetry. Nominal orbit ADACTEST functions consists of replacing gyro and earth sensor inputs with a pre-determined rate history to simulate on-orbit conditions.

The nominal gyro history will be sequenced so as to drive the reaction wheels in a repeatable cyclic pattern which results in momentum unloading. The earth sensor inputs will be held null during nominal operations. Thus, ADACS will be driven entirely from gyro data.

Test specific ADACTEST functions are controlled by ground command. When enabled, a given test consists of overriding the appropriate input data with a

pre-determined sequence of test values for a specified time span. Gyro data, earth sensor measurements data and quadrant status are overrideable on command.

ADACTEST is called as a subroutine of ADS. It will be prevented from operating after launch by a hardware lockout (liftoff flag).

4.10.8.3 ADS (Attitude Determination Software)

ADS performs the functions specified in PS-3274007, and forms part of the ADACS software which satisfies the specification of the subsystem (PS2280431).

ADS is initiated once each 0.5 second control cycle, and there is no requirement to operate at other than once each 0.5 cycle.

The primary function of ADS is to test and process the data from the ESA. This data will have been previously collected and scaled by module ESRS.

The processing consists of computing a parameter X_n for each sensor quadrant. This parameter is be computed by one of several alternative methods, which depend on the state of the sensor and which will in general involve testing for possible error or warning conditions.

Once a set of suitable X_n's has been computed, the program shall compute a set of Euler angle which ultimately are transformed into the roll and pitch error terms for control purposes.

In addition to the computation of the roll and pitch error angles, the program shall examine the data, both the basic sensor readings and computed parameters, to determine the state of the sensor system.

Inconsistencies in the data and certain other conditions (e.g., quadrant off the earth) are flagged for submode determination.

ADS also chooses the proper gyro to P-frame transformation. This is based on the gyro status word (either IMU hardware, or ground supplied).

ADS extracts three orthogonal body rates from the available gyro data and corrects these rates for known biases, and to remove unwanted components such as inertia and orbital precession which are not used for control. This data will have been previously collected and filtered by module DFS.

AFS also monitors the body rates to see if they remain within limits for 10 seconds (20 consecutive cycles). ADS flags the rate history for submode determination.

ADS determines the yaw Euler angle of the satellite. This is accomplished by summation of the corrected yaw axis incremental position.

Once per orbit ADS also determines the yaw axis rate bias and position update requirement, using sun angle measurements.

ADS provides submode determination for the Attitude Control Software. This determination is based on the state of the ESA, namely inconsistencies in data and quadrant off the earth.

All computations within ADS are performed in double precision. For programming convenience, the program may remain in the double precision mode for all operations including housekeeping.

4.10.8.4 AGS (Ascent Guidance Software)

This module is a purchased item and satisfies the requirements of the Statement of Work WS-2629965, and the contractor's equipment specification 2629965. The interfaces between AGS and the other software (most importantly HAND) satisfy the requirements in the Interface Control Specification ICD-T11-25004.

AGS provides for the navigation, guidance and control of the launch vehicle from liftoff through handover to the orbit phase software. It provides its own telemetry routine.

AGS makes such deployments and issue discretes as specified in 1B97937.

In the prelaunch phase, AGS provides for a closed loop test (sim-flight) and other tests. It also provides for an alignment computation to be made before liftoff.

AGS operates in a manner so as to allow interruption by RTP to accept real time commands. These commands will be executed by CMDPRO (called by RTP).

AGS also allows sufficient time margin for the execution of CVQO, TIKS, and RWACS.

4.10.8.5 ATMUL (Automatic Thruster Momentum Unloading)

This module satisfies the requirements allocated to it in PS-2295411. ATMUL always determines from RWA readings and ADS-calculated body rates the total system momentum on a per-axis basis. When this momentum exceeds a threshold value, which is larger than that required for activation of the magnetic torquing coils, the existence of an external disturbance is inferred and ATMUL (if enabled by ground command) takes steps to reduce the momentum. If necessary, ATMUL opens the RCE GN_2 latch valve.

Prior to firing thrusters, ATMUL may request a preliminary slowdown of the reaction wheels in order to lessen attitude excursions caused by the impulse nature of the jets. It controls the events in the unloading sequence according to schedules provided. Separate timing parameters are used, depending on whether the attitude control submode is on the earth or in the process of acquisition. ATMUL chooses the proper thruster pair for the axis and direction being unloaded and requests a jet firing of 0.1 seconds by TCNTRL. Further unloading is prevented for a pre-determined interval in order to allow the ADAC subsystem to settle down after each jet pulse.

4.10.8.6 CARP (CPU Alarm Response Program)

This module satisfies all the requirements in PS-2285533.

CARP executes on level 16 in response to CPU alarm interrupts (i.e., hardware-detected faults). When activated, CARP indicates the occurrence of an error for reporting via telemetry and saves pertinent information about the error for later transmittal to the ground.

While CARP is active it provides for the normal operation of CPU telemetry (CTEL) and CPU dump (GDUMP) routines.

Return to the normal processing is made at the time of the next 2 Hz flag. A flag is set to communicate with the MODE program.

CARP also provides the exit routine for (normal) POPS exit.

When an error is first detected, CARP saves all the CPU registers, including S (status), which indicated the type of the hardware alarm and PC (program counter) which gives the location of execution at the time of the error. In the event of multiple alarms, CARP counts the number of alarms and saves the same register information from the most recent set of save locations, thus preserving the data from the first alarm.

4.10.8.7 CMDPRO (Command Processor Software)

CMDPRO shall perform the tasks specified in PS-3274076 and, as part of the Command and Control Subsystem, satisfies the command requirements specified in PS-2285212.

The Command Processor module accepts commands from the ground through the Real Time Processor module (RTP), the Stored Command Processor module (SCPRO), or other CPU software modules.

It tests for proper command syntax and command word format before executing a command. Command Processor executes Level Discrete, Pulse Discrete, Software Discrete, Software Parameter, and Distinct Procedure commands. These commands provide control over the spacecraft and the CPU software. CMDRPO maintains a table of the contents (images) of the parallel buffer to which it outputs.

The Command Processor oversees a queue of Command Verify (CV) words. The input from this circular buffer is handled by the module CVQI, while the output from this circular buffer is handled by the module CVQO. CV queue entries include echoes of the words uplinked through RTP, special command verification words, and error message codes.

CMDPRO provides additional level discrete commands and distinct procedures to satisfy all output needs of the CXU (CIU Annex).

Commands requiring a delayed response (such as the termination of pulses) or a lengthy computation are processed with the assistance of module TIKS on a lower level.

4.10.8. CTES (Cycle Thermal Control Elements)

The module satisfies the requirements assigned to it in PS-2295413.

CTCES monitors the TCE temperatures in the subcom telemetry and use the existing enable/inhibit command to maintain them between maximum and minimum temperatures specified in tabular form.

As part of the PMS, CTCES may be activated when Power Survival State is triggered. A ground flag shall be provided to allow its function to be locked out.

4.10.8.9 CTEL (CPU Telemetry)

This module satisfies all the requirements in PS-2285525.

CTEL provides for the collection and transfer of CPU data to the TIP for inclusion as CPU telemetry. It is called by TIREX 10 times per second, in response to level 11 interrupts generated by the TIP. CTEL transfers three words to the TIP each time it is called.

The commutation scheme used by CTEL is based on 9 tables of addresses which refer to CPU memory locations. Each table includes 15 addresses and thus covers a single half-second cycle. A complete CPU telemetry frame is 8 seconds long. During this 8 seconds, the data referred to by the first table is transmitted 8 times and the data referred to by each of the other tables is transmitted once.

There is no requirement to synchronize the start (or end of a CPU telemetry frame with the overall TIP frame.

4.10.8.10 CVQI (Command Verify Queue Input)

This module satisfies the requirements imposed by PS-2285513.

CVQI is callable as a subroutine by RTP and CMDPRO. If the queue is found to be full, a message to that effect is inserted and additional CV words discarded until space opens up.

4.10.8.11 CVQO (Command Verify Queue Output)

This module satisfies the requirements imposed by PS-2285513.

CVQO is called by TIREX each 0.1 second and outputs to the TIP without requiring an interrupt signal. Entries in the queue are output in the order in which they were inserted.

4.10.8.12 CYCLE (Cycle Executive Software)

This subprogram is described in PS-2285523.

CYCLE is activated each 10 Hz in response to IMU interrupts. It counts such interrupts and check their regularity. It updates software clocks as well as the ephemeris time clock (ETC).

Each 0.1 second, CYCLE shall call the TCNTRL, CVQO, and DFS subroutines.

Each 0.5 second (measured by counting 10 Hz interrupts or observing the backup 2 Hz flag), CYCLE calls MODE and resets the CPU Telemetry Index. CYCLE collects flags into composite telemetry word (s).

CYCLE collects speed and status from one reaction wheel each 0.5 seconds, thus requiring 2 seconds to input and format data from all four wheels.

4.10.8.13 DFS (Digital Filter Software)

This module satisfies the requirements in PS-3274010 and PS-2280431 (filter characteristics only).

DFS is designed to operate at a frequency of 10/sec. It is called by CYCLE as a subroutine.

Each 0.1 second, DFS obtains the gyro data from the special IMU buffer in the CIU. It checks for read errors. In addition, it records the IMU status word. In the backup CPU, DFS provides a delay of the first read of the data until the time when the buffer is expected to be available.

DFS preserves the current and preceding gyro values for 4 past cycles and the filtered values to permit continual filtering.

Each 0.5 second DFS assembles (for use by ADS) the sum of the filtered values over the past 5 samples and the last filtered value for each gyro.

The data from the four gyros is processed independently and is not adjusted for calibration biases at this point.

4.10.8.14 ESRS (Earth Sensor Software)

This module satisfies the requirements of PS-2285516.

ESRS reads and preprocess the ESA data for use in ADS. The ESA generates 4 interrupts each 0.5 seconds, and the TIREX Level 8 executive will respond and call ESRS.

ESRS reads the three data words. A flag is set if excessive read delays are experienced. The data will be checked for errors (per PS-2285516) and scaled by multiplying by the calibration coefficients. If an error is noted, the quadrant will be marked as unused in the quad use word (QUW).

The data is placed in memory for use by ADS. Because of the time sequence of data collection and use, there is a double buffer. A flag is set to establish the buffer use. The data being collected on this cycle is placed in one buffer, and the data being used for computation is taken out of the other buffer.

The design of ESRS insures that if no interrupts are received and ESRS is not called, then ADS will know that no data is available. This is accomplished by having ADS mark the quadrants as "unavailable" and ESRS will mark them "available" when data is received.

4.10.8.15 FATN (Arctangent Function) See PS-2285524.

Given X_1 and X_2 where $-2 \leq X_i < +2$, this module returns the arctangent of X_2/X_1 in π - radians.

4.10.9.16 FCOS (Cosine Function) See PS-2285524.

Given X in π - radians where $-1 \leq X < 1$, this module returns the cosine of X. FCOS calls FSIN to assist in its computation.

4.10.9.17 FMAG (Vector Magnitude Function) See PS-2285524.

Given a three-element vector X, where $-1 \leq X_i < 1$, this module returns $X_1^2 + X_2^2 + X_3^2$. FMAG calls FSRT to assist in its computation. (Notice that the result is ≤ 3.)

4.10.9.18 FROT3 (3-axis rotation of a vector) See PS-2285524.

Given A_1 the array of sines of rotation angles.
B_1 the array of cosines of rotation angles.
C_1 a three-element, normalized vector to be rotated.

This function returns the new coordinates of the vector after it has been rotated about the defined set of axes (Z, X', Z") through the specified set of angles.

4.10.9.19 FSIN (Sine Function) See PS-2285524.

Given X, in π - radians where $-1 \leq X < +1$, this module returns the sine of X.

4.10.9.20 FRST (Square Root Function) See PS-2285524.

Given X where $-1 \leq X < +1$, this function returns an estimated value of the square root of $|X|$.

4.10.9.21 GDUMP (General Dump)

This module satisfies all requirements in PS-2285524.

GDUMP provides for the transfer of data from a continuous block of memory to the TIP. It is called by TIREX in response to interrupts on L10, which occur at the rate of 20/sec. Dumps are initiated by commands executed by CMDPRO.

GDUMP provides for an interface with CMDPRO, whereby the start and stop addresses of the dump are established. GDUMP aborts operations if it is called and it has not been initialized by command.

When activated properly, GDUMP transfers 3 words on each call until the entire area specified has been dumped.

Only one CPU will dump at a time through a commandable bus-select connected to the single dump buffer. GDUMP insures that at termination of its operation the non-control CPU has access to the dump buffer.

4.10.9.22 GEODAT (Geodetic Data Software)

This module satisfies all the requirements in PS-3274078.

GEODAT computes the following instantaneous values based on a clock and an uplinked ephemeris table.

1) The sine of the spacecraft orbit anomaly (SINB) and the orbit rate (ORBIT).

2) The sine of the magnetic latitude (SMAG) and furnish a flag (FASCDES) to indicate whether the spacecraft is on the ascending or descending side of its orbit.

3) The distance of the spacecraft from the local surface of the earth reference model (ALTITUD).

4) The solar array drive reference angle (SOLANG).

5) Sun/moon warning word (SMWARN), which indicates which quadrants of the Earth Sensor Assembly (ESA) will encounter sun/moon interference.

6) In addition, once per orbit GEODAT shall compute a yaw update (NEWSPI). It provides a flag (FYAWUP) to indicate when this update is available.

4.10.9.23 HAND (Handover Software)

HAND satisfies the general system requirements as stated below. It shall perform the tasks specified in its performance specification PS-2285530, which will be in agreement with the Ascent Guidance Interface Control Drawing TBD.

HAND is an independent module resident in the B-Bus CPU during ascent and initial orbit phase operations. It is quiescent until entered by AGS at the end of the ascent sequence of operations. This program will execute on priority level 11. The Ascent Guidance Software (AGS) will initiate handover by jumping to the priority level 11 and branching to HAND. The control of the execution of programs in the CPU remains with HAND until such time as it has completed its tasks. Upon completion of the tasks, HAND turns over control to the orbit software by clearing all IQR bits (except level 9).

HAND issues commands to set or reset the modes and status of external units as specified in PS-2285530. All commands are issued through software module CMDPRO on level 13. HAND shall initialize those variables considered critical for the orbit software. It adjusts clocks to account for the deviation of flight time from the expected value. It synchronizes entry into the orbit software with the 2 Hz signal.

4.10.9.24 ITEST (Instruction Test)

This module satisfies all the requirements specified in PS-2285526.

ITEST is a background program able to detect some cases when the SCP-234 processor is not executing its instructions properly. This is accomplished by executing a series of instructions in both single and double precision modes. For each mode, the calculated result is verified by comparison against a known correct value corresponding to the precision currently being tested. Any discrepancy will be considered an error condition.

The various instructions which cause control to be transferred on a conditional basis are tested separately. Any unexpected path receiving control is considered an error condition.

4.10.9.25 LIBRY Software Library Functions)

This collection of general-purpose subroutines satisfies the requirements of PS-2285524.

The mathematical routines FATN, FCOS, FMAG, FROT3, FSIN, and FRST execute in double precision. They may call one another and may share data structures. They shall use limited approximation if necessary to assure executions in reasonable time. They are scaled so that overflow cannot occur accidentally.

All routines have explicit, standardized protocols for parameter passing.

4.10.9.26 MEMCHK (Memory Checksum)

This module satisfies all the requirements specified in PS-2285525.

MEMCHK performs a check on the integrity of various designated blocks of memory of the CPU in which it resides. This check consists of summing (modulo 2^{16}) the contents of the designated memory words, and comparing this sum to a value supplied as input data to the routine.

If the computed sum and the supplied value do not agree, an error flag will be set.

The routine provides for operation on a number of designated memory segments.

4.10.9.27 MMUS (Magnetic Momentum Unloading Software)

This module satisfies the requirements specified in PS-3274006. As part of the ADACS, it conforms to the requirements specified in PS-2280431.

MMUS generates output to control the operation of the Pitch and Roll-Yaw Torquing air-core Coils to unload the momentum buildup on the satellite axes (temporarily stored in wheels).

MMUS determines from threshold conditions which coils need to be energized or de-energized and sets up commands for ACS to issue via the CMDPRO module. MMUS also generates signals to allow ACS to compensate for the effect of the coil torque on satellite pointing.

To assist in meeting these fundamental objectives, named segment:

INHBTD checks for conditions that inhibit MMUS from performing its functions.

REGION determines which axes need unloading or have already been unloaded, and initiate appropriate commands;

Format Coil Commands (FORCMD) assembles coil control commands and compensation values passes the commands and values to ACS;

CLTEST tests the unloading performance of the coils and switches to backup coils when necessary.

4.10.9.28 MODE (CPU Mode Control Executive)

This module satisfies the requirements of PS-3274009.

MODE provides for the operation of the software, taking into account the state of the CPU and the sensors and control elements associated with ADACS. MODE determines whether a CPU and its associated software are performing their tasks, and provides for corrective action if a problem is found. MODE determines whether a "MEOK" should be issued based on the rules specified in PS-3274009.

The state of health of the software and associated hardware is determined in the various modules. Each module sets certain flags and parameters that will be tested by MODE.

MODE also provides redundancy management based on the indicators and flags set in other modules, and the rules specified in PS-3274009. Switchover to redundant units will be performed by commands issued through CMDPRO. These commands will be arranged in a data structure to permit the user to modify the commands over the life of the satellite.

MODE is called by CYCLE once each 0.5 seconds at 2 Hz flag time.

MODE activates STESM if there has been a transition from STANDBY to CONTROL and "this" CPU is OK but the "other" CPU is NOT OK.

4.10.9.29 NULS (Nitrogen Momentum Unloading Software)

This program satisfies the requirements of PS-3274011. It is composed of the modules ATMUL and TCNTRL. NULS establishes a rigorous interface between them, and with the previously existing software.

NULS is described as an "application" program due to its backup nature. Functionally, it may be classified as part of ADACS. NULS will not inhibit the operation of MMUS.

4.10.9.30 PMS (Power Management Software)

This program satisfies the requirements of PS-3274077. It comprises modules PMS, PSSS, and CTCES. As a system, it provides an onboard capability of continuously monitoring performance of the spacecraft power subsystem. From the basic TIP telemetry items, it derives secondary, more convenient, data, such as filtered values, history, trends, and extremes, as well as perform limit checks. Thus, a summary of the condition of the power subsystem will be available at the beginning of each ground station contact.

In addition, if certain pre-defined anomalies are detected, the PMS issues commands to reduce power consumption. The definition of the triggering conditions may be adjusted from the ground. PSSS and CTES are independent entities which are called only when a power emergency has been recognized. They are also available for ground use if an orderly, self-contained power reduction process is desired.

The module PMS performs both routine monitoring and power survival state triggering functions.

It requires relevant telemetry from TSRS and thus will run only in the control CPU. In addition, it must be provided with conservative warnings of the orbital eclipse/daylight transitions.

Specifically, PMS computes the battery charge levels (utilizing an estimate of battery charge efficiency), checks battery temperatures and voltages, looks for loss of sun during daylight and is able to filter dwell channel data. It maintains a charge level history for the previous three orbits. Thresholds and flags related to PMS activation of power survival state, and filter reset values are contained in a designated uplink area.

When commanded from the ground, PMS runs a Battery Reconditioning Function (BATREC). This function monitors the re-charging action on the battery being reconditioned, along with maintaining proper charge on the two remaining batteries.

4.10.9.31 POPS (Power On Processor Software)

This module satisfies the requirements of PS-2272264.

POPS is implemented in Read Only Memory (ROM) and is incorporated into each CPU at the time of hardware assembly. It operates on the highest priority level (16), and is activated either by applying power to the CPU or by a CIU-decoded command.

When activated, POPS interrogates the uplink processor buffer and accepts uplink words. These are identified as addresses or data by the CIC field (see PS-2285212). The data words immediately following an address are loaded sequentially starting at that address. An address word which is not immediately followed by data will be disregarded.

POPS makes provisions for physically setting the contents of any output buffer in CIU. This specifically includes the TIP mode control buffer.

POPS provides a dump mode, which outputs the contents of CPU memory to the TIP for transmission to the ground station.

Through the use of specified memory words (flags and parameters), POPS allows user control over its functions.

POPS provides for an exit to an arbitrary location (user commandable), where a more specific exit routine will be provided by the user.

4.10.9.32 PRIVMOV (Privileged Mode Software)

See PS-2285524. This module moves a specified amount of data from one location in memory to another. It will operate on priority level (15) and thus, is empowered to alter data in write-protected memory blocks. In calling PRIVMOV, a checksum is be used to minimize the danger of accidental memory corruption.

The PRIMOV routine operates in single precision on level 15 and allows the storage of data into write-protected memory.

4.10.9.33 PSSS (Power Survival State Software)

See PS-2285524. This module, when activated by PMS trigger or a ground command, places the spacecraft in a pre-defined minimum-power configuration. It activates STESM and then gradually turns off those thermal control elements indicated in an internal list of commands.

4.10.9.34 Recovers (Recovery Software)

Designed to help recover a spacecraft from an excessively high rate of spin, as required in PS-20004305. This software will run in the control computer when commanded from the ground, and will use the spacecraft magnetic momentum unloading system to attempt to reduce whatever high rate is on the spacecraft.

4.10.9.35 RTP (Real Time Processor)

This module satisfies the requirements of PS-3274793. RTP accepts ground inputs to the Command and Control Software. The CIU generates a level 12 interrupt when uplink data is present. RTP inputs the uplink buffer status and uplink data word, thus acknowledging the interrupt.

The major duties of RTP are:

1. Check command sequences for proper form;
2. Initiate command execution;
3. Provide command verification.

RTP calls PRIVMOV to perform memory loads. CMDPRO is activated to perform all other functions. RTP generates error messages when improper sequences are detected and calls CVQI to insert them in the Command Verify Queue.

4.10.9.36 RWACS (Reaction Wheel Control Software)

This module satisfies the requirements of PS-2291554.

RWACS runs in the control CPU during the Ascent phase. It executes on Level 4 and is initiated by AGS. Its functions are to run the reaction wheels at a set of constant speeds (to be specified before launch) and to call the TIKS module to allow pulse discrete commands to terminate correctly.

4.10.9.37 SADBIAS

When initiated by ground command, SADBIAS induces an offset to the solar array, as described in PS-20004302. The SADBIAS module feeds an error rate to the SADCS, thus "tricking" the software into placing the array at the desired offset position.

4.10.9.38 SADCS (Solar Array Drive Control Software)

This module satisfies the requirements of PS-2285521.

SADCS is part of the ADACS-related software. Its major function is to command the Array Drive Electronics (ADE) which in turn provides the drive signals for the Solar Array Drive (SAD). SADCS also monitors the SAD/ADE response to issued commands and attempts to correct for electronic failure.

The SAD is a closed-loop rate servo, which drives the Solar Array at a constant commandable rate. SADCS maintains array position within 5° of the sun line, as calculated by GEODAT. If the SAD position error grows excessively or an electronic failure cannot be circumvented, then SADCS sets a flag for MODE to attempt switching to the backup ADE. SADCS issues all other commands (via CMDPRO) itself.

SADCS operates on one of the lower interrupt levels. SADCS is normally called and performs its computations once each half second, but it is designed to perform correctly if delayed for up to 40 seconds.

4.10.9.39 SADTEST (Solar Array Drive Test Software)

This module satisfies PS-2295222.

SADTEST provides simulated nominal and test-specific Solar Array Drive responses to commands issued by SADS, for use in ground testing. In the event that the SAD is restrained ("Pinned"), SADTEST is able to override the SAD position or ADE status.

4.10.9.40 SCPRO (Stored Command Processor)

This module satisfies PS-2285566. As part of the Command Subsystem, it conforms to the requirements of PS-2285212.

The primary function of SCPRO is to arrange for the execution of commands uplinked to a designated area of CPU memory at the desired time. SCPRO calls CMDPRO to actually execute commands.

SCPRO is called every 0.5 seconds and is allowed one second to complete its tasks. That is, on the first half second following a new activation of SCPRO, execution is allowed to resume at an intermediate location.

The major operations of SCPRO in support of its primary functions are:

a. Copy Command Time (CMDT), the current value of the Elapsed Time Clock (ETC);

b. Fetch a command word from the Stored Command Table, and compare its time tag to CMDT;

c. Move the command word to a buffer area when the time tag matches CMDT;

d. Move all data words associated with that command word to the buffer area;

e. Transfer control to CMDPRO to execute the command.

4.10.9.41 SOPS (Standby CPU Operations Software)

This module satisfies all the requirements of PS-2285529.

SOPS is designed to operate in the standby CPU during the Ascent phase of the mission. That CPU is "locked" on the A-bus and receives level 9 interrupts at the rate of 2/sec. There are no telemetry interrupts. This program is intended to encompass all unique code, notably interrupt stubs, needed during Ascent. (Note that there is no backup to the guidance functions of the control CPU during ascent.) The major functions of SOPS are as follows:

- Initialize critical software parameters while on level 16;
- Allow for real-time commands to the standby CPU and command verification;
- Observe liftoff through buffer 149;
- Acknowledge level 9 interrupts and count time into flight, looking for the handover signal from the B-Bus CPU;
- When handover is signalled (or excessive time has passed), SOPS effects a transfer to the orbit mode software;
- This transfer will be similar to handover in the control CPU but contains no hardware commands;
- SOPS waits for IMU interrupts to synchronize before exiting to orbit code.

4.10.9.42 STESM (Software to Establish a Safe Mode)

This module meets the requirements of PS-3274079.

STESM is intended for conditional operation during Orbit phase operations. It provides the facility to place the satellite and its equipment into a known state. This is done by issuing a sequence of commands.

The commands are organized in a way that allows them to be changed by ground revision of a table, thereby giving the user control over the state that is established.

STESM is be called by MODE on the cycle when the standby CPU becomes the control CPU. This establishes a known state before the CPU begins to execute its control software. STESM may also be called by PSSS prior to power reduction.

4.10.9.43 TCNTRL (Thruster Control Software)

This module satisfies the requirements allocated to it in PS-2295411.

TCNTRL is activated at 0.1 second intervals during orbit phase operations and provides for the accurate metering of nitrogen gas pulses if needed. TCNTRL issues an all-thrusters-off command only if a flag has been set to indicate that some thrusters were previously turned on.

TCNTRL while enabled, checks for the presence of a thruster request from either the ATMUL software or the ground. If a request is pending, TCNTRL first assures that the SCU is on and then opens the indicated jets at the last 10 Hz before 2 Hz. (This is done to minimize the disruption caused by a level 16 alarm during the pulse). Requests for more than 0.1 second are realized as multiple 0.1-second on-pulses occurring at 2 Hz intervals.

4.10.9.44 TIKS (Timed Tasks)

The requirements for this routine are in PS-2285513.

TIKS will be activated every 0.5 seconds, in both ascent and orbit phases, on a low priority interrupt level. Its primary functions are as follows:

- Maintain prologue timer;
- Terminate pulse-discrete commands. TIKS calls CMDPRO to do the hardware output;
- Compute commanded memory checksums. This code is similar to the background MEMCHK program.

TIKS shall issue appropriate command verification during its operations.

4.10.9.45 TIREX (TIROS-N Executive Software)

The module satisfies the requirements of PS-3274075. It is the executive control and contains entry points for all interrupt levels:

	LEVEL 16	CARP
	LEVEL 15	PRIVMOV
	LEVEL 14	stub
	LEVEL 13	(CMDPRO)
*	LEVEL 12	(RTP)
*	LEVEL 11	(CTEL)
*	LEVEL 10	(GDUMP)
*	LEVEL 9	(CYCLE, TCNTRL, DFS, CVQS, MODE)

4.10.9.48 XPOPS

An extended version of POPS, written in software, as specified in PS-2303078. Once activated, XPOPS runs on level 16, and performs the following functions:

1. Accepts and executes a limited class of commands.

2. Provides command verification and error messages identical to those provided by flight command and control software.

3. Provides skewed-load protection and checksum verification of the loaded XPOPS.

4. Detects uplink errors.

5. Provides write-protection over itself while it is executing.

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4.11 INSTRUMENTS

4.11.1 ADVANCED VERY HIGH RESOLUTION RADIOMETER

The Advanced Very High Resolution Radiometer (AVHRR/3) is a six channel, cross-track scanning radiometer which produces digital data for each of five spectral intervals. The AVHRR/3 is a single module mounted on the earth-facing side (+x) of the spacecraft Instrument Mounting Platform (IMP). The radiative cooler has an unobstructed hemispherical view of space (-z direction). The outline of the AVHRR/3 is shown in Figure 4.11.1-1. The channel sequence in the data readout is 1,2,4,3,5,6.

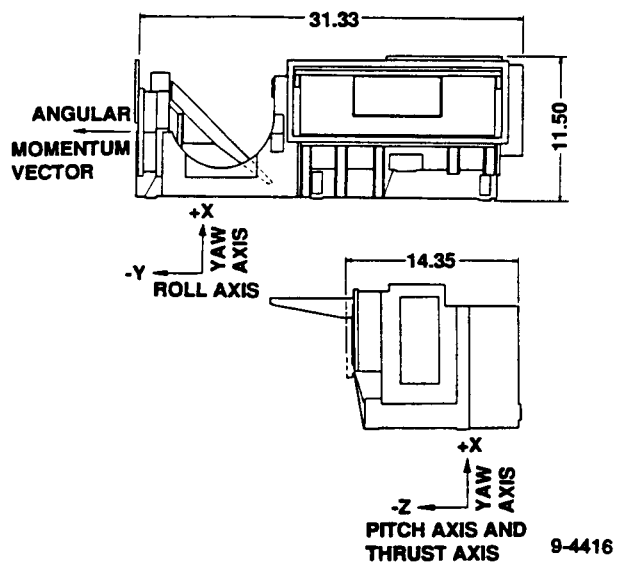

Figure 4.11.1-1. AVHRR/3 Outline Drawing

Silicon photodiodes are used as the detectors in the visible (0.58 to 0.68 micrometers) and near infrared (0.725-1.0, 1.58- 1.64 micrometers) channels (Channel 1, 2, and 3A, respectively). Data from the visible channel is used primarily for cloud, ice, and snow distribution, as well as daytime cloud top temperature and mapping. The near infrared channel provides land/surface water discrimination data.

The AVHRR/3 visible channel past amplifiers incorporate a new design providing dual slope gains. The channel parameters are as follows:

Ch No.	Preamp Output @ 100% Albedo (TYP)	Dual Slope Break-point (% Albedo)	Break-point Ref Voltage	Dual Gain Slope		Zero Radiance Output Voltage	Maximum Radiance Output Voltage
				$<V_{BP}$	$>V_{BP}$		
1	1.199V	25	-0.5245	5.43	1.89	0.25	6.10
2	2.485V	25	-0.7765	3.67	1.28	0.25	6.10
3A	0.61V	12.5	-0.1335	21.3	3.18	0.25	6.10

The infrared channels (channels 3B, 4, and 5) utilize detectors which are cooled to 105°K by the AVHRR/3's passive radiative cooler. An Indium Antimonide detector is used for Channel 3B (3.55-3.93 micrometers). Mercury-Cadmium Telluride detectors are used for Channel 4 (10.3-11.3 micrometers) and Channel 5 (11.5-12.5 micrometers). These channels provide global mapping of sea surface temperatures to an accuracy of 1.5° absolute.

The AVHRR/3's 8-inch entrance aperture and five secondary optical paths produce a square 1.3 milliradian Instantaneous Field of View (IFOV) in each channel. This IFOV is scanned continuously at a 360 RPM rate in a direction perpendicular to the suborbital track. The 0.59 nautical mile (1.1 km) IFOV resolution at the sub-satellite point is designed to provide contiguous ground coverage by adjacent scans. The AVHRR/3 produces radiometric calibration data during two portions of each scan: first when the scan mirrors views space (in the pre-earth scan position) and again when it views an internal blackbody at a known temperature. In addition to the instrument space and blackbody calibration, a ramp calibration voltage is inserted in each line and upon command, simulated earth voltages and calibration target voltages may be inserted in the scan data. See Figure 4.11.1-2 for a simplified block diagram of the AVHRR.

Each of the AVHRR/3's channels is sampled at a 39.936 KHz rate under control of the MIRP. The digital data, composed of 10 bits per sample, is transferred to the MIRP on parallel lines where it becomes the prime constituent of the MIRP's four meteorological data streams: global recorded data, real time high-resolution data, local area coverage data, and real-time medium resolution APT data. The AVHRR/3 additionally provides a once-around synchronization signal to the MIRP. A detailed description of the MIRP data formats for the AVHRR may be found in Section 4.8, Data Handling System.

The general system characteristics of the AVHRR/3 and interfaces between the AVHRR/3 and the spacecraft are described in the Unique Interface Specification for the AVHRR, RCA Drawing No. IS-2280260. A summary of these interface characteristics is shown in Tables 4.11.1-1 through 4.11.1-4.

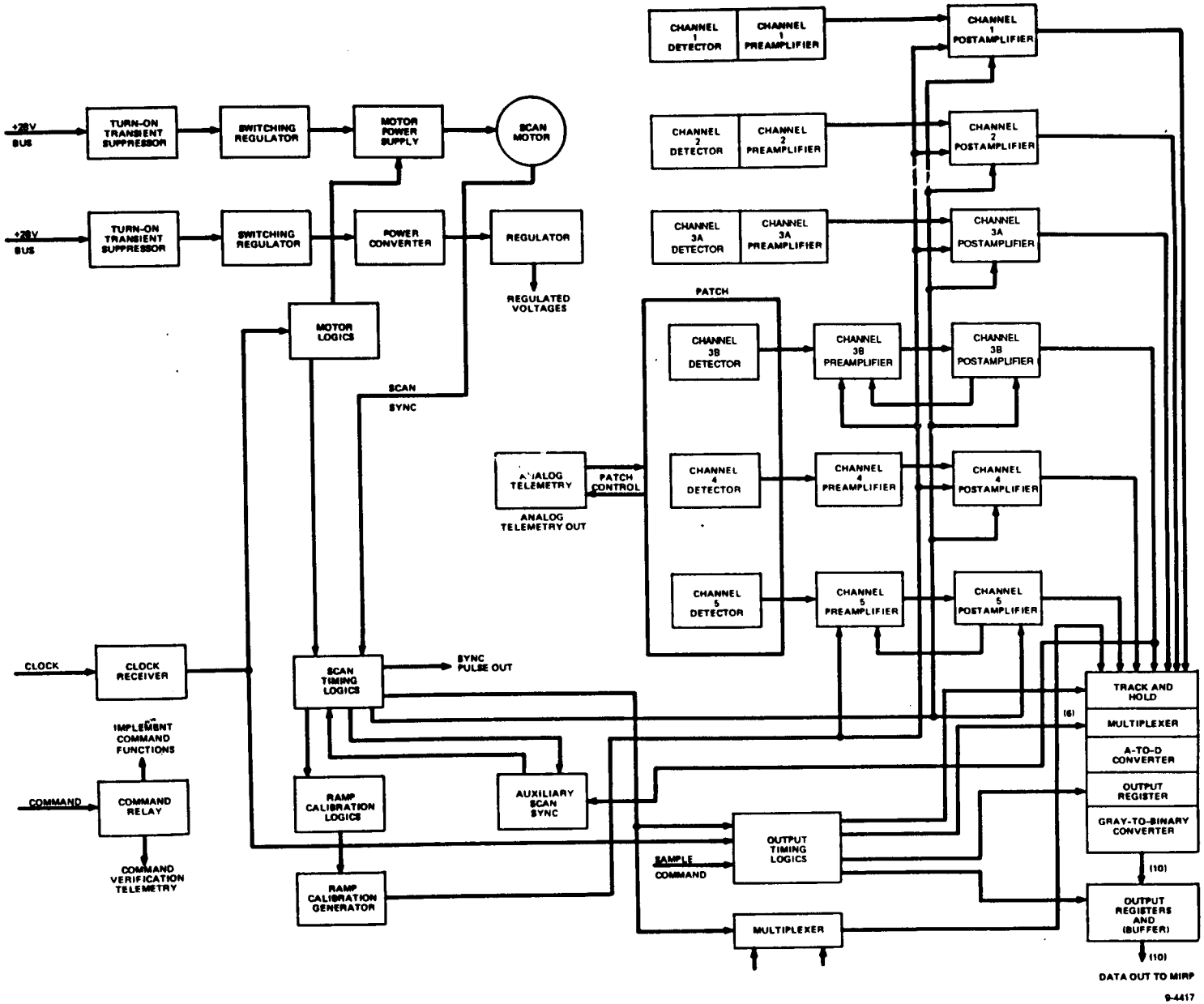

Figure 4.11.1-2. AVHRR/3 Simplified Block Diagram

TABLE 4.11.1-1. AVHRR/3 OPTICAL PARAMETERS

Scan Field of View:	
• Space View	70° to 62.5° from Nadir (in the -z direction)
• Earth View	-62.5° to +55.5° from Nadir
Instantaneous Field of View	1.3×10^{-3} radians (Square)
Aperture Diameter	8 inches
Minimum Clearance Required for Scan Field of View:	
• Cross Track	-75° to 58°
• Orbit Plane	±2.5° about +x axis

Channel Performance Parameters:

	Ch. 1	Ch. 2	Ch. 3A	Ch. 3B	Ch. 4	Ch. 5
Spectral Range (μM)	0.58-0.68	0.725-1.0	1.58-1.64	3.55-3.93	10.3-11.3	11.5-12.5
Resolution (nmi)	0.59	0.59	0.59	0.59	0.59	0.59
Signal to Noise Ratio @ 0.5% Albedo	9:1	9:1	9:1	-	-	-
Noise Equivalent Temp @ 300K	-	-	-	≤ 0.12°K	≤ 0.12°K	≤ 0.13°K
Modulator Transfer Function (1 IFOV/ Single Bar)	> 0.30	> 0.30	> 0.30	> 0.30	> 0.30	> 0.30

TABLE 4.11.1-2. AVHRR/3 ELECTRICAL PARAMETERS

Output Telemetry:	
Science Data	• One 10-bit word for each of 5 AVHRR channels. • Parallel read out of 10-bits • Serial read out of channels • 199,680 words per second
Digital B Telemetry	15 (status indicators)
Analog Telemetry	22 (temperature and voltage values)
Power (orbit average)	
+28 Volt Main Bus	28.2 W - normal operation 30.4 W - decontamination phase (1 week)
+10 Volt Interface Bus	10 mW
Power Converter Frequency	TBD
Input Signals:	
Commands - Pulse - Level	28 0
Clock Signals	
MIRP 0.9984 MHz	AVHRR Specific
MIRP Data Sample Pulse	AVHRR Specific

TABLE 4.11.1-3. AVHRR/3 MECHANICAL PARAMETERS

Outline Drawing	ITT Drawing No. 8150176
Number of Modules	1
Weight	65 pounds-maximum
Size*	
Cooler Door Stowed	11.25 x 30.33 x 14.35 in.
Cooler Door Deployed	11.25 x 30.33 x 19.2 in.
Uncompensated Momentum	38 in-oz-sec, ccw, -z to +z
*X x Y x Z	

TABLE 4.11.1-4. AVHRR/3 THERMAL PARAMETERS

Thermal Interface Drawing	ITT Drawing No. 8123499, Rev. E
Normal Operating Temperature (measured at baseplate)	+15°C
Operating Temperature Range (measured at baseplate)	+10°C to +30°C
TCE - Louver Set Point - Heater Set Point - Heater Power	+15 ±1°C +13°C TBD
Temperature Control Method	Radiation to space via louvers
Heat exchanged with S/C	AVHRR is hard mounted to the IMP but no heat flow is anticipated as AVHRR and IMP are both controlled to +15°C

4.11.2 HIGH RESOLUTION INFRARED RADIATION SOUNDER

The High Resolution Infrared Radiation Sounder (HIRS/3) is a 20 spectral channel radiometer with the capacity of step scaning across the satellite subpoint track. The radiance measurements of the HIRS/3 permit calculation of a vertical temperature profile from the earth's surface to about 40 km (130,000 feet).

The HIRS/3 makes a temperature sounding in both the 15 micrometer carbon dioxide band and in the 4.3 micrometer carbon dioxide/nitrous oxide band. The 4.3 micrometer band channels provide better sensitivity to the temperature of the relatively warm regions of the atmosphere than is achieved with the 15 micrometer band channels. Also, the short-wave radiances are less sensitive to clouds than those of the 15 micrometer region. There is also a 0.69 micrometer visible channel for cloud detection. The water vapor soundings are made in the 6.7 micrometer band. A single channel at 9.7 micrometers is used to sense ozone concentration.

The cross track scanning is $\pm$49.5 degrees each side of the nadir. The scan consists of 56 discrete steps incremented at 1.8 degrees per step. The HIRS/3 Instantaneous Field of View (IFOV) is 1.4 degrees at the half power points. The scan period is 6.4 seconds, including 0.8 seconds for retrace.

The calibration sequence consists of a space view and a view of two internal calibration targets. Each space and internal target view is sampled 56 times per channel during each calibration period; the timing and integration periods of each spectral filter are the same as those normally used for measurement of the earth radiances. A calibration sequence is initiated every 256 seconds.

A single telescope is used to gather the energy from the scene. Spectral selectivity is achieved by a spinning filter wheel containing the 20 filters. A radiant cooled mercury cadmium telluride detector is used for the long wavelength channels. The shorter wavelength infrared channels are sensed by a cooled indium antimonide detector. The visible channel uses a silicon photodetector.

The radiometric signals from the 20 spectral regions are digitized to a 13-bit level. The twenty 13-bit radiometric samples and some identification information are packaged into eighteen 16-bit words for each step of earth view, and transferred to the TIP every 0.1 second. During the 0.8 second of retrace the data output format is changed to transmit related housekeeping voltages and instrument temperatures. The HIRS/3 functional block diagram is shown in Figure 4.11.2-1.

The HIRS/3 is a single module mounted on the earth-facing (+x) side of the IMP. The radiative cooler has an unobstructive view of space (-z direction). The outline of the HIRS/3 is shown in Figure 4.11.2-2.

The general system characteristics of the HIRS/3 and interfaces between the HIRS/3 and the spacecraft are described in the TIROS-N Unique Interface Specification for the HIRS/2, RCA Drawing No. IS-2285780. A summary of these characteristics is given in Tables 4.11.2-1 through 4.11.2-4.

4.11.2 HIGH RESOLUTION INFRARED RADIATION SOUNDER

The High Resolution Infrared Radiation Sounder (HIRS/3) is a 20 spectral channel radiometer with the capacity of step scaning across the satellite subpoint track. The radiance measurements of the HIRS/3 permit calculation of a vertical temperature profile from the earth's surface to about 40 km (130,000 feet).

The HIRS/3 makes a temperature sounding in both the 15 micrometer carbon dioxide band and in the 4.3 micrometer carbon dioxide/nitrous oxide band. The 4.3 micrometer band channels provide better sensitivity to the temperature of the relatively warm regions of the atmosphere than is achieved with the 15 micrometer band channels. Also, the short-wave radiances are less sensitive to clouds than those of the 15 micrometer region. There is also a 0.69 micrometer visible channel for cloud detection. The water vapor soundings are made in the 6.7 micrometer band. A single channel at 9.7 micrometers is used to sense ozone concentration.

The cross track scanning is $\pm$49.5 degrees each side of the nadir. The scan consists of 56 discrete steps incremented at 1.8 degrees per step. The HIRS/3 Instantaneous Field of View (IFOV) is 1.4 degrees at the half power points. The scan period is 6.4 seconds, including 0.8 seconds for retrace.

The calibration sequence consists of a space view and a view of two internal calibration targets. Each space and internal target view is sampled 56 times per channel during each calibration period; the timing and integration periods of each spectral filter are the same as those normally used for measurement of the earth radiances. A calibration sequence is initiated every 256 seconds.

A single telescope is used to gather the energy from the scene. Spectral selectivity is achieved by a spinning filter wheel containing the 20 filters. A radiant cooled mercury cadmium telluride detector is used for the long wavelength channels. The shorter wavelength infrared channels are sensed by a cooled indium antimonide detector. The visible channel uses a silicon photodetector.

The radiometric signals from the 20 spectral regions are digitized to a 13-bit level. The twenty 13-bit radiometric samples and some identification information are packaged into eighteen 16-bit words for each step of earth view, and transferred to the TIP every 0.1 second. During the 0.8 second of retrace the data output format is changed to transmit related housekeeping voltages and instrument temperatures. The HIRS/3 functional block diagram is shown in Figure 4.11.2-1.

The HIRS/3 is a single module mounted on the earth-facing (+x) side of the IMP. The radiative cooler has an unobstructive view of space (-z direction). The outline of the HIRS/3 is shown in Figure 4.11.2-2.

The general system characteristics of the HIRS/3 and interfaces between the HIRS/3 and the spacecraft are described in the TIROS-N Unique Interface Specification for the HIRS/2, RCA Drawing No. IS-2285780. A summary of these characteristics is given in Tables 4.11.2-1 through 4.11.2-4.

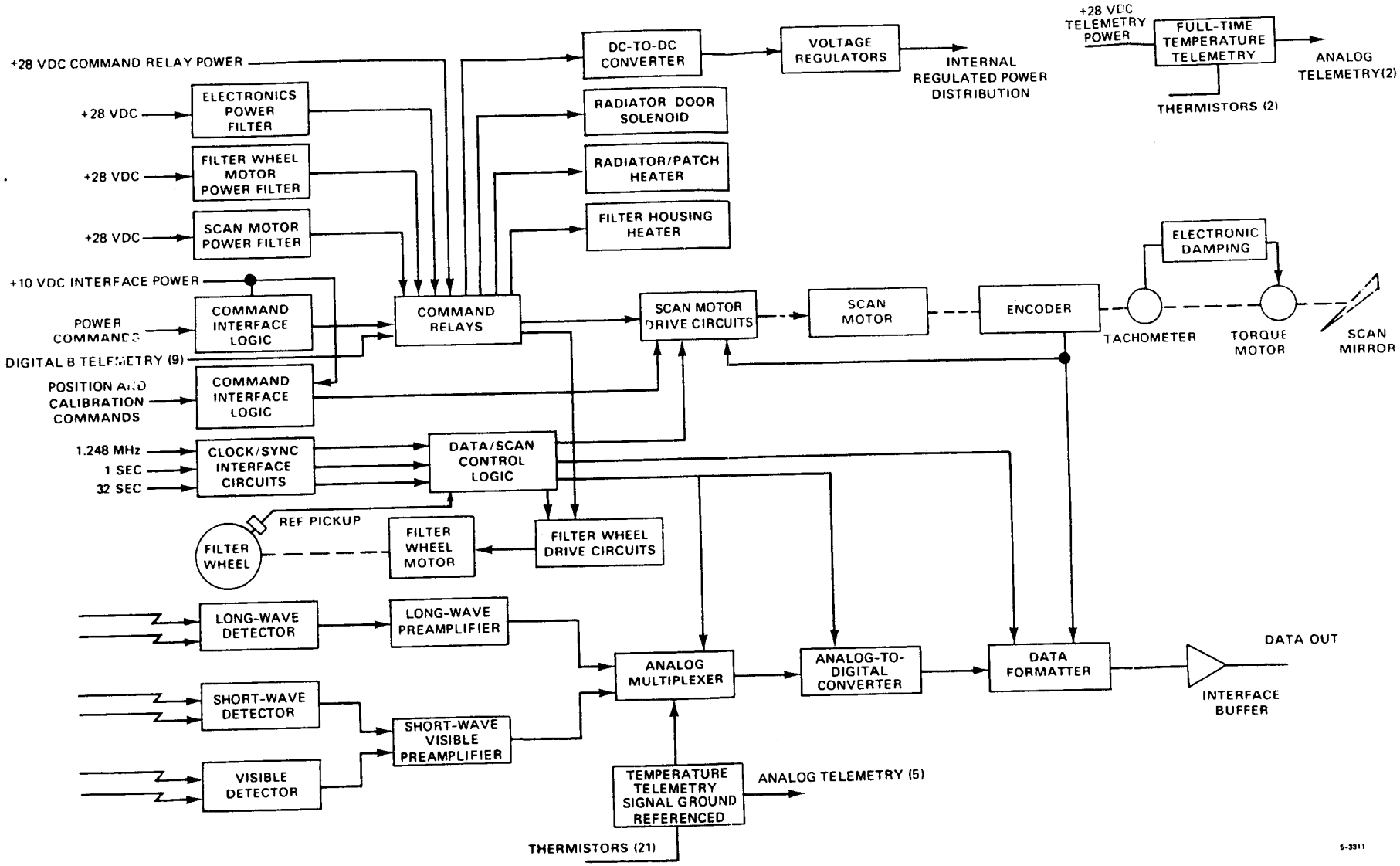

Figure 4.11.2-1. HIRS/3 Functional Block Diagram

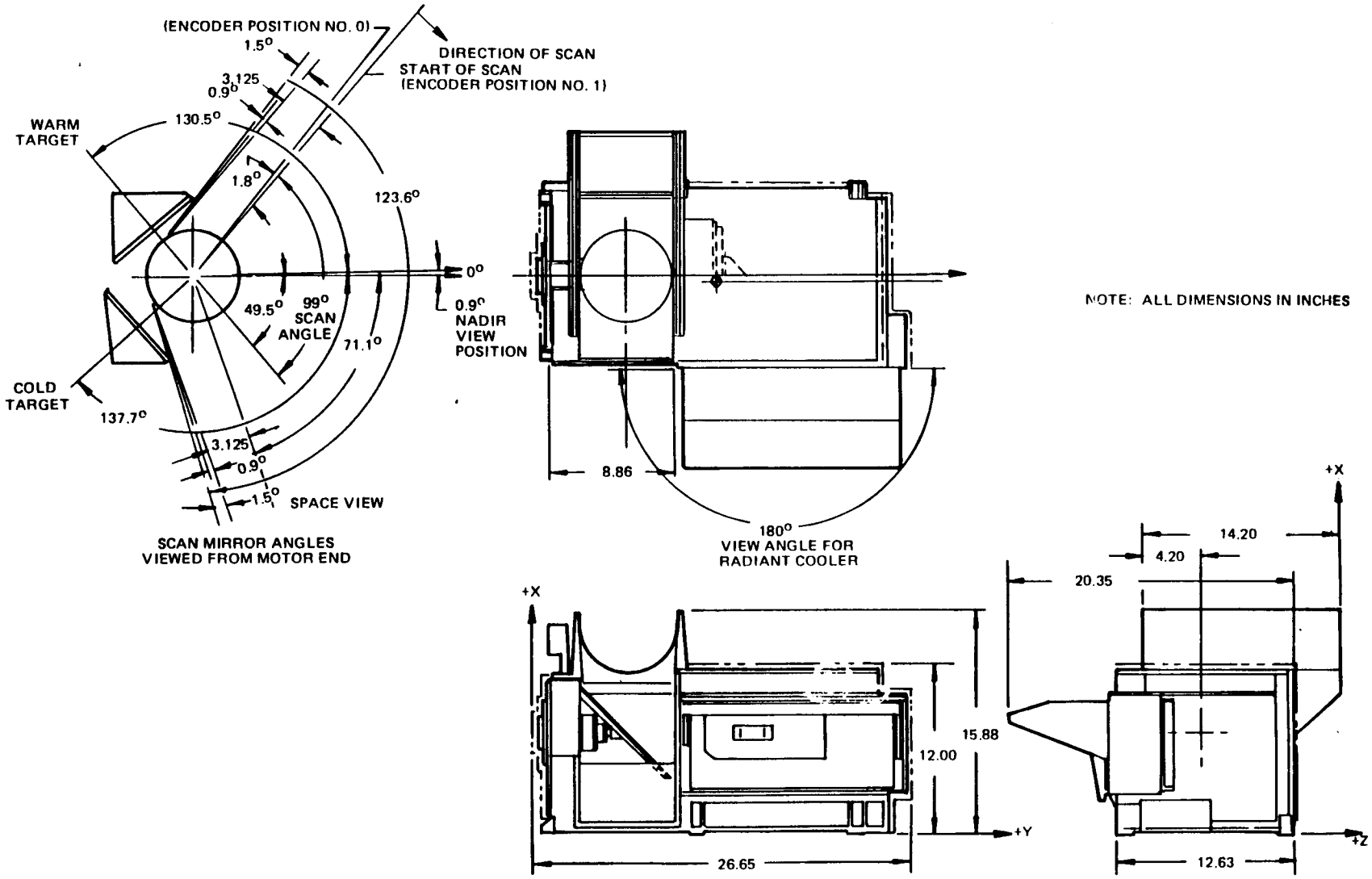

Figure 4.11.2-2. HIRS/3 Outline Drawing

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TABLE 4.11.2-1. HIRS/3 OPTICAL PARAMETERS

Earth Scan Field of View	±49.5° from Nadir
Space Calibration Position	71.1° from Nadir (in the -z direction)
Instantaneous Field of View	1.4°
Aperture Diameter	6 inches
Steps per Earth Scan Line	56

Channel Spectral Parameters:

Channel Number	Channel Frequency (cm^{-1})	Spectral Range (μm)	Half Power Bandwidth (cm^{-1})	NEΔN (Spec.)
1	669	14.95	3	3.00
2	680	14.71	10	0.67
3	690	14.49	12	0.50
4	703	14.22	16	0.31
5	716	13.97	16	0.21
6	733	13.64	16	0.24
7	749	13.35	16	0.20
8	900	11.11	35	0.10
9	1030	9.71	25	0.15
10	802	8.16	16	0.16
11	1365	7.33	40	0.20
12	1533	6.72	55	0.19
13	2188	4.57	23	0.006
14	2210	4.52	23	0.003
15	2235	4.46	23	0.004
16	2245	4.40	23	0.002
17	2240	4.24	28	0.002
18	2515	4.00	35	0.002
19	2660	3.76	100	0.001
20	14500	0.69	1000	0.1%

TABLE 4.11.2-2. HIRS/3 ELECTRICAL PARAMETERS

Output Telemetry	
Digital A Telemetry	64 elements per 6.4 seconds (status words, radiance data for 20 channels, housekeeping telemetry)
Digital B Telemetry	14 (status indicators)
Analog Telemetry	16 (temperature, voltage, current, and power values)
Power (Orbit Average)	
+28 Volt Main Bus	7.9W
+28 Volt Pulse Load Bus	14.6W - normal operation 27.0W - outgas heater on
+28 Volt Telemetry Bus	0.03W
+10 Volt Interface Bus	0.1W
Power Converter Frequency	78 kHz
Input Signals	
Commands	
- Pulse	26
- Level	0
Clock Signals	
- 1.248 MHz	
- 1.0 Hz	
Sync. Signals	
- 32 sec	
- 256 sec	
A_1 Data Enable Pulse	
C_1 Data Clock (8320 pps.)	

TABLE 4.11.2-3. HIRS/3 MECHANICAL PARAMETERS

Outline/Interface Control Drawing	8129882
Number of Modules	1
Weight	73 pounds - maximum
Size*	13.06 x 26.65 x 20.35 in.**

* X x Y x Z
** With cooler door open

TABLE 4.11.2-4. HIRS/3 THERMAL PARAMETERS

Thermal Interface Drawing	8121519
Operating Temperature (measured at baseplate)	+15°C
Operating Temperature Range (measured at baseplate)	+5 to +25°C
TCE - Louver Set Point - Heater Set Point - Heater Power	+15 ±1°C +13°C 24W
Temperature Control Method	Radiation to space via louvers
Heat exchanged with S/C	None

4.11.3 ADVANCED MICROWAVE SOUNDING UNIT

The Advanced Microwave Sounding Unit (AMSU) is a 20-channel microwave radiometer. The AMSU, together with the HIRS/3, will constitute the operational sounder package. The primary mission objective of the AMSU is to obtain global temperature and humidity profile data. The AMSU is comprised of three separate units: AMSU-A1, AMSU-A2, and AMSU-B. The AMSU channel breakdown is as follows: A1 - channels 3 through 14; A2 - channels 1 and 2; B - channels 16 through 20.

AMSU channels 3 through 14 use the 50 to 60 GHz oxygen band to provide data for a vertical temperature profile of the atmosphere up to 50 km. The "window" channels (1, 2, 15, and 16) provide data that will enhance the temperature sounding by correcting for the surface emissivity, atmospheric liquid water, and total precipitable water. Channels 17 through 20 use the 183.3 GHz water vapor absorption line to provide data for the humidity profile.

4.11.3.1 AMSU-A1

The AMSU-A1 instrument has two 6-inch diameter antennas, each having a 3.3 degree nominal field-of-view at the half power points. Each antenna provides a crosstrack scan ±48.33 degrees from Nadir with a total of 30 earth fields-of-view per scan line. In-orbit calibration will be performed using the internal warm loads and cold space. The total scan period is 8 seconds.

The AMSU-A1 functional block diagram is shown in Figure 4.11.3-1 and the outline of the instrument is shown in Figure 4.11.3-2. Additional information on the AMSU-A1 is provided in Tables 4.11.3-1 through 4.11.3-4.

4.11.3.2 AMSU-A2

The AMSU-A2 instrument has an 11-inch diameter antenna, which has a 3.3 degree nominal field-of-view at the half power points. The antenna provides a crosstrack scan ±48.33 degrees from Nadir with a total of 30 earth fields of view per scan line. In-orbit calibration will be performed using the internal warm load and cold space. The total scan period is 8 seconds.

The AMSU-A2 functional block diagram is shown in Figure 4.11.3-3 and the outline of the instrument is shown in Figure 4.11.3-4. Additional information on the AMSU-A2 is provided in Tables 4.11.3-5 through 4.11.3-8.

4.11.3.3 AMSU-B

The AMSU-B instrument has a 12-inch diameter antenna which has a 1.1 degree instantaneous field of view. The antenna provides a crosstrack scan ±49.50 degrees from Nadir with a total of 90 earth fields of view per scan line. In-orbit calibration will be performed using an internal warm load and cold space. The total scan period is 8/3 seconds.

The AMSU-B functional block diagram is shown in Figure 4.11.3-5 and the outline of the instrument is shown in Figure 4.11.3-6. Additional information on the AMSU-B is provided in Tables 4.11.3-9 through 4.11.3-12.

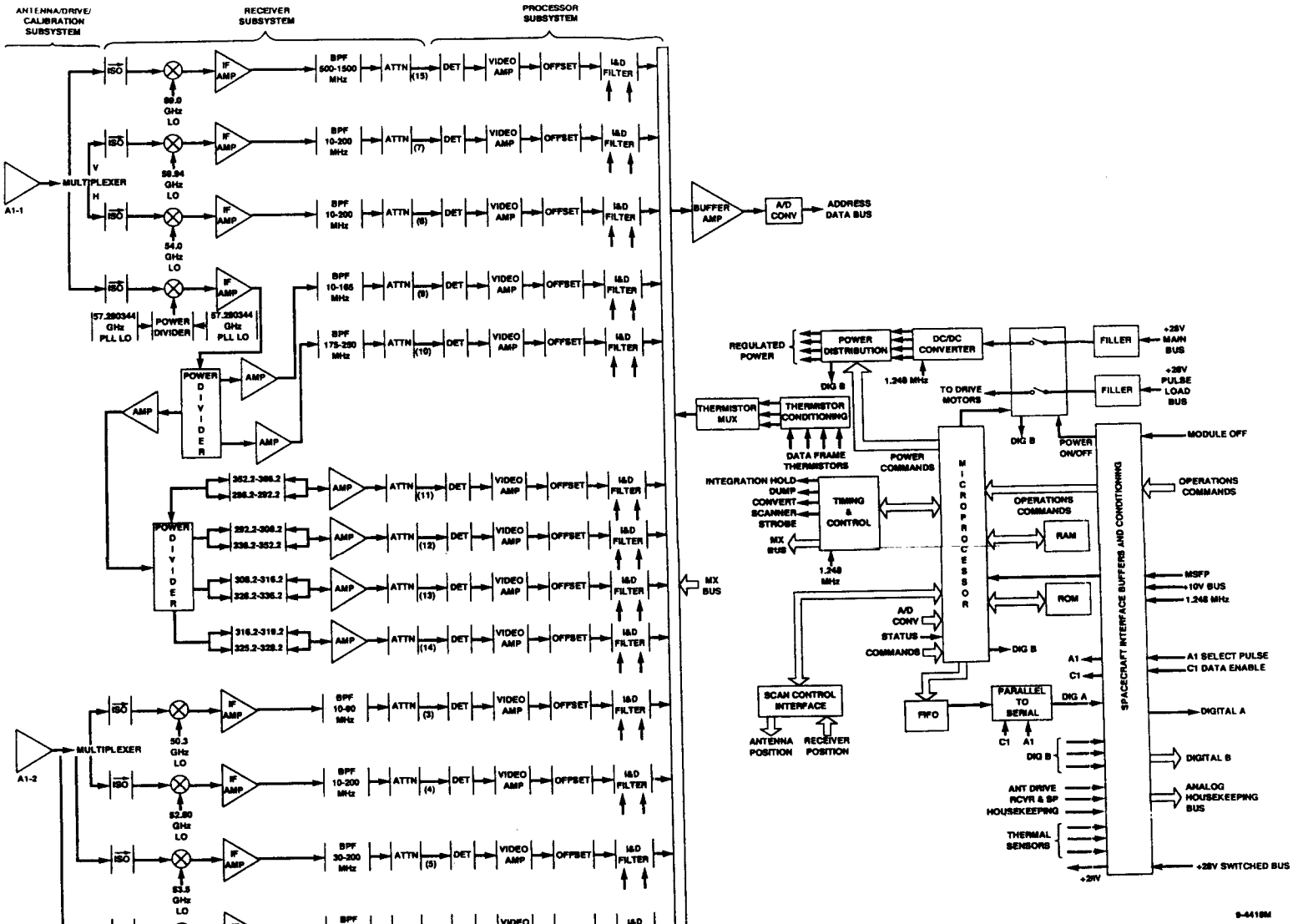

Figure 4.11.3-1. AMSU-A1 Functional Block Diagram

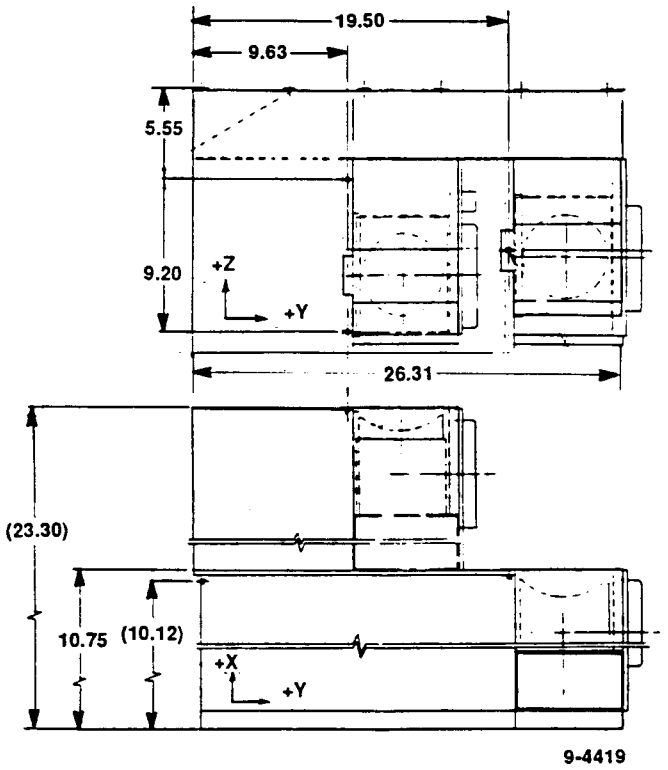

Figure 4.11.3-2. AMSU-A1 Outline Drawing

TABLE 4.11.3-1. AMSU-A1 OPTICAL PARAMETERS

Earth Scan Field of View	±48.33° from Nadir
Space Calibration Position	84° from Nadir (in the -Z direction)
Instantaneous Field of View	3.3° at half power points
Steps per Scan Line	30 Earth Viewing 1 Space Viewing 1 Internal Warm Load Viewing

Channel Spectral Parameters:

Channel Number	Central Frequency (GHz)	Bandwidth (MHz)	Sensitivity NEΔT (°K)
3	50.300	180	0.4
4	52.800	400	0.25
5	53.596	170	0.25
6	54.400	400	0.25
7	54.940	400	0.25
8	55.500	330	0.25
9	57.290	330	0.25
10	57.290 ±.217	78	0.4
11	57.290 ±.048	36	0.4
12	57.290 ±.022	16	0.6
13	57.290 ±.010	8	0.80
14	57.290 ±.0045	3	1.20
15	89.0	6000	0.5

TABLE 4.11.3-2. AMSU-A1 ELECTRICAL PARAMETERS

Output Telemetry:	
Digital A Telemetry	Thirteen 16-bit words per AIP minor frame
Digital B Telemetry	11 (status indicators)
Analog Telemetry	27 (temperatures and voltages)
Power (Orbit Average):	
+28 Volt Main Bus	82.0 watts
+28 Volt Pulse Load Bus	6.0 watts
+28 Volt Telemetry Bus	0.2 watts
+10 Volt Interface Bus	0.1 watts
Power Converter Frequency	78 kHz
Input Signals:	
Commands - Pulse	4
- Level	10
Clock Signals - 1.248 MHz	
Sync Signals - 8 sec	
A_1 Data Enable Pulse C_1 Data Clock	

TABLE 4.11.3-3. AMSU-A1 MECHANICAL PARAMETERS

Interface Control Drawing	Aerojet Drawing No. 1333964
Number of Modules	1
Weight	112.0 pounds (maximum)
Size*	23.8 x 28.8 x 16.1 in.
* X x Y x Z	

TABLE 4.11.3-4. AMSU-A1 THERMAL PARAMETERS

Interface Control Drawing	Aerojet Drawing No. 1333964
Normal Operating Temperature (measured at baseplate)	TBD
Operating Temperature Range (measured at baseplate)	TBD
Thermal Control Components	Surface Finishes and Radiators Survival Heaters

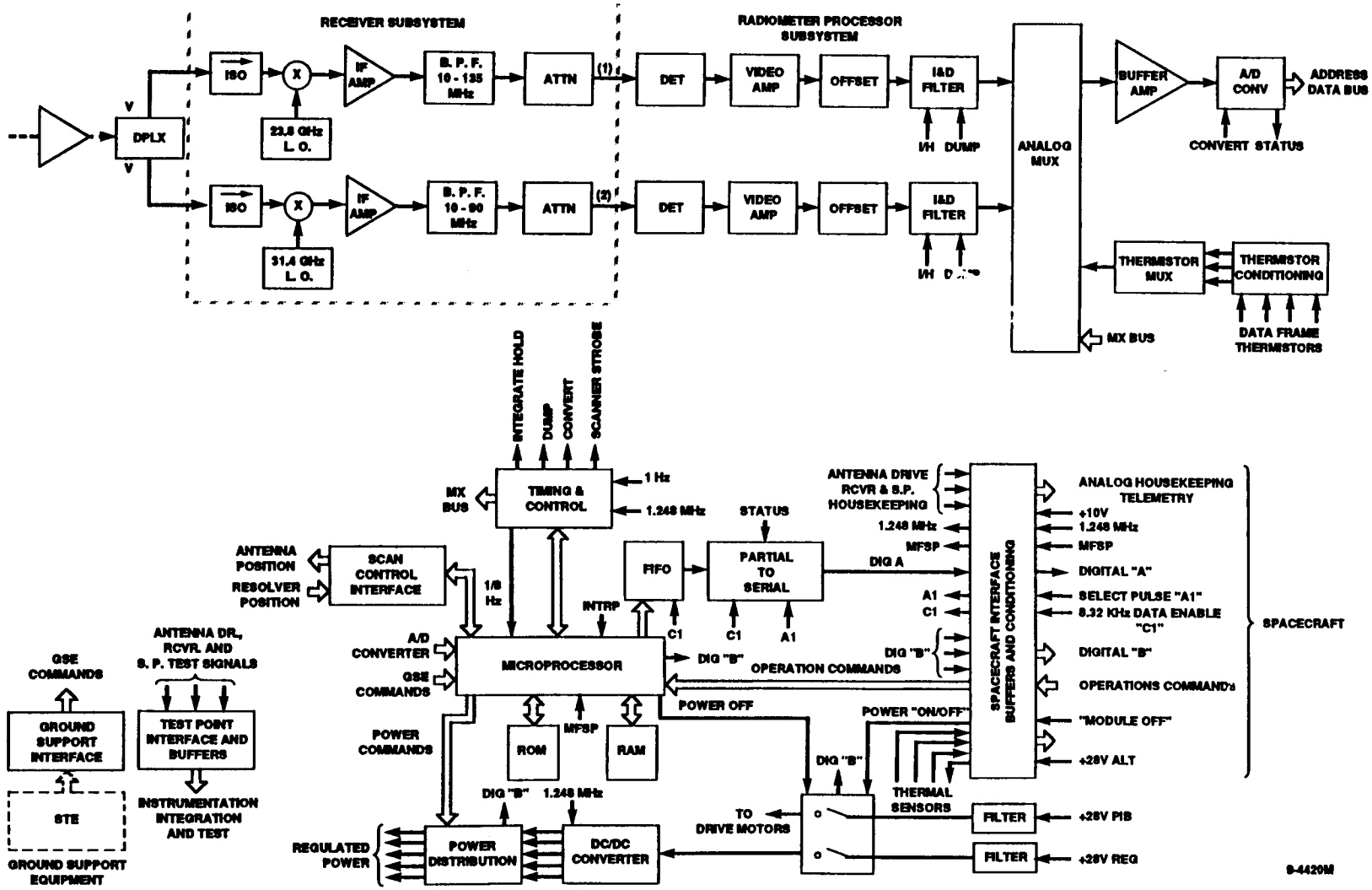

Figure 4.11.3-3. AMSU-A2 Functional Block Diagram

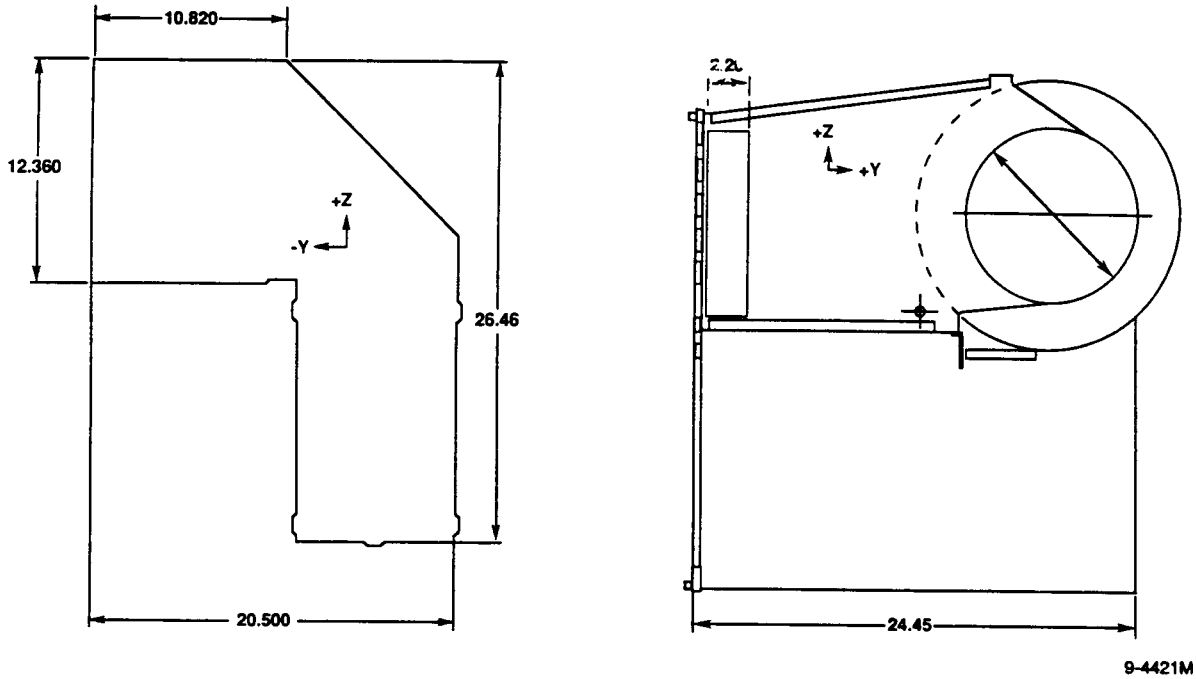

Figure 4.11.3-4. AMSU-A2 Outline Drawing

TABLE 4.11.3-5. AMSU-A2 OPTICAL PARAMETERS

Earth Scan Field of View	±48.33° from Nadir
Space Calibration Position	84° from Nadir (in the -Z direction)
Instantaneous Field of View	3.3° at half power points
Steps per Scan Line	30 Earth Viewing 1 Space Viewing 1 Internal Warm Load Viewing

Channel Spectral Parameters:

Channel Number	Central Frequency (GHz)	Bandwidth (MHz)	Sensitivity NEΔT (°K)
1	23.800	270	0.3
2	31.400	180	0.3

TABLE 4.11.3-6. AMSU-A2 ELECTRICAL PARAMETERS

Output Telemetry:	
Digital A Telemetry	Seven 16-bit words per AIP minor frame
Digital B Telemetry	10 (status indicators)
Analog Telemetry	15 (temperatures and voltages)
Power (Orbit Average):	
+28 Volt Main Bus	25.0 watts
+28 Volt Pulse Load Bus	12.0 watts
+28 Volt Telemetry Bus	0.15 watts
+10 Volt Interface Bus	0.10 watts
Power Converter Frequency	78 kHz
Input Signals:	
Commands - Pulse - Level	4 9
Clock Signals - 1.248 MHz	
Sync Signals - 8 sec	
A_1 Data Enable Pulse C_1 Data Clock	

TABLE 4.11.3-7. AMSU-A2 MECHANICAL PARAMETERS

Interface Control Drawing	Aerojet Drawing No. 1333965
Number of Modules	1
Weight	110.0 pounds (maximum)
Size*	27.5 x 20.5 x 26.7 in.
* X x Y x Z	

TABLE 4.11.3-8. AMSU-A2 THERMAL PARAMETERS

Interface Control Drawing	Aerojet Drawing No. 1333965
Normal Operating Temperature (measured at baseplate)	TBD
Operating Temperature Range (measured at baseplate)	TBD
Thermal Control Components	Surface Finishes and Radiators Survival Heaters

TBD

Figure 4.11.3-5. AMSU-B Functional Block Diagram

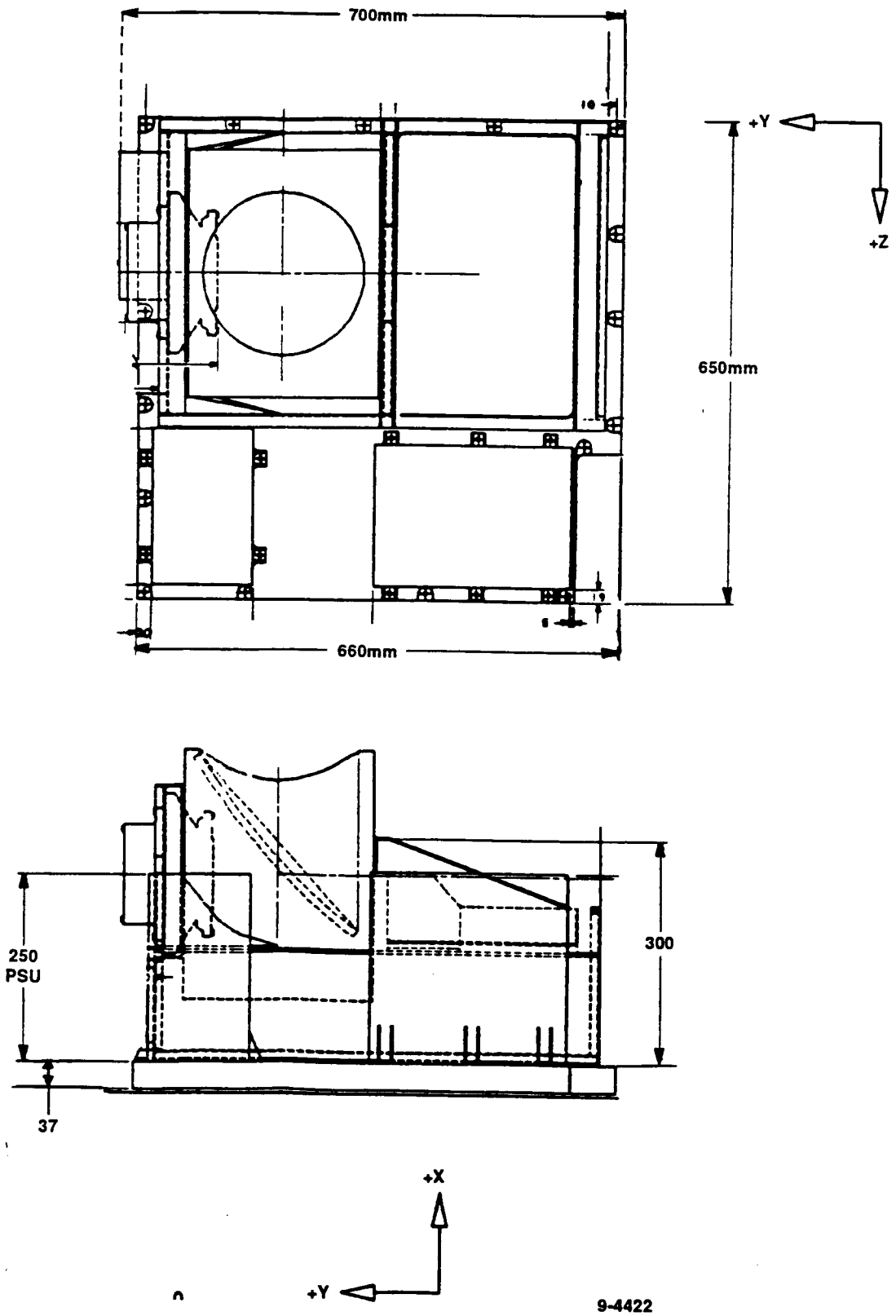

Figure 4.11.3-6. AMSU-B Outline Drawing

TABLE 4.11.3-9. AMSU-B OPTICAL PARAMETERS

Earth Scan Field of View	±49.50° from Nadir
Space Calibration Position	84° from Nadir (in the -Z direction)
Instantaneous Field of View	1.1°
Steps per Scan Line	90 Earth Viewing 1 Space Viewing 1 Internal Warm Load Viewing

Channel Spectral Parameters:

Channel Number	Central Frequency (GHz)	Bandwidth (MHz)	Sensitivity NEΔT (°K)
16	89.0	6000	1.0
17	166.0	4000	1.00
18	183.31 ±1.00	1000	1.00
19	183.31 ±3.00	2000	1.0
20	183.31 ±7.00	4000	1.20

TABLE 4.11.3-10. AMSU-B ELECTRICAL PARAMETERS

Output Telemetry:	
Digital Telemetry	Twenty-five 16-bit words per AIP minor frame
Digital B Telemetry	16 (status indicators)
Analog Telemetry	24 (voltages, temperatures, currents)
Power (Orbit Average): (NOTE:	Total Power = 90.0 Watts - maximum)
+28 Volt Main Bus	TBD
+28 Volt Pulse Load Bus	TBD
+28 Volt Telemetry Bus	TBD
+10 Volt Interface Bus	TBD
Power Converter Frequency	78 kHz
Input Signals:	
Commands - Pulse	10
- Level	3
Clock Signals - 1.248 MHz	
Sync Signals - 8 sec	
Data Enable Pulse Data Clock	

TABLE 4.11.3-11. AMSU-B MECHANICAL PARAMETERS

Interface Control Drawing	TBD
Number of Modules	1
Weight	136.4 pounds (maximum)
Size*	300 mm x 700 mm x 650 mm
*X x Y x Z	

TABLE 4.11.3-12. AMSU-B THERMAL PARAMETERS

Interface Control Drawing	British Aerospace Drawing No. CPL 066
Normal Operating Temperature (measured at baseplate)	TBD
Operating Temperature Range (measured at baseplate)	TBD
Thermal Control Components	TBD

4.11.4 DATA COLLECTION AND PLATFORM LOCATION SYSTEM

The Data Collection and Platform Location System (DCS-2) is a random-access system that provides a means for locating and/or collecting data from remote fixed and free-floating terrestial and atmospheric platforms. Location information is determined by using a differential Doppler measurement technique on the carrier frequencies of the signals transmitted by the platform. The data collected from each platform includes identification and meteorological information. Information derived by the DCS is transferred to the spacecraft TIP and transmitted to earth for additional ground data processing.

The spacecraft portion of the DCS includes four units: a receiver/power unit, two signal processing units, and a UHF collection antenna (designated UDA). Data from the platforms is transmitted to the DCS at a nominal frequency of 401.65 MHz, in the form of bilevel digital data at approximately 400 bps. The receiver intermediate frequency output is swept by the search unit and when the signal threshold is exceeded the search unit data is output to one of eight processing channels called Data Recovery Units (DRU). The data processing unit reformats the sensor data with other internally generated data and adds the Doppler information. The resulting output data stream is then transferred to the TIP in the form of 8 bit words at an average rate of 2560 bps. The DCS additionally has provision to identify jammers in the DCS band through the process of generating pseudo-messages and an anti-jammer algorithm to minimize messages lost due to interfering signals. See Figure 4.11.4-1 for a simplified block diagram of the DCS.

The antenna is a 1-1/2 turn, 1-1/4 wavelength quadrifilar which has a circularly polarized pattern with a maximum gain of +3.5 dBli at the earth's horizon (63° off axis). See Section 4.7 for details of the DCS/SARP antenna.

The three DCS electronic modules are mounted on the inside of the Equipment Support Module (ESM) Panel No. 1 and the UDA antenna is mounted on the outside of Panel No. 1. The outlines of the DCS modules are shown in Figures 4.11.4-2 and 4.11.4-3.

The general system characteristics of the DCS and interfaces between the DCS and the spacecraft are fully described in the Unique Interface Specification for the DCS, RCA Drawing No. IS-3267402. A summary of these interface characteristics are shown in Tables 4.11.4-1 through 4.11.4-4.

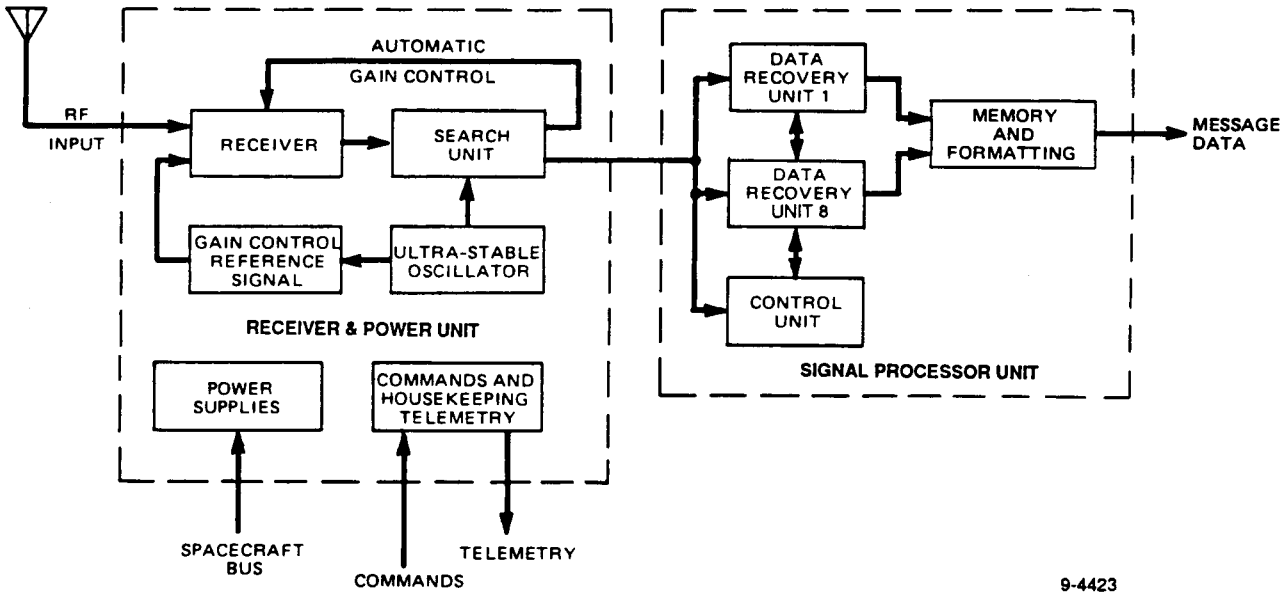

Figure 4.11.4-1. DCS-2 Simplified Block Diagram

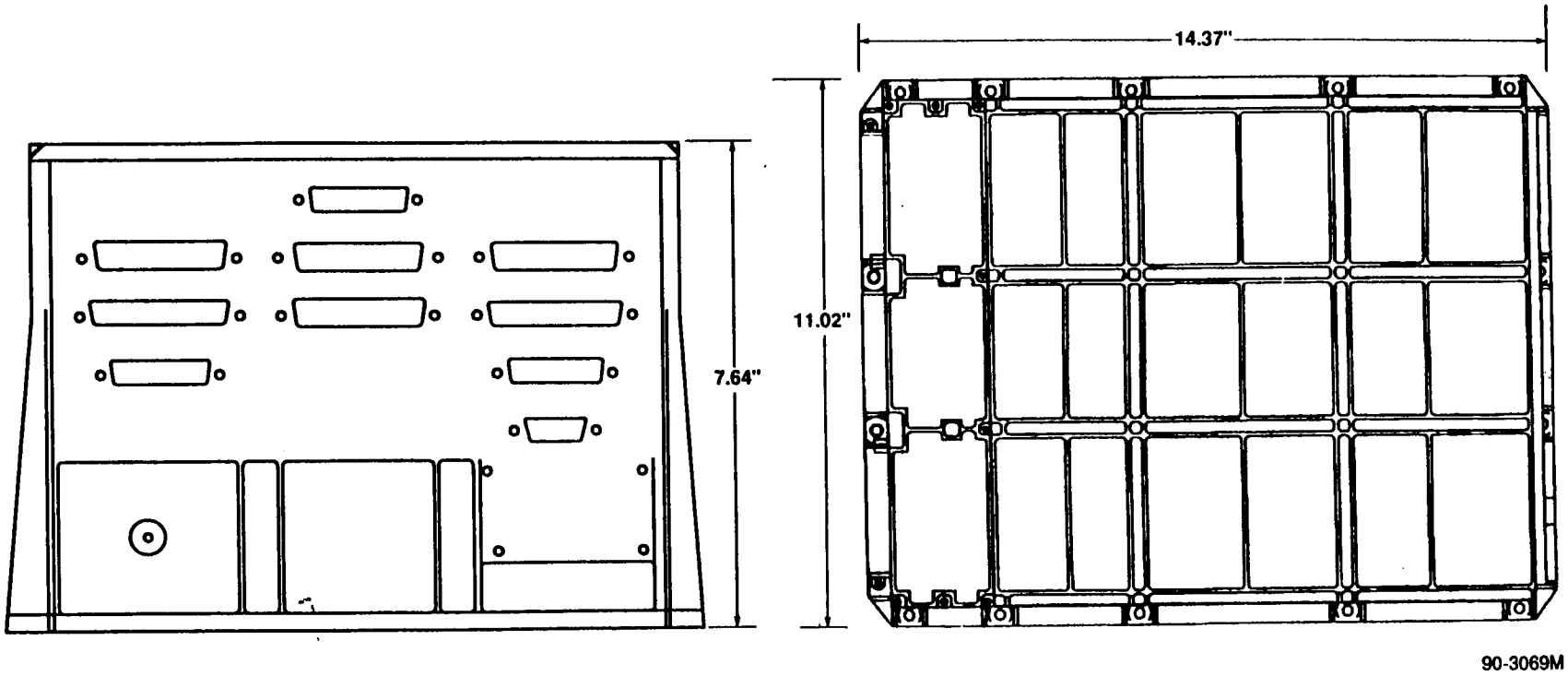

Figure 4.11.4-2. DCS-2 RPU Outline Drawing

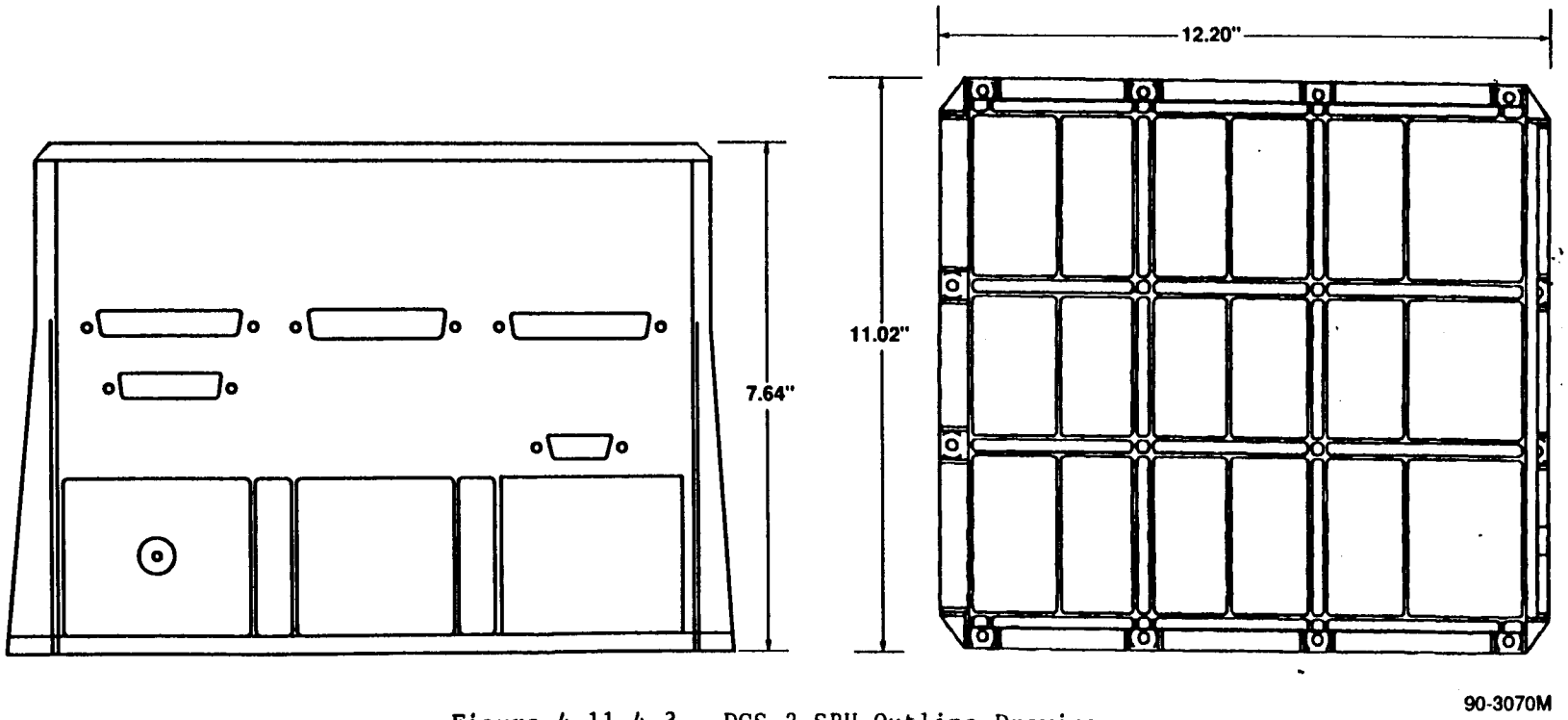

Figure 4.11.4-3. DCS-2 SPU Outline Drawing

TABLE 4.11.4-1. DCS-2 SYSTEM PARAMETERS

Receiver:	
• Frequency	401.650 ±40 KHz
• Sensitivity	-108 to -131 dBm
• Dynamic Range	23 dBm
• Noise Factor	≤ 3 dB
DRUs	8
Message Content:	Synchronization Signal Level Time of Message ID of Incoming Information Sensor Information Doppler Counting
Antenna:	
• Half Cone Angle	63°
• Polarization	Right Circular
• Gain at 63°	+3.5 dBli maximum
• VSWR	< 1.5:1

TABLE 4.11.4-2. DCS-2 ELECTRICAL PARAMETERS

Output Telemetry		
Digital A Telemetry	- 32 8-bit TIP words per minor frame - 1 DCS word equals 1 TIP word	
Digital B Telemetry	13 (status indicator)	
Analog Telemetry	10 (temperature and voltage levels)	
Power (Orbit Average)	RPU	SPU*
+28 Volt Main Bus	15.35W	11.12W
+28 Volt Telemetry Bus	TBD	----
+10 Volt Interface Bus	10 mW	Not Used
Power Converter Frequency	80.418 kHz	
Input Signals		
Commands - Pulse - Level	23 0	
Clock Signals	TIP A_1 Data Enable Pulse TIP C_1 Data Clock (8320 pps.)	
Sync. Signals	TIP 32 Sec Frame Sync	

*2 Units, SPU-A & SPU-B are identical

TABLE 4.11.4-3. DCS-2 MECHANICAL PARAMETERS

	(RPU) Receiver & Power Unit	(SPU-A, -B)* Signal Processing Unit
Mechanical Interface Control Dwg.	8212-200E 380/02	8212-300E 380/01
Number of Modules	1	2
Weight	30.64 lbs.	26.0 lbs. (each)
Size**	14.4 x 11.0 x 7.7 in.	12.2 x 11.0 x 7.7 in.

*SPU-A and -B are identical units
**X x Y x Z

TABLE 4.11.4-4. DCS-2 THERMAL PARAMETERS

Thermal ICD	TBD
Normal Operating Temperature	+20°C
Operating Temperature Range	-5° to +45°C
Temperature Control Method	Conduction to the ESM panel heat sinks
Total System Thermal Dissipation	TBD

4.11.5 SPACE ENVIRONMENT MONITOR

The Space Environment Monitor (SEM) is a multichannel charged-particle spectrometer which provides measurements on the population of the earth's radiation belts and on particle precipitation phenomena resulting from solar activity (both of which contribute to the solar-terrestrial energy interchange). The SEM consists of two separate sensor units and a common Data Processing Unit (DPU). The sensor units are the Total Energy Detector (TED) and the Medium Energy Proton and Electron Detector (MEPED). It should be noted that the lower-energy sensors (the TED, plus the proton and electron telescopes of the MEPED) have pairs of sensors with different orientations. This is because the direction of the particle fluxes is important in characterizing the energy interchanges taking place. See Figures 4.11.5-1 through 4.11.5-3 for the TED, MEPED and DPU block diagrams.

4.11.5.1 Total Energy Detector

TBD

4.11.5.2 Medium Energy Proton Electron Detector

TBD

4.11.5.3 Data Processing Unit

TBD

4.11.5.4 SEM Component Location

The SEM components are distributed about the spacecraft in order to satisfy their individual field of view requirements. The DPU is mounted on the inside of the ESM Panel #1. The MEPED is mounted on ESM Panel #2 (-Z end of ESM) so that it has clear fields of view in the -X and +Y directions. The TED is mounted to the +Y side of the truss between the ESM and RSS. The outlines of each of these boxes are shown in Figures 4.11.5-4 through 4.11.5-6.

TBD

Figure 4.11.5-1. TED Simplified Block Diagram

TBD

Figure 4.11.5-2. MEPED Simplified Block Diagram

TBD

Figure 4.11.5-3. DPU Simplified Block Diagram

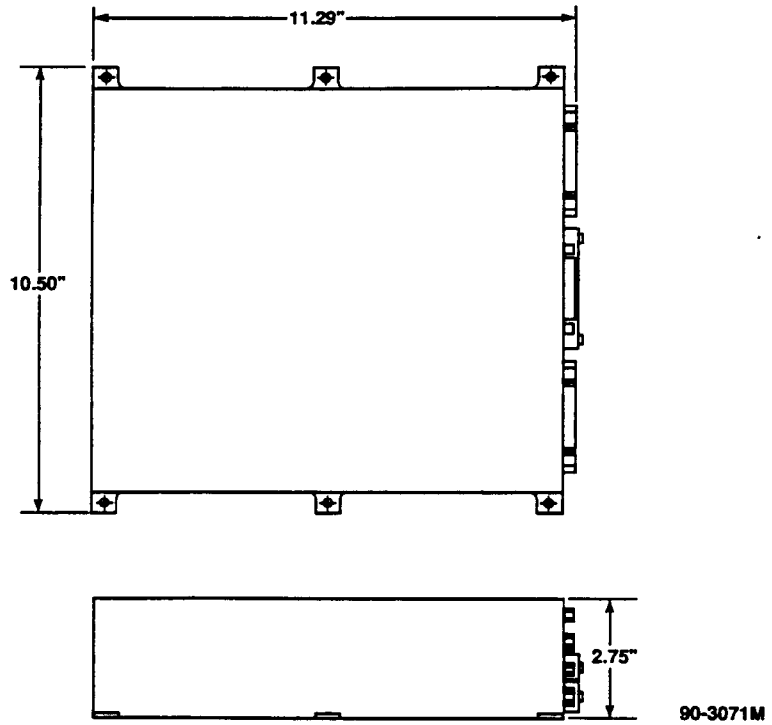

Figure 4.11.5-4. SEM DPU Outline Drawing

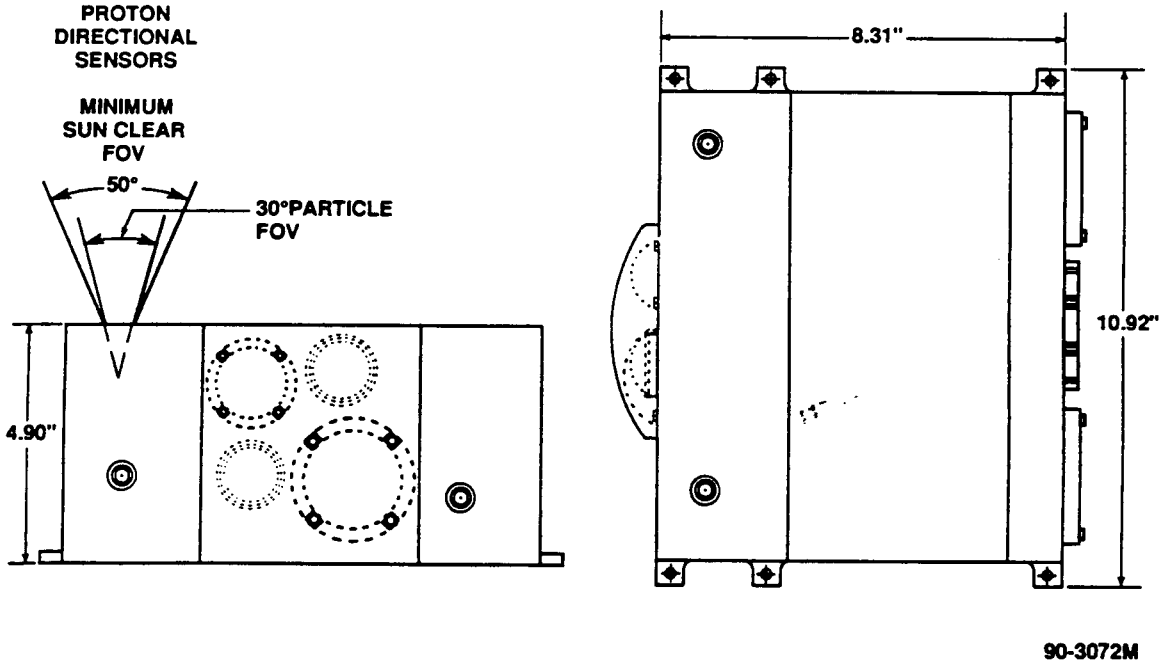

Figure 4.11.5-5. SEM MEPED Outline Drawing

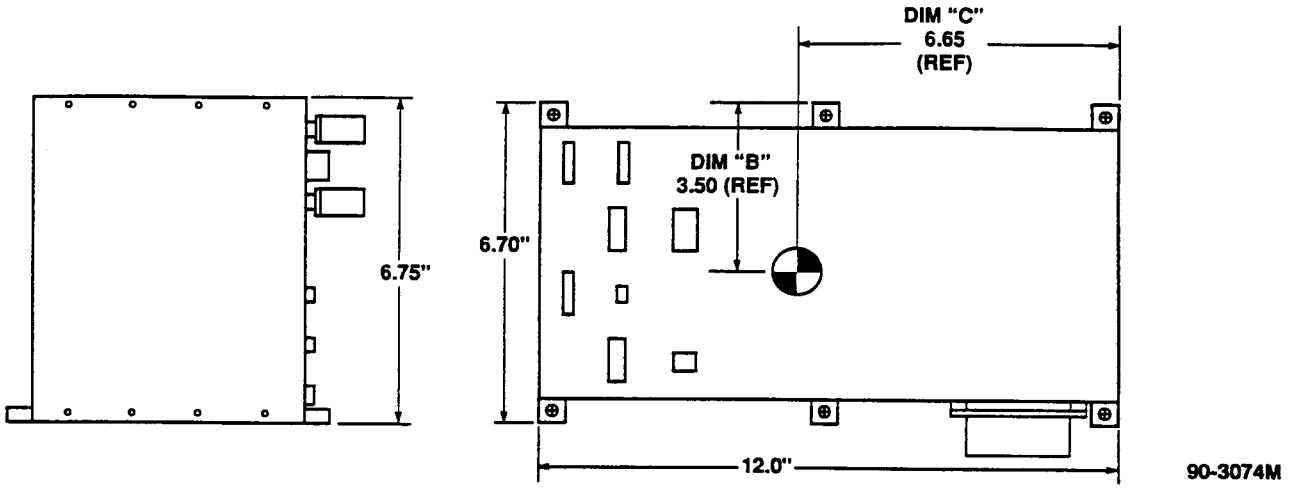

Figure 4.11.5-6. SEM TED Outline Drawing

The general system characteristic of the SEM and interfaces between the SEM and the spacecraft are fully discussed in the Unique Interface Specification for the SEM, RCA Drawing IS-3267700. A summary of these interface characteristics is shown in Tables 4.11.5-1 through 4.11.5-4.

TABLE 4.11.5-1. SEM FIELD OF VIEW PARAMETERS

TBD

TABLE 4.11.5-2. SEM ELECTRICAL PARAMETERS

Output Telemetry			
Digital A Telemetry	Two 8-bit TIP words per minor frame		
Digital B Telemetry	TBD		
Analog Telemetry	TBD		
Power (Orbit Average)	MEPED	TED	DPU
+28 Volt Main Bus	TBD	TBD	TBD
+28 Volt Pulse Load Bus	-	-	-
+28 Volt Telemetry Bus	-	-	TBD
+10 Volt Interface Bus	-	-	TBD
+5 Volt Interface Bus	-	-	-
Power Converter Frequency	TBD		
Input Signals			
Commands - Pulse - Level	TBD TBD		
Clock Signals	TBD		
Sync. Signals	TBD		
A_1 Data Enable Pulse C_1 Data Clock (8320 pps.)			

TABLE 4.11.5-3. SEM MECHANICAL PARAMETERS

	MEPED	TED	DPU
Mechanical/Thermal ICD	TBD	TBD	TBD
Number of Modules	1	1	1
Weight (maximum - pounds)	TBD	TBD	TBD
Size	TBD	TBD	TBD

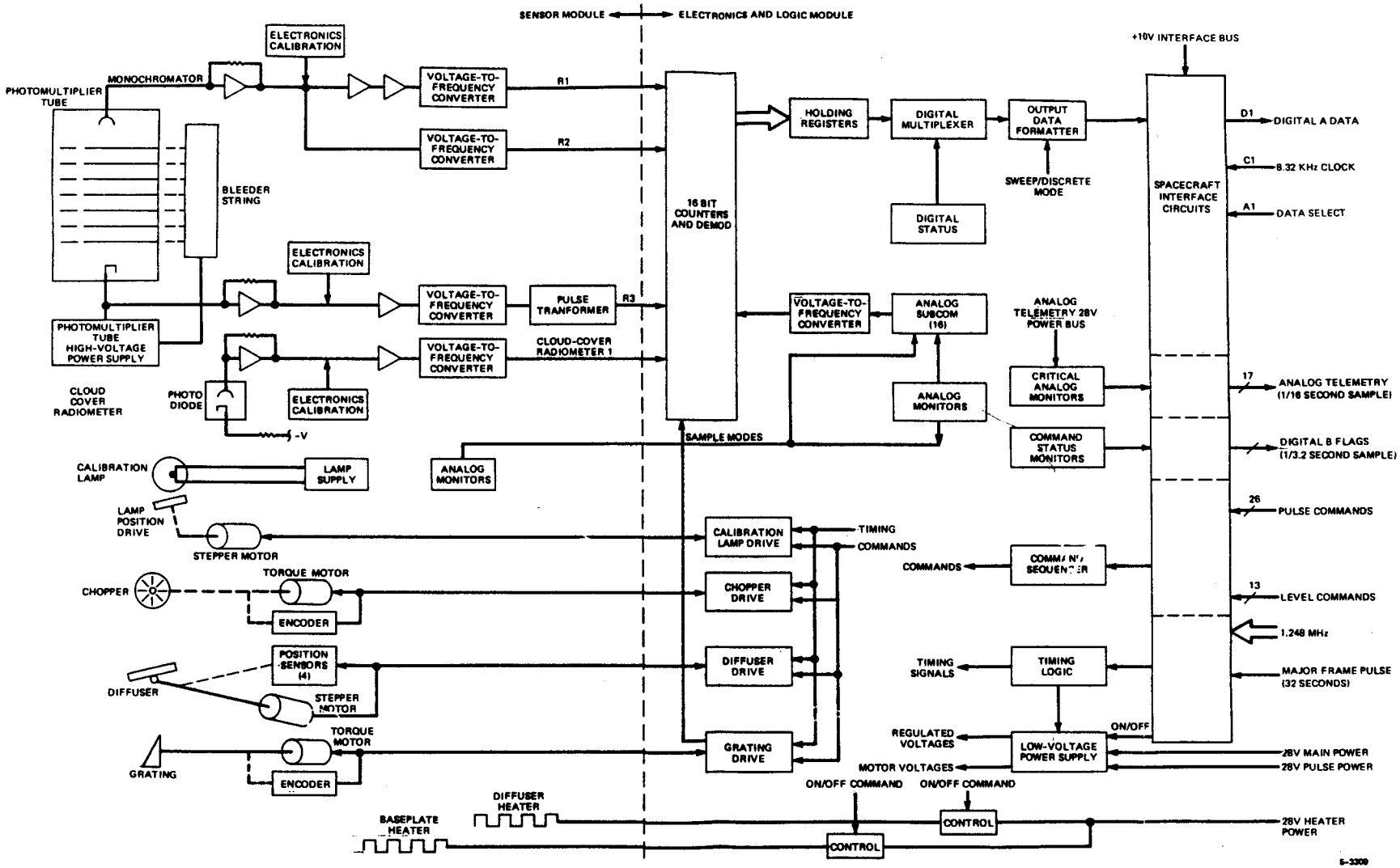

Figure 4.11.6-1. SBUV/2 Electrical Block Diagram

TABLE 4.11.5-4. SEM THERMAL PARAMETERS

	MEPED	TED	DPU
Mechanical/Thermal ICD (AFC Dwg. No.)	TBD	TBD	TBD
Normal Operating Temperature	TBD	TBD	TBD
Operating Temperature Range	TBD	TBD	TBD
TCE - Louver Set Point	TBD	TBD	TBD
- Heater Set Point	TBD	TBD	TBD
- Heater Power	TBD	TBD	TBD
Heat exchanged with S/C	TBD	TBD	TBD
Temperature Control Method			
DPU - Radiation and Conduction to the ESM panel.			
MEPED - TBD			
TED - TBD			

4.11.6 SOLAR BACKSCATTER ULTRAVIOLET SPECTRAL RADIOMETER

The SBUV/2 is an operational remote sensor designed to map, on a global scale, the total ozone concentrations and the vertical distribution of ozone in the earth's atmosphere. The SBUV/2 measures the spectral radiance of the solar ultraviolet radiation backscattered from the earth and the direct solar spectral irradiance; both measurements are made in the 160 to 400 nm spectral range.

The SBUV/2 measures the backscattered radiation in an 11.3° x 11.3° field of view in the nadir direction at 12 discrete, 1.1 nm wide wavelength bands between 252.0 and 339.8 nm using a scanning double monochromator. The solar irradiance is measured at the same 12 wavelength bands by displaying a lenticular diffuser which reflects sunlight into the instrument field of view. The SBUV/2 also has the capacity to measure the solar irradiance or atmosphere radiance with a continuous spectral scan from 160 to 400 nm in 0.148-nm increments, providing data on the photochemical processes in the atmosphere. A separate narrowband filter photometer, the Cloud Cover Radiometer, continuously measures the earth's surface brightness outside the ozone absorption band at 379 nm. The Cloud Cover Radiometer's 11.3° x 11.3° field of view is co-aligned with the monochromator's field of view.

The SBUV/2 is a non-spatial scanning, spectrally scanning instrument which operates in four monochromator modes, four scene modes, and a diffuser decontamination mode. The four monochromator modes are the discrete mode, the sweep mode, the wavelength calibration mode, and the position mode. The four scene modes, which are achieved by commanding the diffuser and the calibration lamp, are the earth view, sun view, wavelength calibration, and the diffuser check modes.

The SBUV/2 is contained in two distinct modules. The Sensor Module, designated SBUV on the spacecraft, is mounted on the outside of the Equipment Support Module (ESM) earth-facing panel. The Electronics and Logic Module (ELM), designated SBUVE, is mounted inside the ESM. All spacecraft electrical interfaces with the instrument are made through the ELM. The SBUV/2 electrical block diagram is shown in Figure 4.11.6-1. The outline of the SBUV/2 is shown in Figure 4.11.6-2. The general system characteristics of the SBUV/2 and interfaces between the SBUV/2 and the spacecraft are discussed in the SBUV/2 Unique Instrument Interface Specification, IS-2295548. A summary of these interface characteristics are shown in Tables 4.11.6-1 through 4.11.6-4.

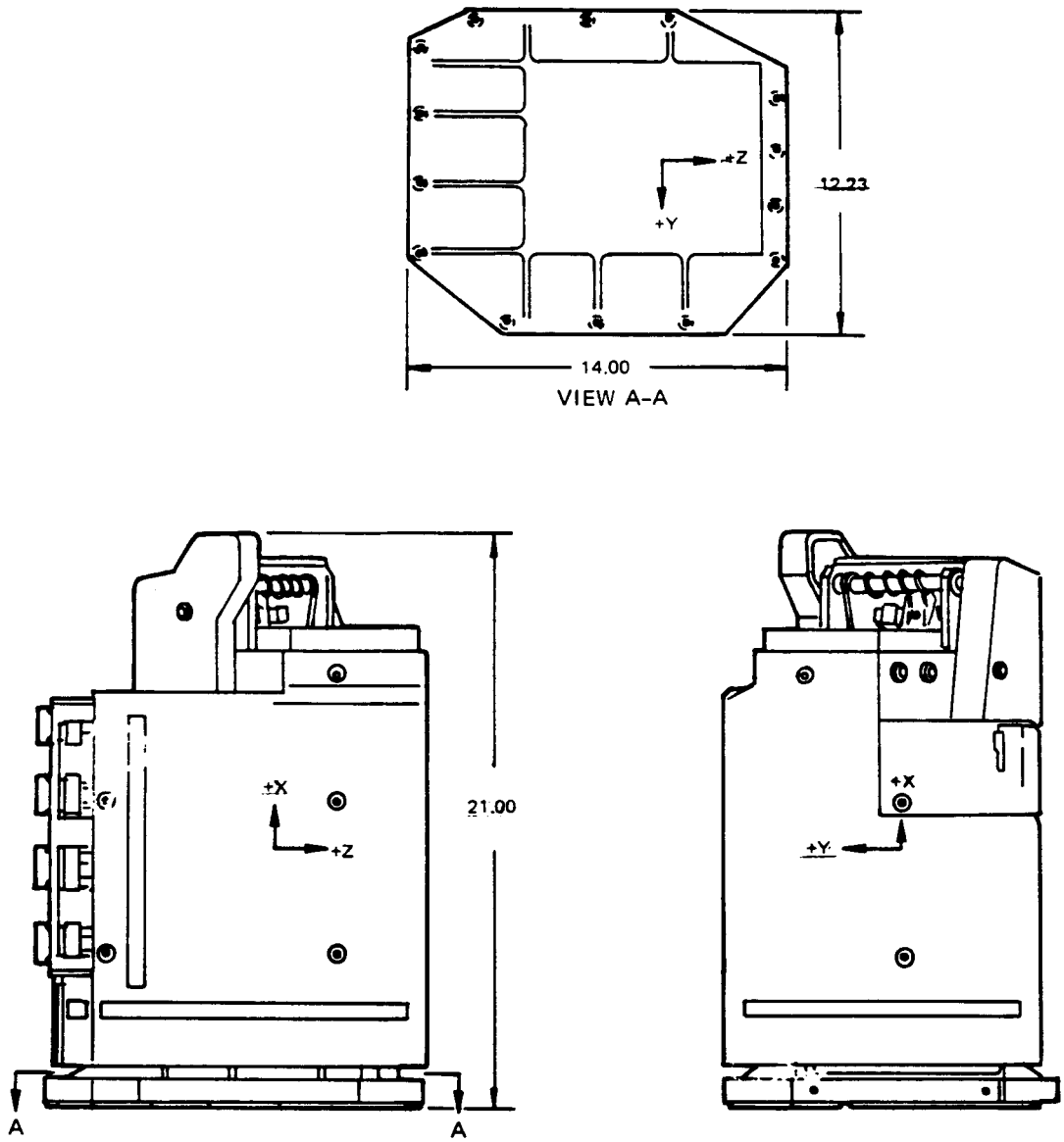

Figure 4.11.6-2. SBUV/2 Outline Drawing

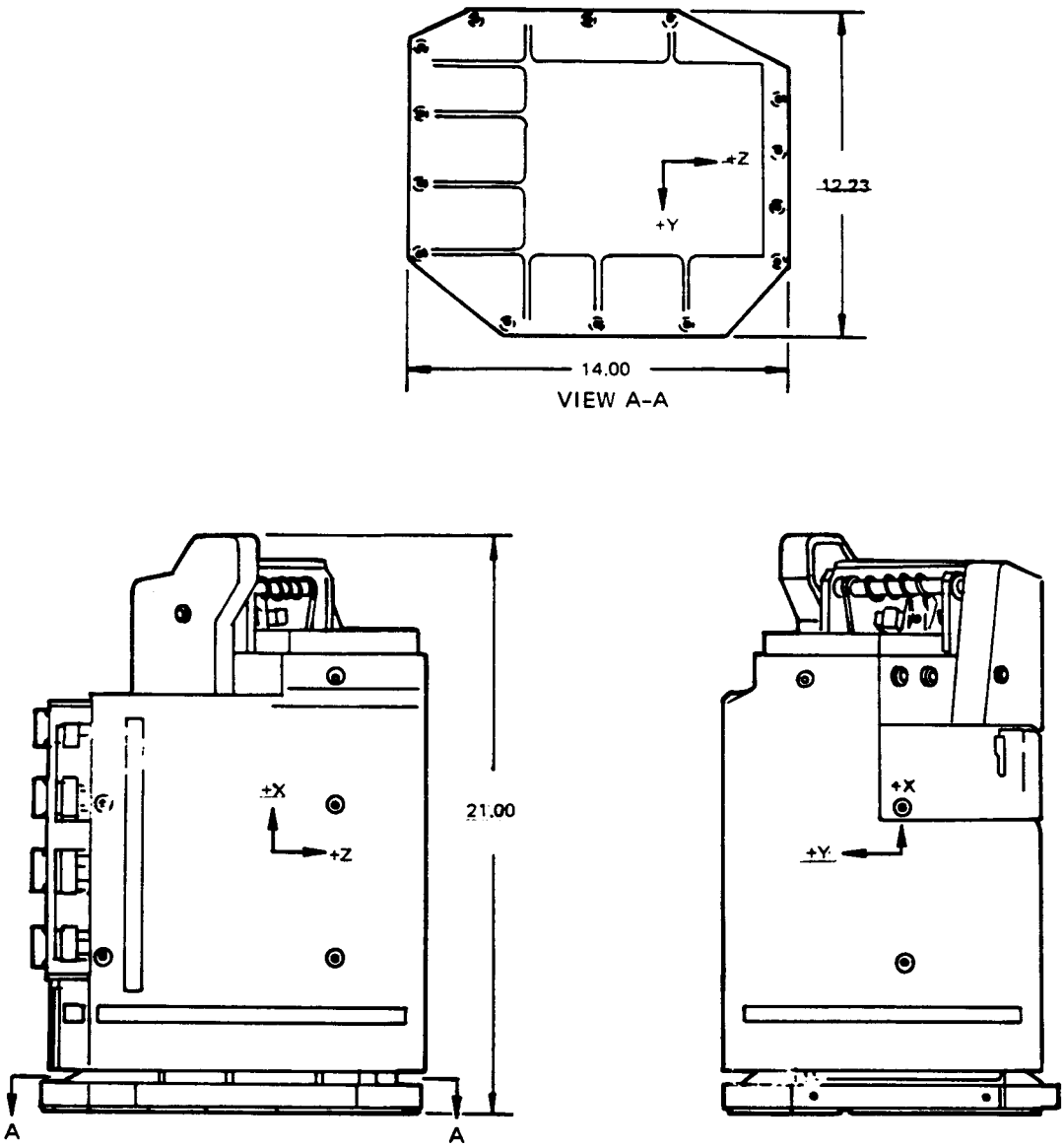

Figure 4.11.6-2. SBUV/2 Outline Drawing

TABLE 4.11.6-1. SBUV/2 SPECTRAL PARAMETERS

Parameter	Spectrometer	Cloud-Cover Radiometer
Spectral Range (nm)	160 to 400	379
Detector Type	Photomultiplier	Photodiode
Dynamic Range (mW/m^2-sr-Ä)		
Maximum Scene Radiance Minimum Scene Radiance	53 1.2×10^{-4}	40 0.125
Maximum Solar Irradiance Minimum Solar Irradiance	166 0.01	
Ground Resolution - measured from Nadir (km)	160 x 160	160 x 160
Spectral Scan Period (sec)	32	N/A

TABLE 4.11.6-2. SBUV/2 ELECTRICAL PARAMETERS

Output Telemetry	
Digital A Telemetry	Twenty 16-bit words per second (scientific data instrument status housekeeping telemetry)
Digital B Telemetry	22 (status indicators)
Analog Telemetry	17 (temperature, current, and voltage values)
Power (Orbit Average) +28 Volt Main Bus +28 Volt Pulse Load Bus +28 Volt Telemetry Bus +10 Volt Interface Bus Power Converter Frequency	 6.3W 9.1W 0.10W 75 mW 52 kHz
Input Signals Commands - Pulse - Level	 25 13
Clock Signals - 1.248 MHz - 1.0 Hz	
Sync. Signals - 32 sec	
A_1 Data Enable Pulse C_1 Data Clock (8320 pps.)	

TABLE 4.11.6-3. SBUV/2 MECHANICAL PARAMETERS

Interface Control Drawing, Electronic and Logic Module	BASD Drawing No. 67792	
Interface Control Drawing, Sensor Module	BASD Drawing No. 67899	
Number of Modules	2	
	SBUV	SBUVE
Weight (maximum)	60 pounds (maximum)	26 pounds (maximum)
Size*	21 x 12.1 x 14 in.	13 x 8.75 x 13 in.

* X x Y x Z

TABLE 4.11.6-4. SBUV/2 THERMAL PARAMETERS

SBUV/2 Interface Control Drawing	BASD Drawing No. 67899
Normal Operating Temperature (measured at baseplate)	+15°C
Operating Temperature Range (measured at baseplate)	0° to +30°C
Temperature Control Method	
SBUV	Conduction to the ESM through the mounting feet and radiation to space via a radiator on the back side of the diffuser housing.
SBUVE	Conduction and radiation to the internal ESM.
Heat exchanged with S/C	Less than 5 watts between the sensor module and the ESM front panel.

4.11.7 SEARCH AND RESCUE REPEATER

The Search-and-Rescue Repeater (SARR) receives distress signals at 121.5 MHz, 243 MHz, and 406.05 MHz using a receive antenna with two concentric quadrifilar structures. One structure is used for receiving at 121.5 MHz and 243 MHz; the other is used for receiving at 406.05 MHz. These unprocessed uplinked signals, as well as search-and-rescue signals processed by the SARP-M at 1544.5 MHz using a quadrifilar helix antenna. The SARR is completely redundant except for the 406.05 MHz receivers. There are a total of two 406.05 MHz receivers for use on NOAA-H, -I, and -J. The SARR Receive Antenna (SRA) is deployed at the end of the ascent phase in a two-stage process.

The general system characteristics of the SARR and interfaces between the SARR and the spacecraft are described in the SARR Unique Interface Specification RCA Drawing No. IS-2295546. A summary of these characteristics is shown in Tables 4.11.7-1 through 4.11.7-5.

TABLE 4.11.7-1. SARR INPUT PARAMETERS

Parameter	Values
Frequency	121.5, 243, 406.05 MHz
Bandwidth	25 KHz - 121.5 MHz 46 KHz - 243 MHz 80 KHz - 406.05 MHz
Signal Strength	-179 to -137 dBw - 121.5 MHz -182 to -149 dBw - 243 MHz -165 to -137 dBw - 406.05 MHz
Automatic Level Control	25 ms Attack 75 ms Decay
Transient Recovery Time	2 ms after removal of -60 dBw input signal at any frequency
Processed Data	Retransmission of SARP-M data bit stream of 2.4 kpbs, Coded BiØL

TABLE 4.11.7-2. SARR OUTPUT PARAMETERS

Parameter	Values
Frequency	1544.5 MHz
Frequency Stability	Long Term ± 1 part in 10^6 Short Term ± 1 part in 10^9 in 10 minutes
RF Power	8 Watts Minimum 10 Watts Maximum
Modulation Index	0.7 rad rms 2.0 rad peak peak to rms ratio ≤ 15 dB
Harmonics	50 dB below carrier power
Phase Jitter	Less than 10° rms at 50 Hz bandwidth
RF Power output (rms) variation	$\pm 5\%$ for any combination of input signals or any type of input signal

TABLE 4.11.7-3. SARR ELECTRICAL PARAMETERS

Output Telemetry	
Digital A Telemetry	None
Digital B Telemetry	4 (status indicators)
Analog Telemetry	22 (current, voltage power and temperature values)
Power (Orbit Average)	
+28 Volt Main Bus	43.6W
+28 Volt Pulse Load Bus	0.0W
+28 Volt Telemetry Bus	0.11W
+10 Volt Interface Bus	0.05W
Power Converter Frequency	32.5 kHz
Input Signals	
Commands - Pulse	14
- Level	16
Clock Signals	Not Used
Sync. Signals	Not Used
TIP Interface	Not Used
A_1 Data Enable Pulse	
C_1 Data Clock (8320 pps.)	

TABLE 4.11.7-4. SARR MECHANICAL PARAMETERS

Number of Mounting Feet/Holes	2 - a Receiver Pallet and a Transmitter
Outline Drawing	Figure 2, IS-2295546
Number of Modules	2 - a Receiver Pallet and a Transmitter Assembly
Weight	Receiver Pallet 32 pounds Transmitter Assembly 11 pounds
Uncompensated Momentum	0
Number of Mounting Feet/Holes	Receiver Pallet 60 9 Transmitter Assembly 34
S/C Interface Connectors	11

TABLE 4.11.7-5. SARR THERMAL PARAMETERS

Normal Operating Temperature (measured at baseplate)	+20°C
Operating Temperature Range (measured at baseplate)	0°C to +35°C
TCE - Louver Set Point	10°C
- Heater Set Point	5°C
- Heater Power	6.6W
Temperature Control Method	Pinwheel louvers and electric heaters

4.11.8 SEARCH AND RESCUE PROCESSOR WITH MEMORY

The Search and Rescue Processor with Memory (SARP-2), like the DCS-2, is a random-access system that provides a means for collecting information from and locating the position of distress transmitters-in this case Emergency Locator Transmitters (ELTs) and Emergency Position Indicating Radio Beacons (EPIRBs).

The transmitter location is derived by using Doppler analysis techniques on the measured carrier frequencies of several messages during one or (preferably) two satellite passes. The data received from each distress transmitter contain identification and situation information and this data along with the carrier frequency measurements are formatted into time tagged messages. The messages are transferred to the SARR L-Band link for retransmission in real time and are stored in the unit memory for readout upon command to the ground based control center where the position determining Doppler processing is performed.

SARP-2 equipment on the spacecraft includes a Receiver and Power Unit (RPU), a Signal Processing Unit (SPU) and a UHF antenna (designated UDA) complement including a filter and diplexer which is shared with the DCS. Data from the distress transmitters is transmitted to the SARP-2 with carrier frequencies centered on 406.025 MHz, in the form of bi-level 400 bps digital data. After demodulation by the receiver, the intermediate frequencies are transferred to three DRUs. The DRUs strip the ID and situation data which is combined in the SPU with incoming signal level information, time code, frequency (for Doppler processing) and a sync pattern and transferred to the SARR L-Band link and SPU memory in the form of 24 bit words at a rate of 2400 bps. The memory can store 16380 twenty bit words. See Figure 4.11.8-1 for a simplified block diagram of the SARP-2.

The UDA is a 1-1/2 turn, 1-1/4 a wavelength quadrifilar antenna. It has a circularly polarized pattern with a maximum gain of +3.5 dBli at the earth's horizon (63 degrees off axis).

RPU is mounted on the inside of ESM panel No. 6, the SPU and filter are mounted on the inside of ESM panel No. 5. The diplexer is mounted on the inside of ESM panel No. 1, and the UDA is attached to the outside of ESM panel No. 1. The outlines of these units are shown in Figures 4.11.8-2 and 4.11.8-3.

The general system characteristics of the SARP-2 and interfaces between the SARP-2 and the spacecraft are fully discussed in the Unique Interface Specification for the SARP-2, RCA Drawing IS-2613073. A summary of these interface characteristics is shown in Tables 4.11.8-1 through 4.11.8-4.

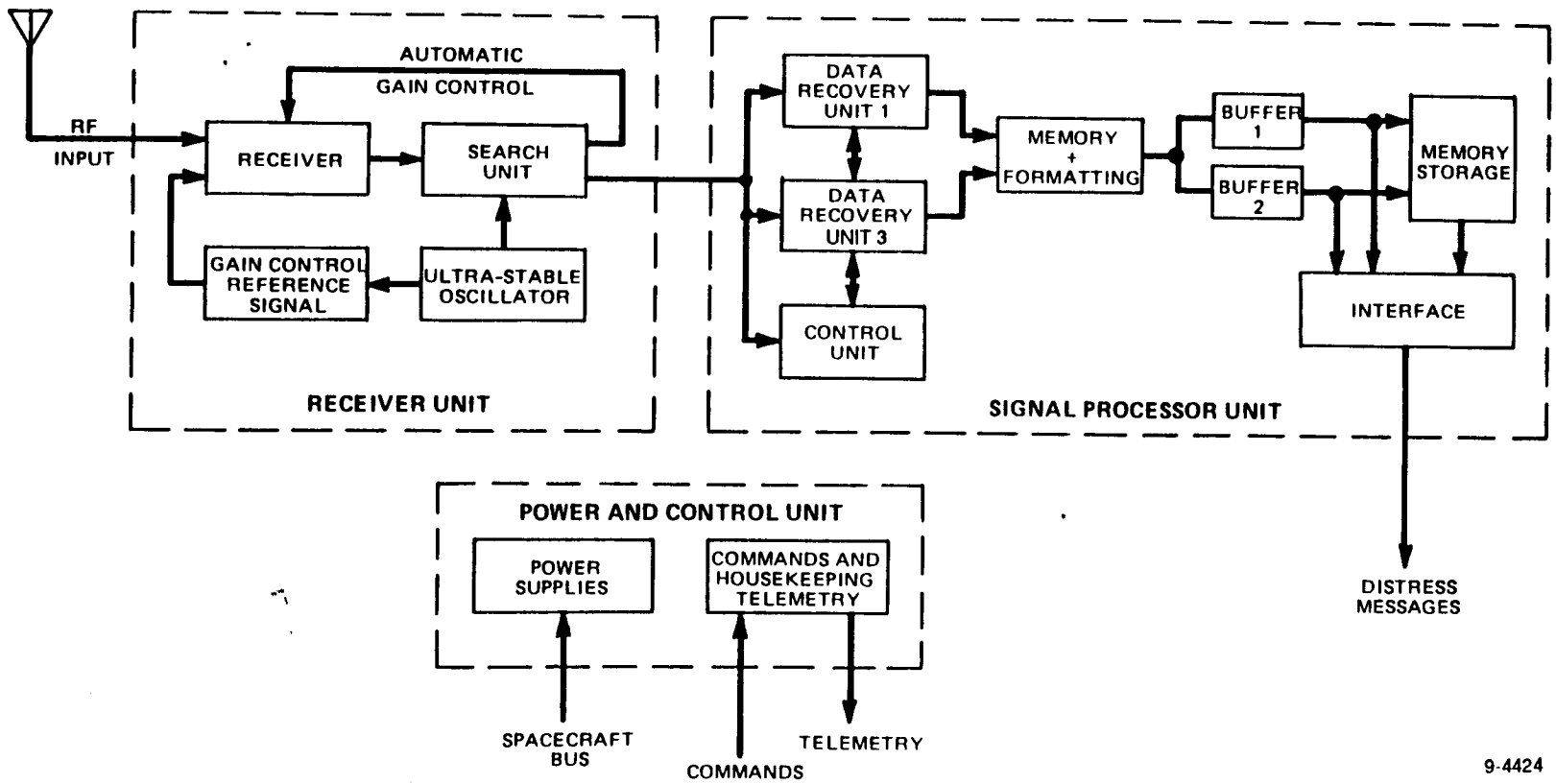

Figure 4.11.8-1. SARP-2 Simplified Block Diagram

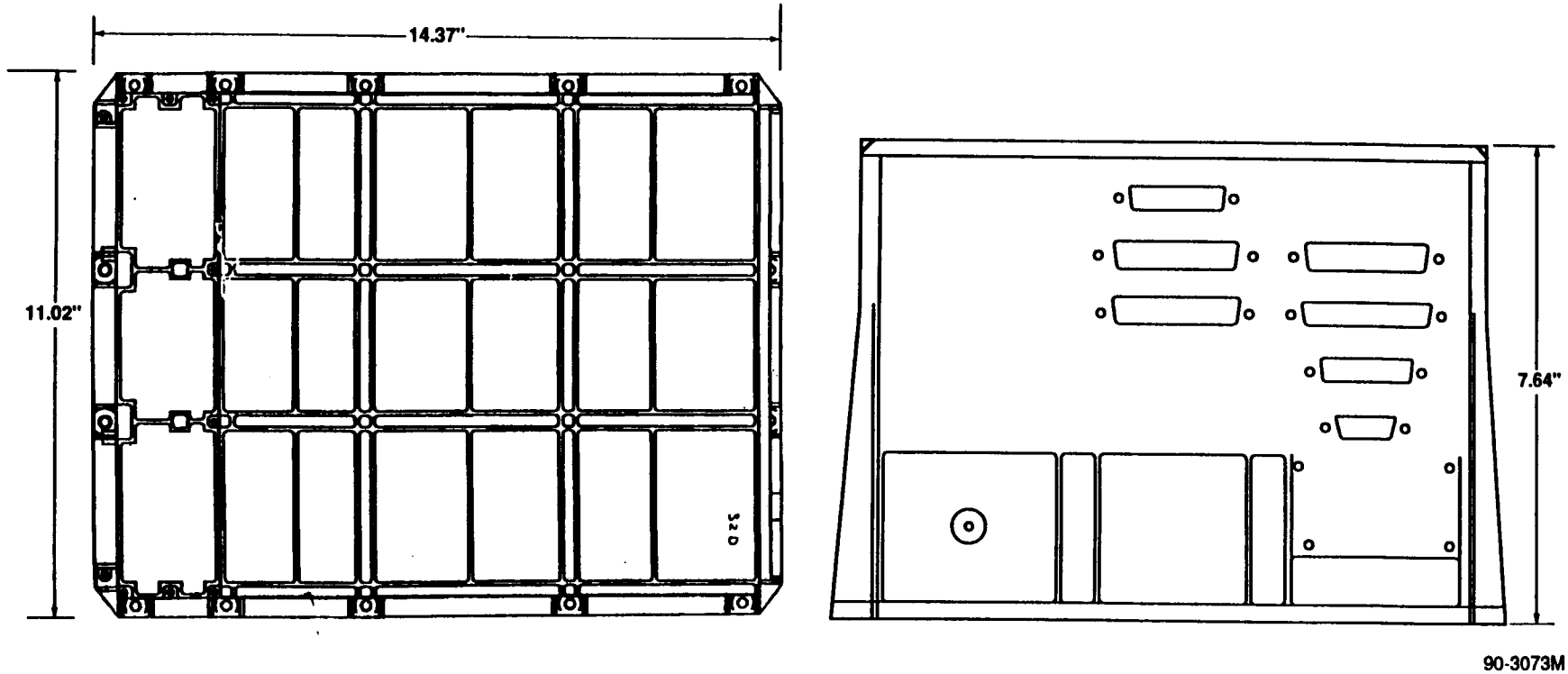

Figure 4.11.8-2. SARP-2 RPU Outline Drawing

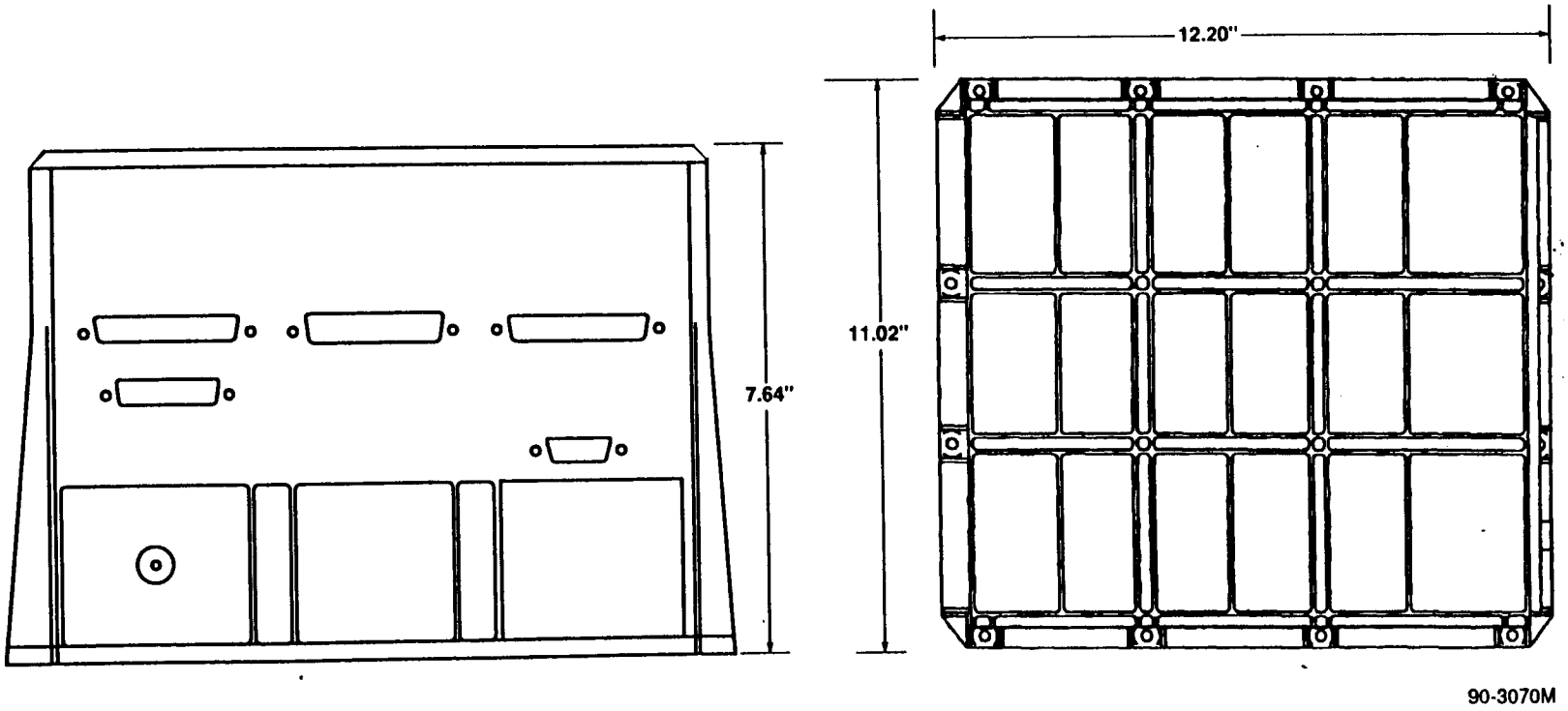

Figure 4.11.8-3. SARP-2 SPU Outline Drawing

TABLE 4.11.8-1. SARP-2 SYSTEM PARAMETERS

Receiver:	
• Frequency	406.025 MHz in three commandable bandwidths, 27 kHz, 40 kHz and 80 kHz
• Sensitivity	-108 to -131 dBm
• Dynamic Range	23 dB
• S/N	$\geq$ 40 dBHz
DRU's	3
Memory	394 Kilo bits
Message Content:	Synchronization Signal Level Time of Message User Class, ID, Country Situation Code Doppler Counting
Antenna:	
• Half Cone Angle	63°
• Polarization	Right Circular
• Gain at 63°	+3.5 dBli maximum
• VSWR	< 1.5:1

TABLE 4.11.8-2. SARP-2 ELECTRICAL PARAMETERS

Output Telemetry		
2400 bps Data	To SARR L-Band	
Digital B Telemetry	17 (status indicators)	
Analog Telemetry	9 (temperature and voltage)	
Power (Orbit Average)	RPU	SPU
+28 Volt Main Bus	14.77W	4.63W
+28 Volt Analog Telemetry Bus	TBD	---
+10 Volt Interface Bus	4 mW	---
Power Converter Frequency	81.3 kHz	
Input Signals		
Commands - Pulse	21	
Clock Signals	None	
Sync. Signals	None	

TABLE 4.11.8-3. SARP-2 MECHANICAL PARAMETERS

	(RPU) Receiver & Power Unit	(SPU) Signal Processing Unit
Mechanical Interface Control Dwg.	9212-200E 380/02	9212-300E 380/01
Number of Modules	1	1
Weight	29.8 lbs.	24.3 lbs.
Size*	14.4 x 11.0 x 7.7 in.	12.2 x 11.0 x 7.7 in.

* X x Y x Z

TABLE 4.11.8-4. SARP-2 THERMAL PARAMETERS

Thermal Interface Drawing	TBD
Normal Operating Temperature (measured at baseplate)	+20°C
Operating Temperature Range (measured at baseplate)	-5 to +45°C
Temperature Control Method	Conduction to ESM Panel Heat Sinks
Total System Thermal Dissipation	TBD

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4.12 ASCENT GUIDANCE SOFTWARE

The following pages describe NOAA-KLM ascent guidance software. Items marked TBD in this section will not be complete until information is available from the AGS PDR/CDR with MDAC.

4.12.1 GUIDANCE SOFTWARE DEVELOPMENT

4.12.1.1 Introduction

The ATN guidance and navigation equations are used to perform the guidance and steering functions for the upper stage of the launch vehicle. The Ascent Guidance System (AGS) will navigate independently of the Titan II G&N system from liftoff until stage separation, but will have no active role in vehicle guidance or control. AGS will assume control of the launch vehicle at stage separation, and will actively guide the second stage and the integral payload until handover to the orbital control system.

The Ascent Guidance Software for NOAA-KLM was developed for the ATN spacecraft (NOAA-F and G), which includes the fourth order digital filter in the controls equations.

4.12.1.1.1 Hardware Description

The AGS hardware consists of an Inertial Measurement Unit (IMU) and a Standard Controls Processor (SCP), more specifically known as the SCP-234. The IMU contains three dual channel gyros and three accelerometers. The gyros and accelerometers employ pulse torquing rebalance loops.

The SCP-234 guidance computer is a 32K word machine with a minimum instruction execution time of 4.7 microseconds and a word length of 16 bits. It is mounted in the spacecraft and controls the performance of all open and closed loop guidance functions, including discrete sequencing and control system operation. Characteristics of this unit are described fully in Section 4.9.2.3 of this report.

Buffering of all data and control signals between the guidance computer and all other spacecraft units is provided by the Controls Interface Unit (CIU). This interfacing function includes processing of gyro and accelerometer data, issuing thruster on-off commands for the vehicle controls system, and provision of timing signals to the SCP, IMU, and other units. Details of this unit are given in Section 4.9.2.2 of this report.

4.12.1.1.2 Functional Description

The AGS performs the in-flight functions of open loop sequencing, autopilot control, navigation, closed loop guidance, and AGS PCM telemetry data formatting. In addition, it performs pre-flight functions of alignment, controls activation tests, navigation test, and dynamic closed loop system test for both the Titan II and the NOAA-KLM flight phases.

4.12.1.1.2.1 In-Flight Functions. Open loop sequencing provides trajectory and vehicle intelligence for up to 17 on/off discretes, for all required control system configuration and gain changes, and for a series of programmed rates to perform the nominal trajectory shaping after Titan II burnout. All sequencing is done on a time basis with 0.5 second resolution, but provisions are made for special treatment of discontinuities caused by Titan II, AKM, and N_2H_4 engine shutdowns.

The autopilot control function generates attitude error and attitude rate data based on gyro-sensed vehicle angular motion. Attitude error data is defined by the integrated difference between the gyro-sensed rates and the commanded (desired) angular rates. Phase plane switching line logic defined by input mission constants utilizes the measured attitude and rate data to determine the appropriate discrete commands to the on/off thrusters, thus providing vehicle control.

The navigation function provides continuous knowledge of the vehicle state parameters of position, velocity, acceleration, and attitude. The attitude states are maintained as a nine-element transformation matrix relating the body axes to a geocentric inertial coordinate system. This matrix is updated using body rate information sensed by the three body-mounted (strapdown) gyros. Calibration compensation for these gyros as well as for the three body-mounted accelerometers is provided within the computer software. Vehicle accelerometer data are transformed through the attitude matrix into the inertial coordinate system, where they are combined with gravitational acceleration data derived from vehicle position data and an oblate earth gravitational model. The combined acceleration is integrated twice to provide velocity and position states of the vehicle. Attitude computations, as well as the transformation of vehicle accelerometer data into inertial coordinates, is accomplished at a rate of 50 times per second. Gravitational computations and the position and velocity updates are made at the rate of twice per second.

Shortly before the Titan II SECO, the guidance system performs an accelerometer test on the thrust axis accelerometer to verify operation within a given tolerance of the Titan II nominal acceleration value. After allowing for the maximum possible variation in Titan Stage II tailoff, a navigation goodness test is performed to ensure the resulting Titan II orbit is within the corrective capability of the ATN-KLM vehicle. If both the acceleration and the navigation tests are acceptable, closed loop guidance is initiated at a pre-programmed time point. If either test fails, an attitude pointing mode is implemented to orient the vehicle to the nominal separation attitude and the remainder of the mission is commanded in a non-guided pre-programmed sense.

Closed loop guidance provides trajectory updates to compensate for vehicle non-nominal performance and generates a set of end conditions necessary to achieve the desired orbit. To accomplish this, the guidance equations provide a nominal vehicle predictor for each powered stage. Predicted stage end conditions of position and velocity are defined by adding the predicted amounts that a nominal vehicle would gain over the remainder of the stage to the current vehicle position and velocity supplied by the navigation function. These predicted end conditions are compared to the desired end conditions on the nominal orbit which are based on the nominal targeted end state. Resultant errors in acceleration and velocity are used to define pitch and yaw attitude corrections as well as to update the desired vehicle burnout time.

Modification of the actual burnout time based on these updates is possible only during the hydrazine velocity correction burn phase. The attitude corrections are defined in such a manner that they will take the total remaining time to burnout of the current stage to remove all the velocity errors. As time approaches the end of the stage, the velocity constraint is removed from the steering equations to improve the stability characteristics of the closed loop operation and the acceleration only steering commands are applied until guidance is closed out.

The AKM and N_2H_4 powered phases are guided by the above technique using a computation interval of 2 per second. Closed loop guidance is used during the coast phase preceding AKM burn to re-define AKM ignition time and to orient the vehicle such that, if nominal performance is achieved during AKM burn, the orbit perturbations accrued prior to the AKM phase will be totally compensated.

Attitude pointing guidance modes at various points along the trajectory orient the vehicle in a desired attitude relative to the orbit plane.

Pre-selected computational parameters are formatted into a PCM telemetry frame and processed out of the computer through a telemetry buffer register. The basic frame consists of 80 words: 10 transmitted at a repetition rate of 20 times per second, 20 at 10 times per second, and 50 at 2 times per second.

4.12.1.1.2.2 Pre-Launch Functions. Pre-launch alignment consists of establishing precise initial conditions on the navigation attitude matrix which relates vehicle body coordinates to the geocentric inertial coordinate system used as the navigation reference frame. This is accomplished by utilizing the lateral accelerometer information to define a continuous body level condition and an optical measurement to define its azimuth orientation. Since the vehicle may sway on the launch pad, alignment is necessarily a continuous process until liftoff detection. By comparing the gyro-updated attitude matrix against the accelerometer and azimuth data, a closed-form error solution is implemented to slave the gyro matrix continuously to these data. By introducing an integration into the feedback of the error signal as well as the error signal, gyro drifts can also be estimated from this loop. This computation loop is entered at the 50 per second rate, which is consistent with sensor data processing.

Controls activation tests consist of providing an attitude error profile which will cause gas jet operation. The tests are accomplished by stepping through the control sequencer and allowing the attitude error profile to be exercised each time a change in control mode is sensed.

To accommodate a complete checkout of the AGS after it is installed in the vehicle, a closed loop checkout capability was incorporated into the AGS flight software. This capability provides dynamic vehicle models of the Titan II and the ATN-KLM spacecraft to close the loop between the flight program output signals and sensor input signals. By adding the vehicle model output computation data to IMU sensor data, a complete mission can be simulated while on the pad in a launch configuration. The basic flight program, including sensor data processing, is executed by this technique, and all normal flight functions can be observed. Since the vehicle model is not a perfectly nominal model because of its simplicity, even the guidance system demonstrates its performance

characteristics. This test is capable of being executed at any time while the flight program is loaded into the computer along with mission specific constants. Since the actual flight program is used, the test necessarily is run in real time.

4.12.1.2 General Requirements

The features of the Titan II/ATN-KLM vehicle and the AGS hardware which were important in the design of the AGS guidance equations are discussed in this section.

4.12.1.2.1 Mechanization

The AGS program is coded to run in the SCP-234, which as previously mentioned has a 16 bit word length. Because of the short word length the majority of the guidance program requires coding in double precision. Approximate memory allotments are 3,712 words for the program code, 700 words for variable storage, and 700 words for storage of constants.

The maximum time consumption for 50 per second guidance computations is estimated at 21.2 milliseconds for closed loop test processing during pre-launch exercises, and 19.2 milliseconds for processing flight functions. Maximum processing time for the 2 per second guidance loop is approximately 20.9 milliseconds; this occurs when the coast adjust guidance mode is active. Peripheral functions such as telemetry processing are not included in these estimates.

4.12.1.2.2 Flexibility/Adaptability

The guidance software for ATN-KLM, is identical to that used on ATN-HIJ, the NOAA-F and G which is a close derivative of the TIROS-N software and, to a more limited degree, also a derivative of the MDAC Delta Inertial Guidance System software. As such, the ATN-KLM software provides flexibility for a wide range of mission requirements and adaptability for expansion to accommodate possible variations in vehicle configuration.

There are two primary features of AGS that provide the indicated flexibility and adaptability. The first of these is the targeting method, coupled with the manner in which the guidance system defines the nominal vehicle capability. This feature, which is adaptable to a variety of vehicle configurations, is discussed in Section 4.12.1.2.4 (Targeting).

The second feature contributes predominantly to the system adaptability. It is the guidance error policy which, coupled with the steering scheme, guides the vehicle into a nearly nominal orbit. Time of passage of a given point and out-of-orbit-plane position error are sacrificed by the approach used. The time error has been estimated to have 3 sigma variation of well under 20 seconds, and is not foreseen as violating orbital requirements. The error policy is implemented by generating corrective pitch and yaw attitude rate steering commands based on velocity and acceleration errors, and updating the change in time-to-go to stage termination based on velocity error along the vehicle roll axis.

4.12.1.2.3 Accuracy

The guidance software program does not, in itself, contribute a significant amount to the total system error. This is accomplished by processing a large portion of the guidance computations in double precision. Use of single precision is limited to the controls equations, the sequencer processing, and most of the pre-launch tests except the navigation test. Since the guidance policy corrects the vehicle performance variations, it requires some level of error signal. Unlike radio guidance systems, inertial systems are not hampered by noise; therefore, guidance steering gains can be set quite high, thereby reducing the magnitudes of the error signals required to provide corrective signals. Previous analyses performed on DIGS and ATN-KLM have demonstrated that the error due to the guidance system is nearly negligible in relation to the sensor errors which affect the navigational accuracy.

4.12.1.2.4 Targeting

Trajectory design will be performed months in advance of a flight and will provide an "optimal" nominal trajectory for the vehicle to fly. The resultant trajectory satisfies not only the mission requirements but also any range safety or vehicle constraints placed on the system. An early definition of such a nominal trajectory is required both for payload customer analysis and for range safety purposes. Since this requirement exists, it is not necessary to incorporate a real time targeting capability in the AGS guidance equations.

The nominal trajectory provides the open loop programmed rates, position and velocity end conditions for each stage, desired vehicle orientation, and sequencing times. It also provides a definition of the nominal vehicle capability. The most flexible, efficient, and accurate method of defining the vehicle capability in a manner suitable for in-flight predictions was determined to be acceleration curve fits. Use of these acceleration curve fits to define the vehicle capability allows inclusion of the nominal gravity effect, thus minimizing the required on-board computations. The acceleration curve fits are derived independently for each of the three inertial axes for each stage and are limited to second order to keep the computations simple.

Several segments, each valid over a given time interval, can be used to increase accuracy. Because the nominal position and velocity capability of the vehicle must be well-defined, the curve fits are generated so that the integrals of the acceleration over each curve fit segment are exactly equal to the nominal position and velocity to be gained over that segment, satisfying two of the three possible constraints which may be imposed on a second order curve fit. The third constraint used is that the acceleration at the beginning of each curve fit segment be equal to the predicted acceleration at the end of the previous segment. The acceleration at the start of guidance for a stage is set equal to the nominal acceleration at that time.

4.12.1.3 <u>Navigation and Open Loop Guidance</u>

The guidance function is separable into the distinct categories of open loop and closed loop guidance. Open loop guidance consists basically of application of pre-programmed vehicle rotational rates and sequencing of vehicle

discrete functions, both of which are done with the assumption of nominal vehicle performance. Closed loop guidance consists of compensation for vehicle non-nominal performance by use of navigation data generated from internal measurements.

Navigation data must be processed from liftoff throughout the entire ascent flight phase to maintain knowledge of certain vehicle states; control system processing must be active throughout the ATN-KLM portion of flight, after stage separation. The navigation and control functions must be processed throughout both open and closed loop guidance phases, and will be discussed in this section along with the sequencing function. Furthermore, since the pre-launch alignment process is related to the navigation function in that it initializes the navigation attitude matrix, it will also be discussed in this section.

4.12.1.3.1 Navigation

The navigation function of the guidance system uses gyro and accelerometer sensor data to maintain current knowledge of vehicle states of position, velocity, attitude, and acceleration. First, the attitude state is defined by a 9 element transformation matrix from the current body coordinates to a geocentric inertial coordinate system. This matrix, TC, is updated from the strapdown gyro information at a computational rate of 50 times per second. The equations used for maintaining the TC matrix can be derived several ways; however, relating them to a closed form solution for a fixed inertial rate input provides a straightforward development.

The closed form equations for constant vehicle rates equal to $\dot{\phi}$, $\dot{\theta}$, and ψ over time interval θ are provided below.

Let

$$\omega = (\dot{\phi}^2 + \dot{\theta}^2 + \dot{\psi}^2)^{1/2}$$

The final matrix elements, $T_f(i,j)$, are given as a function of the initial matrix, $T_o(i,j)$, and the constant rates.

$$T_f(i,1) = T_o(i,1) \cos \omega\tau + \frac{\dot{\psi}T_o(i,2) - \dot{\theta}T_o(i,3)}{\omega} \sin \omega\tau$$

$$+ \frac{\dot{\psi}\dot{\phi}T_o(i,3) + \dot{\theta}\dot{\phi}T_o(i,2) + \dot{\phi}^2 T_o(i,1)}{\omega^2} (1 - \cos \omega\tau)$$

$$T_f(i,2) = T_o(i,2) \cos \omega\tau + \frac{\dot{\phi}T_o(i,3) - \dot{\psi}T_1(i,1)}{\omega} \sin \omega\tau$$

$$+ \frac{\dot{\phi}\dot{\theta}T_o(i,1) + \dot{\theta}\dot{\psi}T_o(i,3) + \dot{\theta}^2 T_o(i,2)}{\omega^2} (1 - \cos \omega\tau)$$

$$T_f(i,3) = T_o(i,3) \cos \omega\tau + \frac{\dot{\theta}T_o(i,1) - \dot{\phi}T_o(i,2)}{\omega} \sin \omega\tau$$

$$+ \frac{\dot{\psi}\dot{\theta}T_o(i,2) + \dot{\psi}\dot{\phi}T(i,1) + \dot{\psi}^2 T_o(i,3)}{\omega^2} (1 - \cos \omega\tau)$$

By substituting

$$\dot{\theta}\tau = \varepsilon\theta,$$

$$\dot{\psi}\tau = \varepsilon\psi,$$

$$\dot{\phi}\tau = \varepsilon\phi,$$

$$\sin \omega\tau = \omega\tau, \text{ and}$$

$$\cos \omega\tau = 1 - \frac{(\omega\tau)^2}{2},$$

the above equations can be formulated as the strapdown matrix algorithm where

$$G = \begin{bmatrix} -(\frac{\varepsilon\theta^2 + \varepsilon\psi^2}{2}) & \frac{\varepsilon\phi\ \varepsilon\theta}{2} - \varepsilon\psi & \frac{\varepsilon\phi\ \varepsilon\psi}{2} + \varepsilon\theta \\ \frac{\varepsilon\phi\ \varepsilon\theta}{2} + \varepsilon\psi & -(\frac{\varepsilon\phi^2 + \varepsilon\psi^2}{2}) & \frac{\varepsilon\theta\ \varepsilon\psi}{2} - \varepsilon\phi \\ \frac{\varepsilon\phi\ \varepsilon\psi}{2} - \varepsilon\theta & \frac{\varepsilon\theta\ \varepsilon\psi}{2} + \varepsilon\phi & -(\frac{\varepsilon\phi^2 + \varepsilon\theta^2}{2}) \end{bmatrix}$$

$$TC_n = TC_{n-1} + TC_{n-1}\ G$$

The values of $\varepsilon\phi$, $\varepsilon\theta$, and $\varepsilon\psi$ are, of course, used directly from the integrated gyro outputs over a 20 millisecond period.

Since the exact closed form equations will not cause TC matrix problems in terms of orthogonality or normality, errors of this type can be evaluated by the errors in the mechanization assumption ($\sin \omega\tau = \omega\tau$, $\cos \omega\tau = 1 - (\omega\tau)^2/2$) and word length considerations. To minimize these effects, the TC matrix is handled in a double precision manner, and approximately once each second it is orthonormalized using the Gram-Schmidt technique.

The other assumptions of the rate being constant in each of the axes over a given compute interval and the specific value used for this rate are major causes of computational error. This error is controlled mainly by the computation interval and the sensor loop dynamics.

4.12.1.3.1.1 Alignment. Alignment consists of establishing initial values of the above TC matrix at the time of liftoff. Since the vehicle may be swaying on the pad just prior to liftoff, it is necessary to provide a dynamic alignment which continuously tracks this motion. To do this, the alignment scheme depicted in Figure 4.12.1-1 is implemented.

The reference TC matrix is generated using accelerometer data and a fixed azimuth reference. The inertial reference coordinates are chosen as a right-handed earth-centered orthogonal coordinate system with its X and Y axes in the equatorial plane, with the X axis piercing the earth surface at the launch site meridian, with the Z axis along the earth's rotation axis positive out the North Pole, and with the Y axis completing the orthogonal triad as shown in Figure 4.12.1-2.

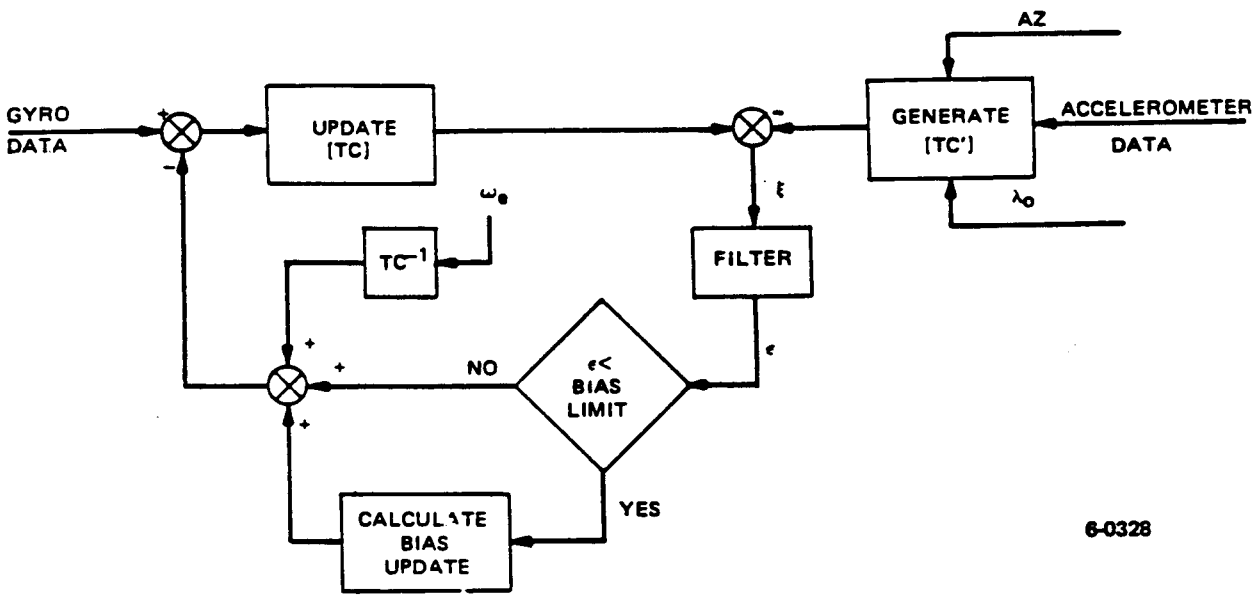


Figure 4.12.1-1. Alignment Loop

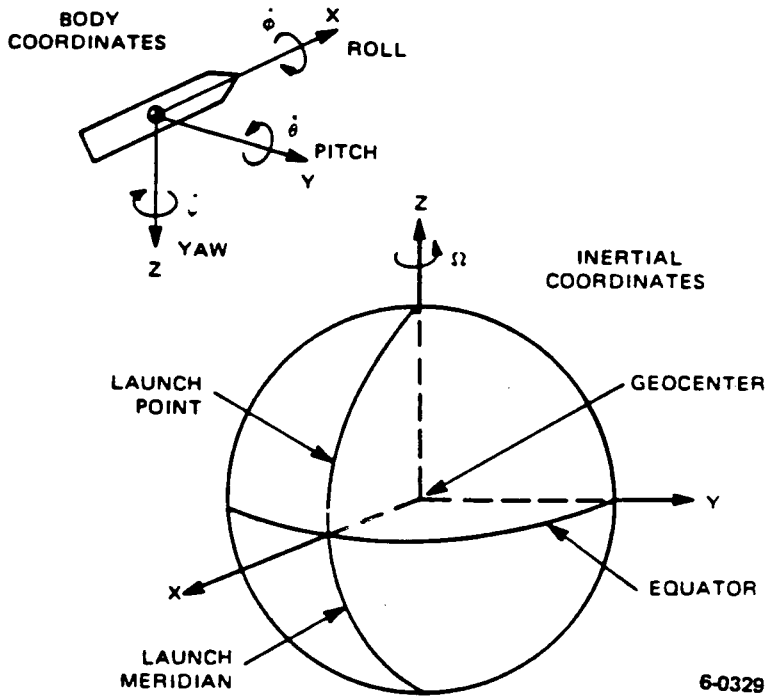


Figure 4.12.1-2. Coordinate Systems

To form the desired matrix, the accelerometer data are utilized to orient the body axes to the gravitational vector. The azimuth information orients the system with respect to the launch meridan, and the geodetic latitude is used to rotate from launch site coordinates to equatorial coordinates. Only the necessary matrix elements are generated from these data to allow defining the off-diagonal error terms when multiplied by the inverse of the TC matrix.

Accelerometer data are averaged over a short time (0.2 seconds) to reduce the effects of pulse moding on these matrix elements. The equations for this portion of the alignment process, including the error signal generation, are provided below.

For accelerometer summing,

$$SV(j) = SV(j) + \varepsilon VB(j)$$

$$j = x, y, z$$

For TC matrix element generation;

$$SV = [\Sigma\, SV(j)^2]^{1/2}$$

$$\begin{bmatrix} F_{31} \\ F_{32} \\ F_{33} \end{bmatrix} = (1/SV) \begin{bmatrix} SV(x) \\ SV(y) \\ SV(z) \end{bmatrix}$$

Since SV is required only for computations of the F_{3i} (i = 1, 2, 3) parameters, a solution was achieved which involved use of the available SV^2, thus completely avoiding the need for SV.

In the alignment equations the exact value of F_{31} was given as

$$F_{31} = SV(x)/SV$$

which may be rewritten as

$$F_{31} = SV(x)/(SV^2)^{1/2}$$

Squaring both sides yields

$$F_{31}^2 = SV(x)^2/SV^2 = X^2$$

So that the function of interest becomes

$$f(X) = F_{31} = (F_{31}^2)^{1/2} = Y^{1/2}$$

The Taylor series expansion for f(X) about X_o is given by

$$f(X) = F(X_o) + f'(X_o)(X-X_o) + f''(X_o)(X-X_o)^2/2! + \ldots$$

where the primes (') indicate derivatives.

During alignment, the primary component of gravitational force is sensed by the X axis accelerometer so that

$$SV(X)/SV \simeq 1$$

We may, therefore, apply the Taylor series expansion about $X_o = 1$. Evaluating the derivatives at X_o we obtain

$$f(X_o) = 1$$

$$f'(X_o) = (1/2)\, Y^{-(1/2)} = 1/2$$

$$f''(X_o) = -(1/4)\, Y^{-(3/2)} = -1/4$$

so that

$$f(X) = 1 + 0.5\,(Y-1) - 0.125\,(Y-1)^2 + \ldots$$

The $(Y-1)^n$ terms will be insignificant since Y = 1, therefore

$$F_{31} \simeq f(X) = 1 + 0.5\,(Y-1) = 0.5\,(1 + Y) = 0.5\left(1 + \frac{SV(X)^2}{SV^2}\right)$$

so that a solution for F_{31} is possible by using SV^2 directly.

In the alignment equations development, F_{32} and F_{33} are given by

$$F_{32} = SV(y)/SV$$

$$F_{33} = SV(z)/SV$$

Substitution to make use of F_{31} yields

$$F_{32} = \frac{SV(y)}{SV(x)} F_{31}$$

$$F_{33} = \frac{SV(z)}{SV(x)} F_{31}$$

Restating for clarity:

$$\begin{matrix} F_{31} \\ F_{32} \\ F_{33} \end{matrix} = \begin{bmatrix} (1 + SV(x)^2/SV^2) \text{ X } 0.5 \\ (F_{31}/SV(x) \quad) \text{ X } SV(y) \\ (F_{31}/SV(x) \quad) \text{ X } SV(z) \end{bmatrix}$$

Next, it is desired to simplify

$$A = (1 - F_{33}^2)^{1/2}$$

The approximation for the parameter A follows the same basic approach as above. Starting with

$$A = (1 - F_{33}^2)^{1/2}$$

as the exact solution, we square both sides to get

$$A^2 = 1 - F_{33}^2$$

then

$$f(X) = A = (A^2)^{1/2} = Y^{1/2}$$

Since F_{33} is small, the value of A approaches 1; therefore, we may again use the Taylor series expansion about $X_o = 1$. Because of the similarity to the above derivation, we see that the derivatives used in the series are identical. As a result, we may again make the appropriate substitution to obtain

$$A = f(X) = 1 + 0.5\ (Y - 1) = 0.5\ (1 + Y) = 0.5\ (1 + 1 - F_{33}^{\ 2})$$

$$= 0.5\ (2 - F_{33}^{\ 2}) = 1 - 0.5\ F_{33}^{\ 2}$$

which yields the desired approximation for A without having to take the square root of the A^2.

$$A = 1 - 0.5\ F_{33}^{\ 2}$$

$$TC_{23}' = A \sin AZ$$

$$F_{23} = A \cos AZ$$

$$F_{22} = (TC_{23}'F_{31} + F_{23}\ F_{32}\ F_{33})/A^2$$

$$TC_{22}' = F_{23}\ F_{31} - TC_{23}'\ F_{32}\ F_{33})/A^2$$

$$TC_{12}' = -F_{22} \sin \lambda_o + F_{32} \cos \lambda_o$$

$$TC_{32}' = F_{22} \cos \lambda_o + F_{32} \sin \lambda_o$$

$$TC_{13}' = -F_{23} \sin \lambda_o + F_{33} \cos \lambda_o$$

$$TC_{33}' = -F_{23} \cos \lambda_o + F_{33} \sin \lambda_o$$

$$\varepsilon N(x) = TC_{13}'TC_{12} + TC_{23}'TC_{22} + TC_{33}'TC_{32}$$

$$\varepsilon N(y) = -\ (TC_{13}'TC_{11} + TC_{23}'\ TC_{21} + TC_{33}'\ TC_{31})$$

$$\varepsilon N(z) = TC_{12}'TC_{11} + TC_{22}'\ TC_{21} + TC_{32}'\ TC_{31}$$

Solution of the exact F_{22} and T_{22}' equations would require multiplication of A by itself and then division into other quantities. An approximation for $1/A^2$ was found which would require the use of only a multiplication and an addition, as explained below. The method is the simplest approach to the approximation used. From

$$A^2 = 1 - F_{33}^{\ 2}$$

it follows that

$$1/A^2 = 1/(1 - F_{33}^{\ 2})$$

Performing the division on the right side of the above equation results in

$$1/A^2 = 1 + F_{33}^{\ 2} + \frac{F_{33}^{\ 4}}{1 - F_{33}^{\ 2}}$$

But since F_{33} is small, $1 - F_{33}^2$ approaches the value of 1 and F_{33}^4 is negligibly small. Therefore

$$1/A^2 = 1 + F_{33}^2$$

Since the quantity F_{33}^2 is already available from an intermediate step in the solution of A, it does not need to be re-computed. Thus, we simply add 1 to the available F_{33}^2 and use the result as a multiplier for the F_{33}^2 and T_{22}' equations.

The error signals described above are filtered with a second order recursive digital filter which employs the appropriate loop gains, K_{A1} and K_{A2}. When the sum squared value of these errors is sufficiently small, indicative of a small alignment error, the alignment errors are integrated and longitudinal axis gyro mass unbalance correction is updated as a function of the computed bias. By closing the loop with appropriate gains for the summed errors as well as the alignment errors, all system biases will show up as steady state values of these summed errors. Finally, to complete the alignment signal and allow the TC matrix to follow an earth-rate rotating coordinate system up to launch, earth rate is added into the alignment computations. It should be noted that by following this rotating coordinate system the actual TC matrix elements will remain constant except for local disturbances. The equations for this portion of the alignment loop are the following:

A. Alignment error equation:

$$\begin{bmatrix} \varepsilon(x) \\ \varepsilon(y) \\ \varepsilon(z) \end{bmatrix}_n = KA1 \left\{ \begin{bmatrix} \varepsilon N(x) \\ \varepsilon N(y) \\ \varepsilon N(z) \end{bmatrix}_n + \begin{bmatrix} \varepsilon N(x) \\ \varepsilon N(y) \\ \varepsilon N(z) \end{bmatrix}_{n-1} \right\} - KA2 \begin{bmatrix} \varepsilon(x) \\ \varepsilon(y) \\ \varepsilon(z) \end{bmatrix}_{n-1}$$

B. Bias update equation:

If $\varepsilon(x)^2 + \varepsilon(y)^2 + \varepsilon(z)^2$ is less than a preset lower limit, then

$$\begin{bmatrix} B(x) \\ B(y) \\ B(z) \end{bmatrix}_n = \begin{bmatrix} B(x) \\ B(y) \\ B(z) \end{bmatrix}_{n-1} + K_c \begin{bmatrix} \varepsilon(x) \\ \varepsilon(y) \\ \varepsilon(z) \end{bmatrix}_n$$

C. Final feedback correction equation:

In all cases

$$\begin{bmatrix} \varepsilon\phi A \\ \varepsilon\theta A \\ \varepsilon\psi A \end{bmatrix} = \omega_e \tau_1 \begin{bmatrix} TC_{31} \\ TC_{32} \\ TC_{33} \end{bmatrix} + \begin{bmatrix} \varepsilon(x) \\ \varepsilon(y) \\ \varepsilon(z) \end{bmatrix}_n + \begin{bmatrix} B(x) \\ B(y) \\ B(z) \end{bmatrix}_n$$

The alignment loop is discontinued at the time of liftoff; however, the bias update terms are left in the system for compensation during flight.

4.12.1.3.1.2 Position Tracking. The present vehicle position and velocity are initialized at first stage ignition to the vehicle position and velocity on the launch pad in the computational coordinate system. Since this system rotates with the vehicle until liftoff occurs, this will be the correct inertial position and velocity of the vehicle at liftoff. Also input is the initial velocity gain increment over one guidance compute cycle resulting from the effect of gravity at the launch pad. When liftoff is detected, the inertial velocity data from navigation are added to the velocity gain due to gravity to generate the total velocity change over the guidance compute cycle. This is then added to the initial velocity to generate the new present velocity. A trapezoidal integration of the velocity data is used to generate the present vehicle position. These operations are shown in block diagram form in Figure 4.12.1-3. The equations for these operations are the following:

$$\Delta\bar{V}_N = \Delta\bar{V}_A + \Delta\bar{V}_G \tag{1}$$

$$\bar{P}_{N_n} = \bar{P}_{N_{n-1}} + \left[\bar{V}_{N_{n-1}} + \frac{1}{2}\Delta\bar{V}_N\right]\tau_c \tag{2}$$

$$\bar{V}_{N_n} = \bar{V}_{N_{n-1}} + \Delta\bar{V}_N \tag{3}$$

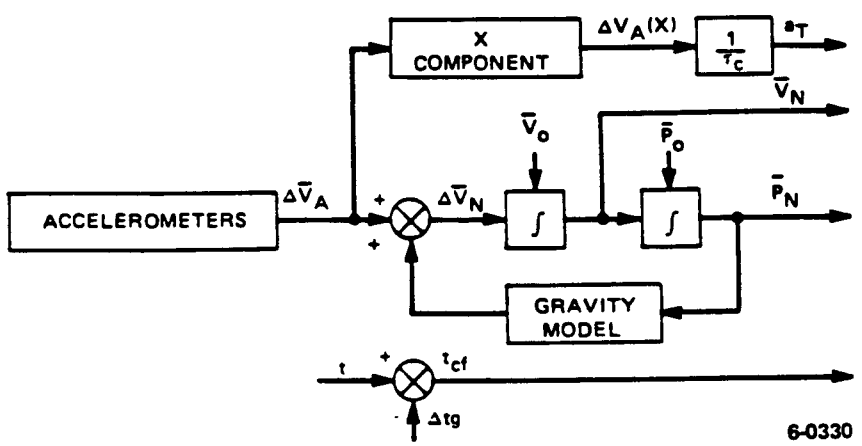


Figure 4.12.1-3. Navigation Block Diagram

From the position value obtained from Equation 2, a new value of ΔV_G is calculated by first using an oblate earth gravity model to compute the current value of the gravitational acceleration vector components. The gravity model is described below.

The square of the current radius vector is defined as

$$R_N^2 = \sum_{i=x,y,z} P_{Ni}^2 \tag{4}$$

from which a solution for the inverse radius $1/R_N$ must be obtained. To avoid use of a time consuming square root algorithm, a normalized function of the inverse of R_N was formed whose solution yielded the approximation

$$R_I = \frac{1}{8}\left[3 + \frac{R_x^2}{R_N^2}\left(6 - \frac{R_x^2}{R_N^2}\right)\left(\frac{1}{R_x}\right)\right] \tag{5}$$

where R_x is a reference normalizing radius applicable for a span of R_N values. Three sets of R_x and $1/R_x^2$ are input as mission constants for separate ranges of the ascent trajectory. The derivation of the R_I approximation is shown in Section 4.12.1.3.1.1. A plot of the acceleration errors resulting from use of the approximation in the preliminary trajectory is shown in Figure 4.12.1-4. The 2 discontinuities in the figure result from introduction of updated values of R_x^2 and $1/R_x$ via the mission constants; the zero crossings are the specific points for which the values were derived.

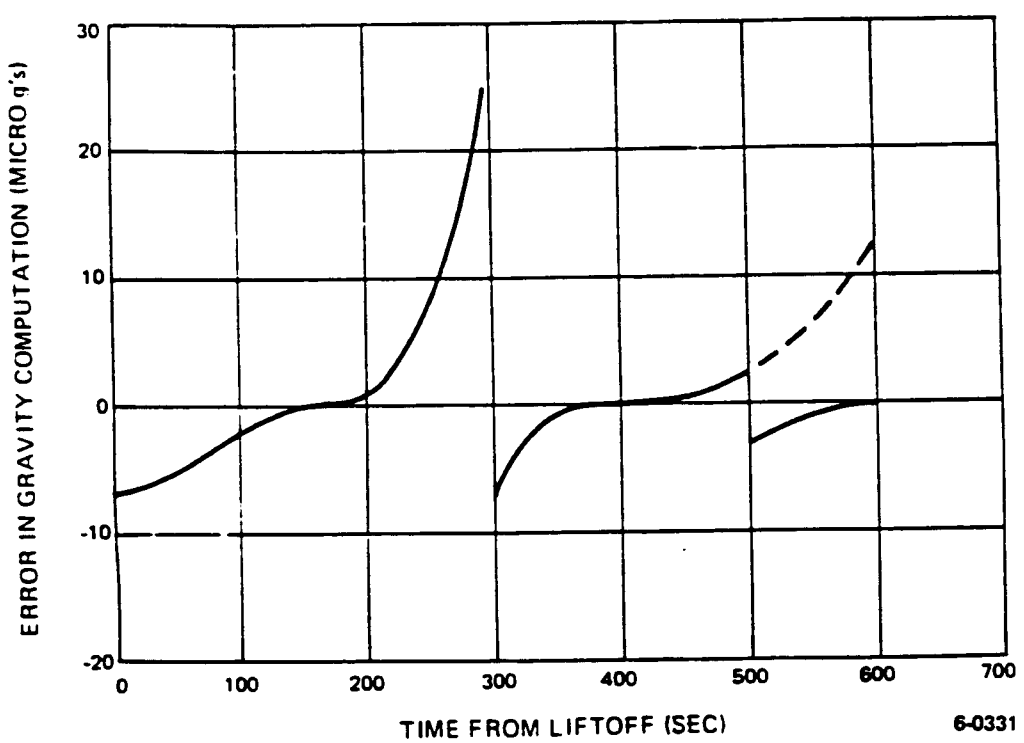


Figure 4.12.1-4. Gravity Error Due to Square Root Approximation (TIROS-N SAR)

For the Titan II ascent phase the position at approximately TBD seconds was used, since that was the point at which gravity was approximately the average value for the time span shown. The second set of R_x^2 and $1/R_x$ used was applicable for the time span from TBD seconds to TBD seconds, with an average value at about TBD seconds. This set of values is introduced at the start of the accelerometer synchronization guidance mode. The last set of R_x^2 and $1/R_x$ is inserted at the start of the coast adjust guidance mode at about TBD seconds and is valid for the remainder of the guided phases. The greatest accuracy for this last set is in the region encompassing AKM burn and the hydrazine velocity correction. A slight overlap is shown in the region of TBD to TBD seconds for information only.

It can be seen that the acceleration errors resulting from the approximation are negligible, never exceeding 26 x 10^{-6} g's.

A normalized current radius vector is found as

$$R = \bar{R}_I \, \bar{P}_N \tag{6}$$

which is used in the primary gravity model equation to compute the gravitational acceleration vector components

$$\bar{g} = \frac{(-GM)\,\bar{R}}{R_N^{\,4}} \left[R_N^{\,2} + (-1.5\ J_2\ R_o^{\,2})\ (5\ \frac{P_{Nz}^{\,2}}{R_N^{\,2}} - 1) \right] \tag{7}$$

where GM is the product of the gravitational constant and earth mass, J_2 is the second zonal harmonic, and R_o is the equatorial radius of the earth model employed. The product $(-1.5\ J_2\ R_o)$ is input as a mission constant. Mechanization of Equation 7 in the software was accomplished in several steps designed for computational expediency. As a last step in the gravitational model, the z component of gravity is modified to the following value

$$g_z = f_z + \frac{2\ R_z\ GM}{R_N^{\,4}}\ (-1.5\ J_2\ R_o) \tag{8}$$

$\Delta\bar{V}_G$ is then updated using

$$\Delta\bar{V}G = \frac{\tau c}{2}\ (3\bar{g}_n - \bar{g}_{n-1}) \tag{9}$$

where τ_c is the compute interval.

Equation 9 is a linear prediction of the average gravity over the next compute cycle integrated over 1 compute cycle. The prediction is necessary because the gravity computation is made after the position computationN This value of $\Delta\bar{V}_G$ is then used in Equation 1 on the next cycle.

4.12.1.3.2 Sequencing

All vehicle and guidance operations are controlled by a computed time base referred to as t_{cf} time. This is the time which is used in all closed loop guidance computations involving present time and also in the sequencer. The closed loop guidance equations compute the nominal time-to-go to the end of the current stage as a measure of time remaining for required end conditions to be met. For the hydrazine velocity correction burn, the shut down time is modified on the basis of this time-to-go computation.

The t_{cf} time is the nominal stage end time minus the predicted time-to-go and is derived as follows:

$$t_{cf} = T_f - t_g = T_f - (T_f - t + \Delta t_g) \tag{10}$$

$$t_{cf} = t - \Delta t_g \tag{11}$$

Equation 11 is used to compute t_{cf} in the actual programmed equationsN The Δt_g term of Equation 10 is derived in Section 4.12.1.4.5.2 of the closed loop guidance equations. The Δt_g term is, of course, zero prior to initiation of closed loop guidance for a stage. Using the t_{cf} time in the predictor equations allows the prediction to be made for the predicted value of time-to-go.

The vehicle sequencer is the mechanization of the vehicle open loop program. The sequencer would fly a nominal vehicle into the proper orbit without the closed loop guidance system. The sequencer performs three functions; it issues the pre-programmed rate commands to the vehicle, it changes the control system gains, and it also issues the vehicle discretes (i.e., engine ignitions, stage separations, deployment sequences, etc.).

Because the acceleration profile used in the guidance predictor is based on the pre-programmed rate commands in the sequencer, these rate commands must be based on t_{cf} time so that the predictor will be correct. Section 4.12.4.5.3 provides a discussion of how t_{cf} is modified at the end of a stage so that the next stage will be ignited at the proper time and the other coast phase sequences will be performed properly.

For each of the three sequencer functions, the sequencer compares the t_{cf} time to the time of the next change in that function. When t_{cf} exceeds that time, the function is sequenced. Thus the sequencer can only run forward.

4.12.1.3.3 Controls

The controls function can be divided into two segments; the controls filter function and the attitude control function.

The control filter function was developed for NOAA-F to eliminate the control system/flexible body interactive coupling problem seen on the NOAA-E spacecraft during ascent. The controls filter is discussed in detail in Section 4.12.2.

The controls equations define the attitude error signal, resolve those signals from vehicle body axes to the thruster axes defined in Figure 4.12.1-5, and implement on-off control logic.

Attitude errors in the roll, pitch, and yaw channels are defined as the integrated differences between the vehicle filtered rates and the sums of the programmed and guidance commanded rates, in the following manner:

$$\Delta\bar{\theta}_n = \delta\bar{\theta}_{n-1} + \Delta\bar{\theta}_{B_F} - (\bar{\dot{\theta}}_p + \bar{\dot{\theta}}_g)\,\tau \qquad (12)$$

where the $\varepsilon\bar{\theta}_{B_F}$ vector notation is used to denote the 3 channels.

The programmed pitch and yaw rates are not resolved through the roll attitude error, since that error will be small during the periods in which programmed commands are applied. The above attitude error signals, as well as the $\varepsilon\bar{\theta}_{B_F}$ filtered body rates, are resolved from the body axes to thruster axes for subsequent use in the on-off control logic.

The on-off control logic provides for the phase plane switching logic shown in Figure 4.12.1-6 and is implemented with the equation logic flow depicted in Figure 4.12.1-7. Provisions are made in the sequencer to allow switching this logic to the appropriate test values depending on the time of flight. A separate set f test values may be used for the roll channel at the same time that another set is being used for the pitch and yaw channels.

Section 4.12.2 provides a detailed description of the control system and the on-off switching characteristics.

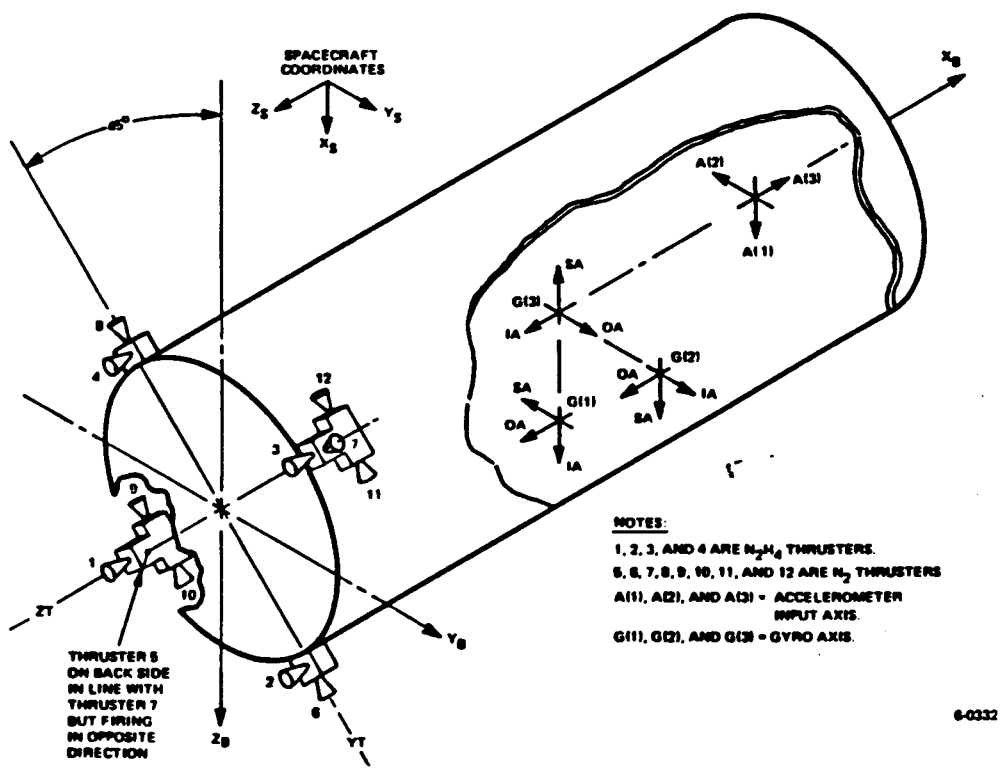


Figure 4.12.1-5. Coordinate Systems Detail-Thrusters

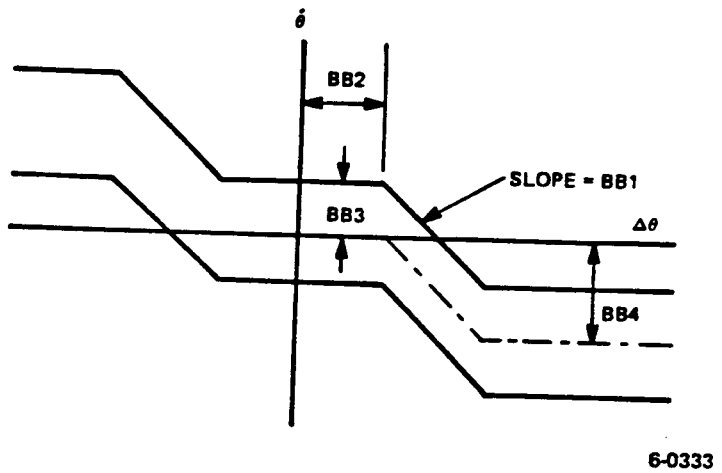


Figure 4.12.1-6. On-Off Phase Plane Description

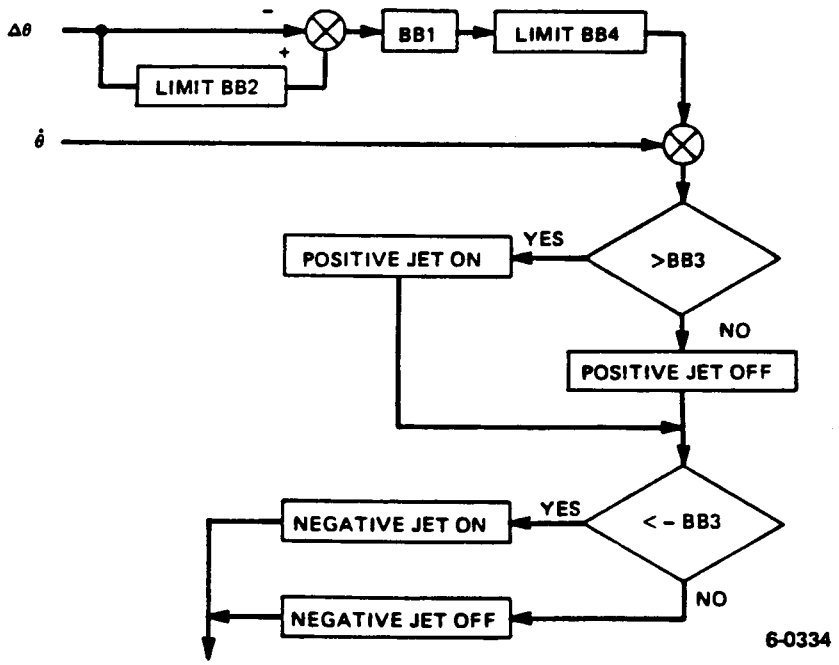


Figure 4.12.1-7. On-Off Control Logic

4.12.1.4 Closed Loop Guidance Equations

The guidance system will be used after separation from the Titan II booster to guide the vehicle upper stage to a pre-determined orbit. To accomplish this, several guidance modes will be employed individually at specific time spans along the post-separation trajectory.

The basic guidance procedure utilizes a nominal, reference trajectory which satisfies all system requirements as the source for targeting data. Since no pre-programmed attitude rates are scheduled during the powered flight phases, the reference trajectory shape ideally would not be modified during flight if all conditions remained nominal. However, perturbations and/or performance anomalies which drive the vehicle from its nominal path and the ensuing corrective guidance commands both tend to modify the trajectory.

AGS employs an explicit guidance policy during a coast adjust mode preceding the AKM burn, during the powered flight guidance modes which are active during AKM burn, and during a velocity correction hydrazine burn phase. This explicit policy compares the predicted and nominal vehicle positions and velocities at the end of the active stage and issues corrective attitude rate commands to the vehicle to steer it onto the nominal orbit at the end of the stage.

Two coordinate systems were used in the formulation of the guidance equations. These are the inertial (navigational) system and the body (vehicle) coordinate system, both of which are shown in Figure 4.12.1-2. The inertial system was defined in the alignment discussion of Section 4.12.3.3.

The body coordinate system is a right-handed Cartesian coordinate system centered at the IMU. The X axis is along the vehicle roll axis, positive toward the nose of the vehicle; the Y axis is the vehicle pitch axis, positive in the direction of an imaginary right wing; and the positive Z axis completes the orthogonal triad by pointing through the vehicle keel. Positive roll, pitch, and yaw rotations are defined along these respective positive body axes.

A detailed derivation of the closed loop guidance equations is presented in this section. Figure 4.12.1-8 shows the main flow of these equations in block diagram form.

4.12.1.4.1 Closed Loop Guidance Modes

A series of guidance modes is used to effect the closed loop guidance function. Brief descriptions of the general in-flight functions of these modes were given in Section 4.12.1; more definitive descriptions of the sequence and specific functions of these modes are presented below. Derivations of equations, in most cases, are deferred until later in this section.

Mode sequencing along the trajectory profile is shown pictorially in Figure 4.12.1-9. The specific mode sequence, approximate start and stop times, and the basic purpose of each mode are summarized in Table 4.12.1-1. Discussion of the software logic and mechanization details are presented in Section 4.12.4.

4.12.1.4.1.1 <u>Acceleration Synchronization Mode</u>. This mode is processed during one guidance cycle at a time point slightly earlier than the 3 sigma early Titan II sustainer engine cutoff (SECO). The measured thrust axis acceleration at that time point is compared with high and low limits of acceleration derived from the nominal trajectory to verify reasonable operation of the primary accelerometer.

Acceleration outside the expected limits is used as a failure indication for which alternate operation will be sequenced upon entry to the navigation fail/test guidance mode. Failure sequencing is discussed more in Section 4.12.3.

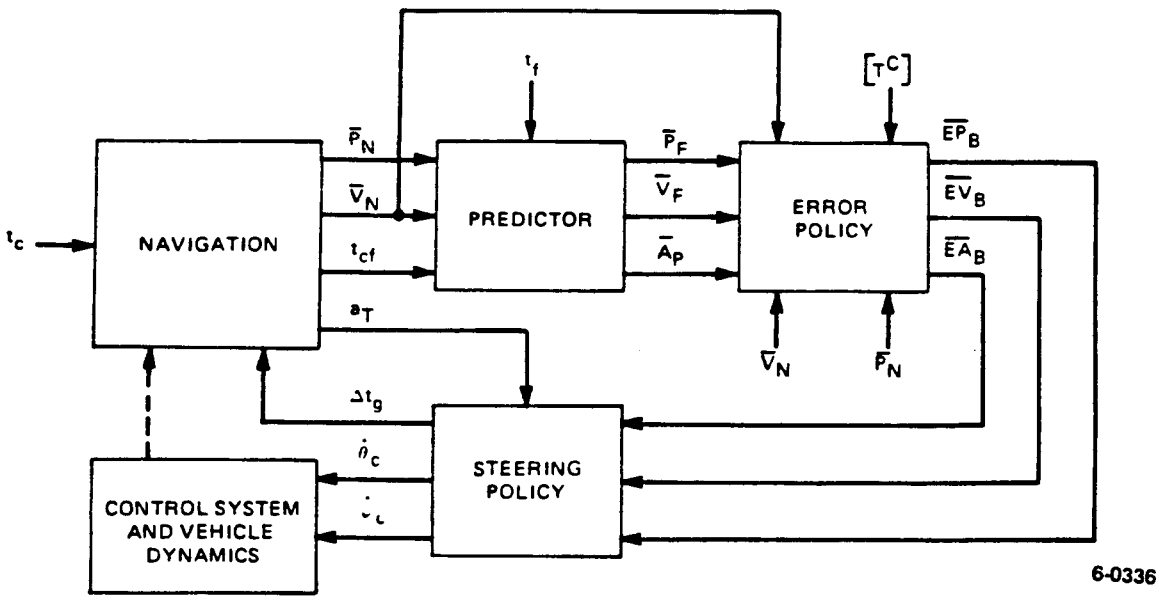


Figure 4.12.1-8. Simplified Guidance System Block Diagram

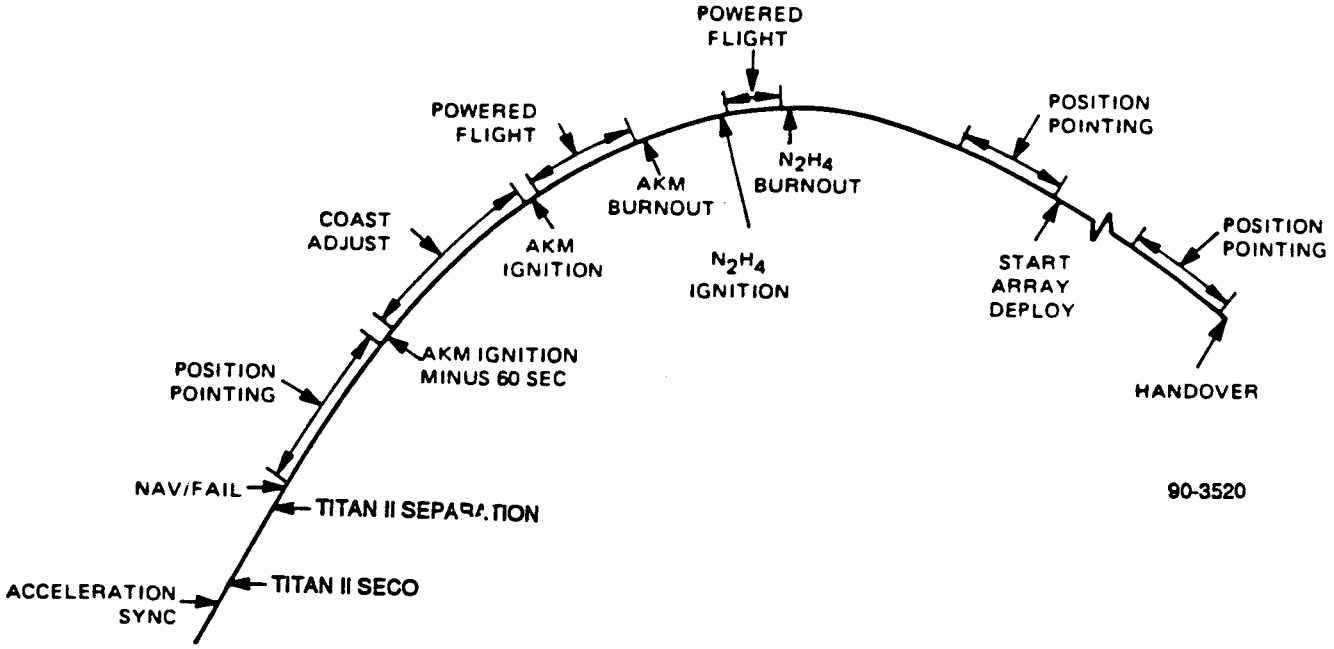


Figure 4.12.1-9. Guidance Mode Sequence

TABLE 4.12.1-1. GUIDANCE MODES (TBD)

Mode No.	Mode Type	Start Time From Liftoff	Start Time Relative To Event	Stop Time Relative To Event	Purpose
1	Accelerometer Sync	TBD	SECO TBD	SECO TBD	Test thrust axis accelerometer
2	Nav Test/Fail	TBD	Separation TBD	Separation TBD	Test navigation. Set up failure mode data
3	Position Pointing	TBD	Separation TBD	Separation TBD	Roll attitude fine point
4	Coast Adjust	TBD	AKM Ignition TBD	AKM Ignition TBD	AKM ignition time and attitude adjustment
5	Powered Flight	TBD	AKM Ignition TBD	AKM Burnout TBD	Guidance steering
6	Powered Flight	TBD	N_2H_4 Ignition TBD	N_2H_4 Burnout TBD	Guidance steering and N_2H_4 burnout adjustment
7	Position Pointing	TBD	N_2H_4 Venting TBD	N_2H_4 Venting TBD	Attitude fine pointing
8	Position Pointing	TBD	Handover TBD	Handover TBD	Attitude fine pointing

All times in seconds

Proper accelerometer operation triggers the setup of certain logic indicators and time parameters which allow proper sensing of Titan II SECO by the software, and allow proper synchronization of time functions to SECO.

The obvious assumption upon which this mode is based is that a faulty acceleration indication is due to a thrust axis accelerometer failure. This is justified on the basis that if the failure were due to any other source the mission would probably be lost, so an effort to salvage the mission is worthwhile in the event that the problem is due to accelerometer failure.

4.12.1.4.1.2 Navigation/Fail Test Mode. Entry to this mode is desirable approximately 2 seconds after separation from Titan II. To accomplish this in the eventuality of an abnormally long time sequence resulting from maximum delays in the Titan II SECO the targeted entry time is set at TBD seconds after nominal SECO.

Upon entry to this mode, the status of the thrust axis accelerometer is examined and, if satisfactory, a measure of navigation accuracy is made to determine if the Titan II VECO orbit is within the corrective capability of the second stage (the spacecraft). This determination is made using the parameter

$$\frac{GM}{a} = 2\ GM/R - V^2 \tag{13}$$

which was derived from the orbit energy equation

$$E = \frac{1}{2} V^2 - \frac{GM}{R} = - \frac{GM}{2a} \tag{14}$$

where R and V are the radius and velocity magnitudes at orbit injection, "a" is the orbit semi-major axis, E is the orbit specific energy, and GM is the earth constant resulting from the product of the earth mass and the gravitational constant.

If the vehicle is within the spacecraft corrective capability, this mode is terminated on the initial entry. If either a thrust axis accelerometer failure or navigation failure has occurred, provisions are made to: 1, initialize a position pointing guidance mode which will orient the vehicle in the desired separation attitude; and 2, continue the mission using open loop guidance, wherein nominal pre-programmed body rates and all nominal sequences are applied. The position pointing mode is processed until termination time established in the targeted data, so that under the failed conditions the navigation/fail test mode will actually last TBD seconds; however, the duration is determined by targeting constants and can be changed as needed.

Two underlying assumptions in the incorporation of this guidance mode are: 1, that open loop operation after either of the specified failures is detected provides a possibility of mission success; and 2, that gyro performance was not the cause of failure. The latter assumption is necessary because body rate application and vehicle control are dependent on gyro operation.

4.12.1.4.1.3 Roll Position Pointing Mode. If acceptable operation was verified by the previous mode, a position pointing mode is initiated about TBD seconds after the navigation/fail test mode has been completed. The purpose for this mode is to drive the vehicle to the desired roll orientation. This roll pointing is accomplished here, since no roll steering will be employed during the next three guidance modes. No pitch or yaw steering corrections are employed during this mode, since they are to be applied during all the remaining guidance modes.

4.12.1.4.1.4 Coast Adjust Mode. At approximately TBD seconds before the nominally scheduled ignition of the AKM stage, a coast adjust mode is initiated and is processed for approximately TBD seconds. Using most of the software designed for the ensuing powered flight modes, this mode determines the changes required to both the AKM ignition time and ignition attitude to compensate for anomalous Titan II performance. These adjustments are based on the assumption that AKM stage performance will be nominal.

Predictions of the vehicle position and velocity at AKM burnout are made by employing the powered flight mode predictor software, combined with a prediction of the vehicle state at AKM ignition.

4.12.1.4.1.5 Powered Flight Mode - AKM Burn Phase. One second after AKM ignition, the first powered flight mode is initiated. This mode will remain active until TBD seconds before the expected stage burnout, as determined by the guidance computations. Continuous comparisons of predicted and desired end conditions will be used to generate corrective steering commands.

Powered stages are the only means by which trajectory corrections can be made to compensate for non-nominal flight and, as such, are the primary reason for design of guidance software. The software implemented entails prediction of conditions at the end of a stage, provision of an error policy by which deviations from desired conditions may be determined, and generation of corrective steering commands based on the error policy.

The software employed for these functions is discussed in detail later in this section.

4.12.1.4.1.6 Powered Flight Mode - N_2H_4 Velocity Correction. Since shutdown of the AKM solid propellant motor cannot be commanded at a precise time, it may not be possible to achieve the desired orbit velocity at AKM burnout. Compensation for this shortcoming is made by a velocity correction burn using the hydrazine thrusters, for which shutdown can be commanded.

Ignition of the hydrazine thrusters for this mode of operation is accomplished via the control system switching constants at a specified time after AKM burnout. One second after ignition, powered flight guidance is again initiated and continues nominally until TBD seconds before hydrazine shutdown is commanded. Should the required velocity correction be such that engine cutoff is desired immediately, then guidance termination would occur within TBD second of cutoff.

Final orbit injection occurs at the end of the hydrazine thruster velocity correction burn.

4.12.1.4.1.7 Position Pointing Mode - Array Deployment. Shortly after orbit injection, open loop yaw and roll rates are applied to orient the vehicle in the approximate attitude desired for array deployment. About TBD seconds before the start of array deployment, a position pointing mode is initiated to trim the attitude to within the desired attitude tolerances; this mode will be in effect for TBD seconds. Roll commands will be superimposed on an open loop roll rate which will be applied until handover to keep the spacecraft X axis aligned with the Earth radius vector.

4.12.1.4.1.8 Position Pointing Mode - Handover. At approximately TBD seconds before handover, a final position pointing mode will be applied for a period of TBD seconds to trim the vehicle to the handover attitude requirement.

4.12.1.4.2 Powered Flight Predictor

The guidance policy is based on comparing the predicted vehicle position and velocity at the end of the active stage to the nominal values. To accomplish this, a means of predicting the vehicle state at the end of the stage based on its present state is required. This means is provided by the powered flight predictor.

The powered flight predictor provides the predicted position and velocity at stage shutdown and the present acceleration error. These calculations are based on the present position and velocity and the predicted time remaining to stage shutdown. Figure 4.12.1-10 shows the predictor in block diagram form.

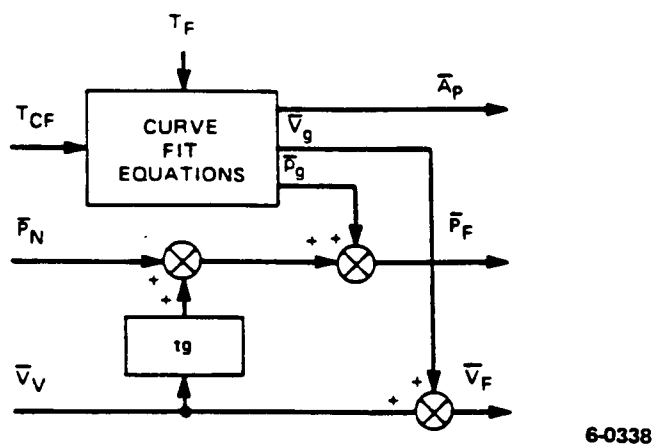


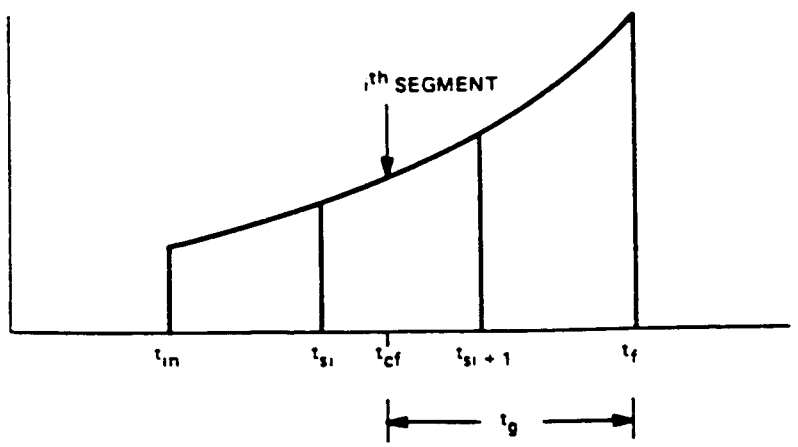
Figure 4.12.1-10. Powered Flight Predictor Block Diagram

The prediction of future vehicle states is achieved by means of a series of second order curve fits of the total nominal acceleration profile, including gravitational acceleration. The nominal acceleration profile along each inertial axis is curve-fit independently, using data from the nominal trajectory. The acceleration curves are separated into as many segments as necessary to achieve satisfactory accuracy with the second order constraint. Examination of the current trajectory indicates that two segments are adequate for the AKM stage and that one segment suffices for the velocity correction burn.

Over each of these segments, a second order curve fit is made which has the same predicted acceleration at the beginning of the segment as was predicted at the end of the adjacent segment; the time integral of the curve over the segment equals the nominal velocity to be gained over the segment due to acceleration. The double integral of the curve over the segment equals the nominal position to be gained over the segment due to the acceleration. The position and velocity to be gained are shown as separate entities in Figure 4.12.1-10 for clarity, but are implicit in the predicted position and velocity equations in the flight software.

The initial segment for each stage begins at approximately guidance initiation of that stage, and has as its initial acceleration the nominal acceleration at that time. Initial entry to the predictor is not made until guidance initiation, which occurs approximately 1 second after ignition.

As in ATN, the curve fit coefficients were based on time measured from the end of a given segment back to the current time. This method allows a closed form solution for position and velocity to go by using the closed form integral for position and velocity to be gained over the remainder of the current segment and adding to this the position and velocity to be gained over the remainder of the segments which are applicable to the active stage. Figure 4.12.1-11 shows typical curve fit segments within a typical acceleration history; the labeling of the various times should aid in understanding the derivation which follows as well as the overall time relationships.



- SECOND ORDER FIT TO INERTIAL ACCELERATION
  $A = a + b(t_{cf} - t_{si+1}) + c(t_{cf} - t_{si+1})^2$
- ACCELERATION AT START OF ith SEGMENT EQUALS ACCELERATION AT END OF i-1 SEGMENT
- INTEGRAL EQUALS VELOCITY TO BE GAINED
- SECOND INTEGRAL EQUALS POSITION TO BE GAINED

6-0339

Figure 4.12.1-11. Acceleration Curve Fits

The basic time used in the curve fit computations is

$$\Delta t = t_{cf} - t_{i+1} \tag{15}$$

which takes on negative values since t_{i+1} is the time at the end of the active segment.

The curve fit segment end times are input as time from liftoff, and t_{cf} is used to determine the curve fit segment to be used as well as to determine the time remaining within a segment. The time span over a complete segment is

$$\Delta t_i = t_i - t_{i+1} \tag{16}$$

which will also be negative.

It should be noted that definition of Δt as the ultimate time to be used allows use of forward integrations in the derivations even though the acceleration integrals of interest are actually backwards from the segment end time to current time. Letting t denote any general time point, the second order acceleration curve fit equation is

$$A = a + bt + ct^2 \tag{17}$$

The velocity and position integrals over the Δt time span remaining in the ith curve fit segment are

$$\Delta V_s = \int_{\Delta t}^{o} (a_i + b_i t + c_i t^2) dt \tag{18}$$

and

$$\Delta P_s = \int_{\Delta t}^{o} \int_{\Delta t}^{t} (a_i + b_i \tau + c_i \tau^2) d\tau \, dt \tag{19}$$

where t and τ represent times measured from the start of the segment. Integrating these equations in a straightforward manner, and temporarily dropping the i subscript for brevity, yields

$$\Delta V_s = -\Delta t(a + 1/2b\Delta t + 1/3c\Delta t^2)$$

and

$$\begin{aligned} \Delta P_s &= (1/2at^2 + 1/6bt^3 + 1/12ct^4) \Big|_{\Delta t}^{o} \\ &\quad - (at\Delta t + 1/2bt\Delta t^2 + 1/3ct\Delta t^3) \Big|_{\Delta t}^{o} \\ &= \Delta t^2(1/2a + 1/3b\Delta t + 1/4c\Delta t^2) \end{aligned}$$

Letting

$$\Delta t_i = t_i - T_{i+1}$$

as previously stated in Equation 16 and changing the Δt in the limits of Equations 18 and 19 to Δt_i results in the following position and velocity to be gained over an entire segment.

$$\Delta Vg_i = -\Delta t_i(a_i + 1/2b\Delta t_i + 1/3c\Delta t_i^2) \tag{20}$$

and

$$\Delta Pg_i = \Delta t_i^2(1/2a_i + 1/3b_i\Delta t_i + 1/4c_i\Delta t_i^2) \tag{21}$$

The acceleration at the start of the segment may also be expressed as

$$A_i = a_i + b\Delta t_i + c\Delta t_i^2 \tag{22}$$

which follows directly from Equations 16 and 17. In view of the definition of Δt_i it can be seen that $a_i = A_{i+1}$, i.e., the a_i coefficient is equal to the acceleration at the end of the segment, and the solution of Equation 22 will yield the acceleration at the start of the segment. Simultaneous solution of Equations 20 and 22 yields the following desired coefficients for the ith segment

$$c_i = \frac{6}{\Delta t_i^2}\left(A_i - \frac{2\Delta V_{g_i}}{\Delta t_i} - \frac{6\Delta P_{g_i}}{\Delta t_i^2}\right)$$

$$b_i = 2\left(\frac{A_i}{\Delta t_i} + \frac{\Delta V_{g_i}}{\Delta t_i^2} - \frac{4}{3}c\Delta t_i\right)$$

$$a_i = A_i - b_i\Delta t_i - c_i\Delta t_i^2$$

Thus, solutions for P_s, V_s, ΔPg_i and ΔVg_i can be obtained from the coefficients.

The total velocity and position to go to the end of the stage can then be solved as follows:

$$V_g = V_s + \sum_{J=i+1}^{M-1} \Delta Vg_j$$

$$P_g = P_s + \sum_{J=i+1}^{N-1} \Delta Pg_j + \sum_{J=i+1}^{N-2} \Delta Vg_j\,(t_{j+1} + t_j) + V_s(T_f - t_{i+1})$$

where N denotes the number of segments used for the active stage.

The final position and velocity at the end of the stage can then be predicted from

$$P_f = P_N + V_N t_g + P_g$$

$$V_f = V_n + V_g$$

The predicted acceleration may be computed directly from Equation 17 by making the obvious substitution of Δt for t. Acceleration error may then be found by subtracting the current measured inertial acceleration from the predicted value. The measured inertial acceleration is determined by combining the measured incremental velocity change over a half-second guidance interval with the computed velocity change resulting from gravitational acceleration over that same interval. Thus

$$\bar{A}_{meas} = (\Delta\bar{V}_m + \Delta\bar{g}/0.5)/0.5 = 2\Delta\bar{V}_N$$

so that

$$\Delta\bar{A} = \bar{A}_{pred} - 2\Delta\bar{V}_N$$

The accuracy of the curve fits described in this section is discussed in Section 4.12.1.5.

4.12.1.4.3 Alternate Predictor for Hydrazine Velocity Correction Phase

The powered flight predictor is applicable to the AKM stage burn phase and can also be used for the velocity correction hydrazine burn phase. However, because the gravitational acceleration is much larger than the thrust acceleration during this latter phase, concern arose that the predicted acceleration vector would be pointing in the wrong direction if the Δt_g and Δt_{orb} adjustments were significantly large. The problem emanates from the fact that the curve fit acceleration is predominantly the gravitational component and an error in this parameter could cause a significant error in the corrective velocity component. To avoid this problem, an alternate predictor was designed for the hydrazine burn phase.

Figure 4.12.1-12 contains an exaggerated geometric description of the problem posed above. As an example, for a 450 nmi orbit altitude, a combined Δt_g and Δt_{orb} adjustment of 30 seconds would result in approximately a 1.8 degree error in the gravitational acceleration vector direction with an ensuing Δg error of about 0.8 ft/sec/sec. This acceleration error is approximately one-fourth the magnitude of the hydrazine phase thrust acceleration.

The alternate predictor was configured as described below. Computation of the gravitational acceleration, $\underline{g}_f$, at the predicted burnout position allows combination with the current gravitational acceleration vector, $\underline{g}_N$, to arrive at the average gravity during the expected remaining hydrazine burn phase. This vector may be added to the thrust acceleration, a_H, to obtain an estimate of

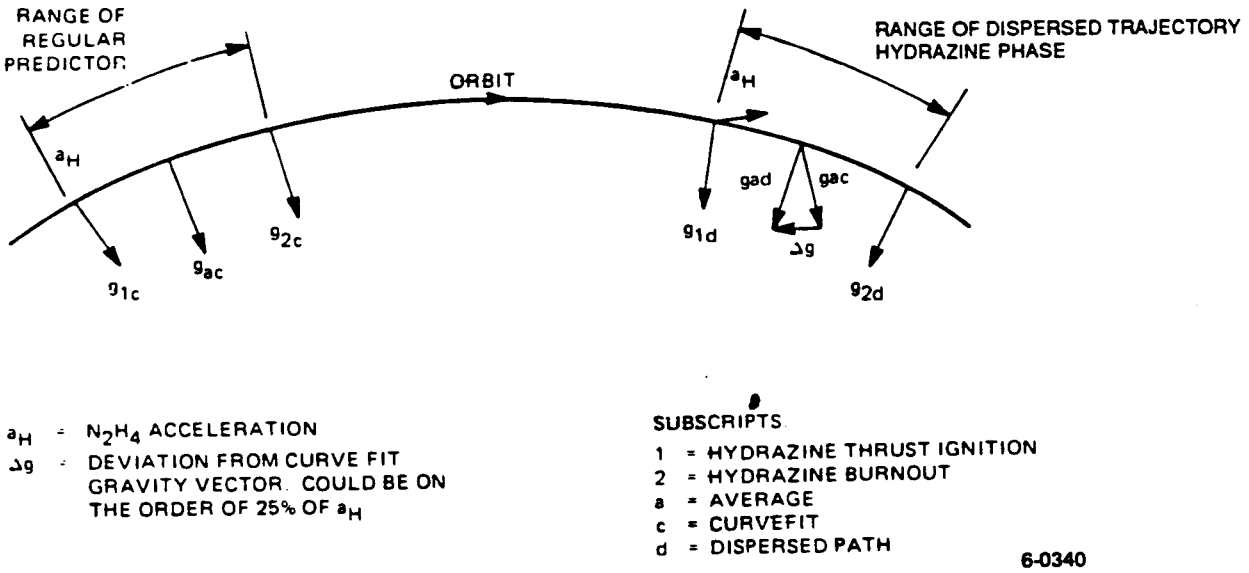


Figure 4.12.1-12. Need for Alternate Predictor

the net predicted acceleration for the remainder of the burn if no guidance commands were issued, i.e.,

$$\bar{a}_p = 0.5\ (\bar{g}_N + \bar{g}_f) + \bar{a}_H$$

Simple integrations of this acceleration over the remaining time to go to burnout may be combined with the current position and velocity to arrive at the predicted burnout position and velocity.

$$\bar{P}_f = \bar{P}_N + \int_o^{t_g} V_N dt + \int_o^{t_g} \int_o^{\tau} \bar{a}_p dt\ dt$$

and

$$\bar{V}_f = \bar{V}_N + \int^{t_g} \bar{a}_p\ dt$$

The acceleration error, i.e., the difference between the predicted and measured total accelerations, is simply

$$\Delta\bar{a} = \bar{a}_p - \bar{a}_{meas}$$

This parameter is required for ultimate use in determining the time adjustment, Δt_g, required to determine the hydrazine burnout time.

4.12.1.4.4 Guidance Error Policy

A guidance error policy must be employed during powered flight to establish an appropriate set of vehicle state error parameters suitable for generation of corrective guidance commands by the guidance steering policy. The error and steering policies are highly interdependent because the error policy cannot control more variables than the steering policy can accommodate. The steering policy is, in turn, constrained by the physical characteristics of the vehicle. During the AKM solid motor burn, the limitations of the vehicle allow a steering law which can control only velocity deviations along the vehicle pitch and yaw axes by issuing pitch and yaw rate commands. The assumption is made that the solid motor burnout time can be altered and that, as a result, velocity along the roll axis can be controlled. Since this assumption is not realizable, the deviation between the desired and actual burnout times will perpetuate into a velocity error which must be compensated during the ensuing hydrazine powered burn phase. During the hydrazine phase, the same type of velocity correction capability along the pitch and yaw axes exists but, in addition, the velocity along the roll axis is controllable by controlling the shutdown time of the hydrazine thrusters.

With the above limitations in mind, it is possible to formulate an error policy which places the vehicle near the nominal orbit. Because both position and velocity control are not available along the roll axis of the vehicle, it is not possible to enter the nominal orbit at the nominal injection point in the presence of perturbations. However, there are a number of possible position and velocity combinations that will place the vehicle on the desired orbit. The error policy selects a new desired orbit injection point on the nominal orbit based on the predicted position of the vehicle at the end of the current stage and then adjusts (in the case of the hydrazine powered phase) the velocity so as to match the orbit velocity at that point. It is again stressed that the velocity adjustment which is achieved by altering burnout time is not possible for the AKM burn.

By using targeted values of nominal injection position and velocity, and bearing in mind that only gravitational acceleration is present after burnout, the new desired burnout aim-point can readily be defined as a function of the time increment, Δt_{orb}, along the nominal orbit. Thus,

$$\bar{V}_d = \bar{V}_t + \int_o^{\Delta t_{orb}} \bar{g}_a \, dt = \bar{V}_t + \bar{g}_a \Delta t_{orb} \tag{23}$$

where $\bar{g}_a$ is the average gravitational acceleration between the targeted and the newly desired injection position. A similar approach using the double integral of $\bar{g}_a$ yields

$$\bar{P}_d = \bar{P}_t + \bar{V}_t \, \Delta t_{orb} + \frac{1}{2} \bar{g}_a \, \Delta t_{orb}^{\,2}$$

A geometric description which will aid discussion of the error policy is shown in Figure 4.12.1-13. Since only the targeted and predicted positions and veloc- ities are initially available, they may be used to estimate the initial value of Δt_{orb} before the above equations are solved. The deviation between the predicted and targeted positions are

$$\Delta\bar{P}_o = \bar{P}_f - \bar{P}_t$$

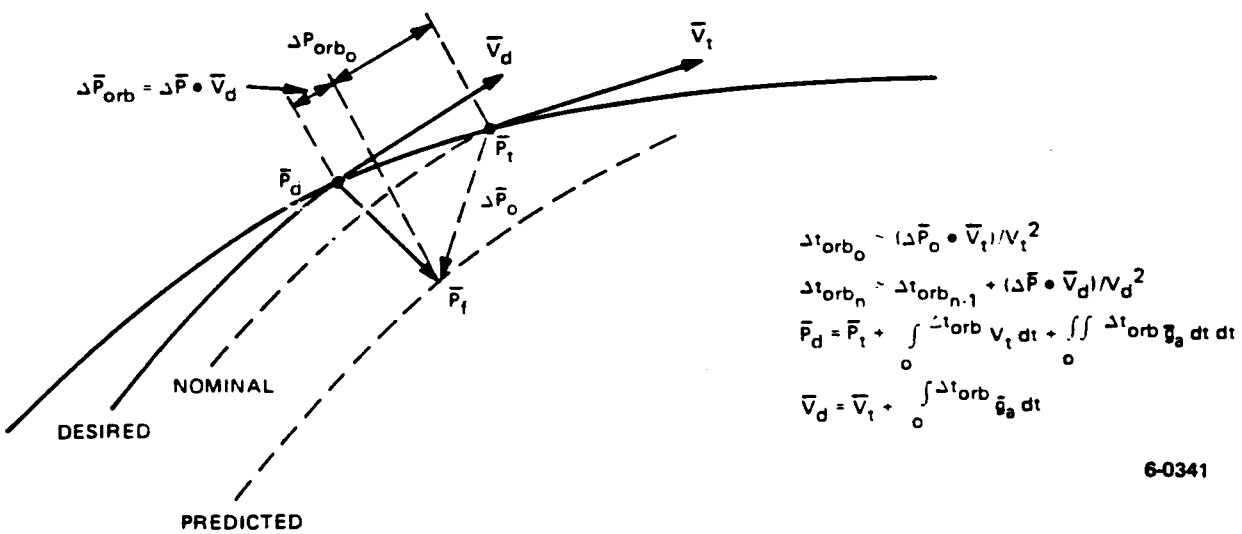


Figure 4.12.1-13. Error Policy Geometry

It is apparent that, if the predicted and nominal orbits are close, the targeted velocity vector integrated over the time separation between $\bar{P}_f$ and $\bar{P}_t$ along the desired orbit will yield the ΔP_o component on the orbit path. Because the velocity vector is very nearly tangent to the orbit path for a circular orbit, the $\Delta\bar{P}_o$ projection on $\bar{V}_t$ will very nearly lie on the orbit path. This projection may be computed as the vector dot product of $\Delta\bar{P}_o$ with a unit vector in the $\bar{V}_t$ direction, i.e.,

$$\Delta P_{orb_o} = \Delta\bar{P}_o \cdot (\bar{V}_t/|\bar{V}_t|)$$

From the basic assumption that Δt_{orb} will be the time required to traverse ΔP_{orb} with the velocity V_t, we see that

$$\Delta t_{orb_o} = \Delta P_{orb_o} \; / \; |\bar{V}_t|$$

$$= [\Delta \bar{P}_o \cdot (\bar{V}_t \; / \; |\bar{V}_t|)] \; / \; |\bar{V}_t|$$

$$= (\Delta \bar{P}_o \cdot \bar{V}_t) \; / \; |\bar{V}_t|^2$$

After the initial solution is made for $\bar{P}_d$ and $\bar{V}_d$, these desired quantities will be the new targeted position and velocity and the updated values are used to determine new increments of Δt_{orb} between the updated predicted and target points. These increments are added to the previous solution to maintain the updated value.

$$\Delta t_{orb_n} = \Delta t_{orb_{n-1}} + (\Delta \bar{P} . \bar{V}_d) \; / \; |\bar{V}_d|^2 \qquad (24)$$

For simplicity in solving Equation 24, a useful approximation is

$$|\bar{V}_d| \simeq |\bar{V}_t|$$

since the velocity magnitude for a given circular orbit will not change appreciably, especially for the relatively small position changes anticipated. Hence, the inverse of the square of the targeted velocity may be used as a constant in Equation 24.

When a new value of $\bar{V}_d$ is found using Equation 23, it may be combined with the current $\bar{V}_f$ from the predi or to generate a current estimate of inertial position error, $\Delta\bar{V}$. This error, along with the current acceleration error, may then be transformed to body coordinates in order to represent the errors along the vehicle control axes. In this form, the errors may be used to generate corrective steering commands in the manner to be discussed later.

4.12.1.4.5 Steering Policy and Time-To-Go Change

Steering control on the vehicle is obtained by the use of on/off sequences of nitrogen or hydrazine thrusters; roll control is always achieved with nitrogen thrusters. Turn on of hydrazine thrusters is used for pitch and yaw control starting at the coast period shortly before AKM ignition, through AKM burn, and during the coast period before the hydrazine corrective velocity phase. During the velocity correction hydrazine burn, turn off of the hydrazine thrusters is used to achieve pitch and yaw steering control. During the periods not stated above, the nitrogen thrusters are used for pitch and yaw control.

As previously mentioned, AKM motor shutdown cannot be commanded by the guidance system; it is assumed that stage shutdown will occur as predicted by the time to go equation. Shutdown of the hydrazine thrusters during the velocity correction burn is guidance commanded as determined by the time to go computations.

4.12.1.4.5.1 Steering Policy. The lateral steering policy is a derivative of a policy previously developed at MDAC as a compromise between simplicity and minimum performance losses from guidance commanded maneuvering. This lateral steering law is designed to remove the velocity errors in the pitch and yaw planes by the end of the stage, to place the vehicle on the nominal orbit. Derivation of the original steering policy was based on satisfaction of position and velocity end conditions and minimization of the integral of the square of the lateral acceleration commands. It was felt that the integral square policy gave a good compromise between computational simplicity and reduced angles of attack from steering. The selected steering law can best be visualized by observation of the 2 dimensional geometry in Figure 4.12.1-14.

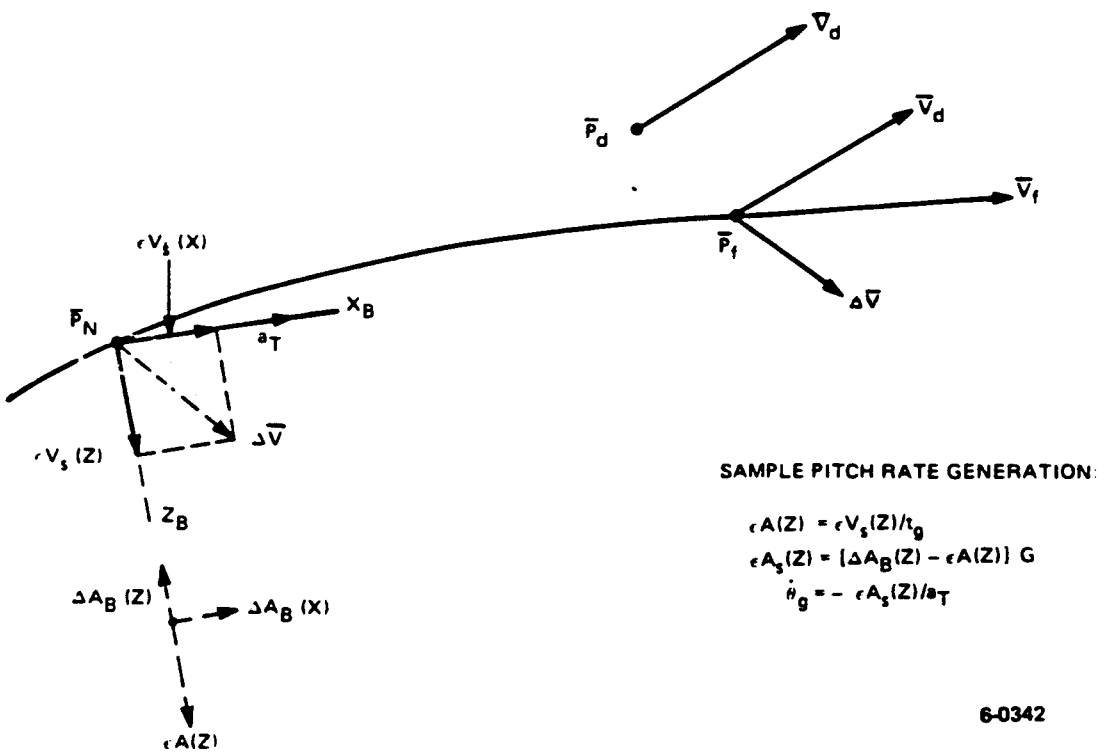


Figure 4.12.1-14. Steering Policy and Time-to-Go Geometry

The vehicle is shown at the current navigated position, $\bar{P}_N$. The predicted final position and velocity, $\bar{P}_f$ and $\bar{V}_f$, established by the powered flight predictor are indicated, as are the desired (retargeted) position and velocity determined by the error policy. $\bar{V}_d$ has been translated to the predicted position to more clearly show the vector difference $\Delta\bar{V} = \bar{V}_f - V_d$ which, in turn, was translated to the current position. For the purpose of this 2 dimensional presentation, the body axis x-z plane is shown in the orbit plane, as are the velocity vectors. It must be noted that although all those parameters will usually be outside the orbit plane, this discussion is still applicable.

Transformation of $\Delta\bar{V}$, which is in the inertial frame, to body coordinates is accomplished by use of the inverse TC matrix maintained by the navigation function. This transformation is carried out in the error policy equations. Components of $\Delta\bar{V}$ on the body y and z axes, $\Delta\bar{V}_s(i)$, divided by the time remaining until stage burnout represent the increments of acceleration changes

$$\varepsilon A(i) = \varepsilon V_s(i)/t_g, \; i = y,z$$

required along the body lateral axes to null the lateral velocity errors by burnout time. Transformation of the current $\Delta\bar{A}$ acceleration error, defined by the predictor equations, to body axes yields the components of acceleration deviation from nominal, $\Delta\bar{A}_B$, along the body axes. Combination of these acceleration data gives a measure of the net acceleration corrections to be applied along the lateral axes to reduce the velocity errors to zero by stage termination. These corrections are

$$\varepsilon A_s(i) = \Delta A_B(i) - \varepsilon A(i)$$

Since the direction of the total thrust acceleration vector must be changed to affect the above corrections, the angle by which this vector must be rotated is given by

$$\theta(i) = \tan^{-1} [\varepsilon A_s(i)/a_T]$$

where a_T is the thrust acceleration magnitude. Use of the small angle approximation $\theta \simeq \tan\theta$ and incorporation of a steering gain, G, required for guidance loop stability, results in

$$\dot{\theta}_G(i) = G\,[\varepsilon A_s(i)/a_T]$$

as the guidance lateral steering commands which represent the increments of angular change required per guidance cycle.

4.12.1.4.5.2 Time-To-Go Change. Aside from the guidance steering commands, the other variable which offers control for placing the vehicle on the desired orbit is engine shutdown time. This capability is available during the hydrazine velocity correction burn but not during the solid motor AKM burn. During AKM burn, time to go to desired burnout will be computed and used in the generation of guidance steering commands as indicated in the εA computation in the steering policy discussion. However, since engine shutdown cannot actually be commanded, there will be a slight error in the burnout velocity which will have to be corrected during the hydrazine burn.

The value of time to go, t_g, is computed during each guided mode as the difference between the targeted stage end time and the guidance time base, t_{cf}. However, t_{cf} is based on true time and is updated each guidance cycle by the time to go change, Δt_g, as

$$t_{cf} = t - \Delta t_g \tag{25}$$

It is Δt_g which is of interest here. Derivation of this parameter follows.

As indicated in the steering policy discussion, $\varepsilon\bar{V}_s$ is the predicted velocity error in body coordinates. It is desired to null the component of this velocity error which acts along the body thrust axis (roll axis) by changing the predicted t_g to the end of the stage. Expanding the thrust axis component, $\varepsilon V_s(x)$, of the velocity error (shown in Figure 4.12.1-14) with respect to changes in t_g and equating the resulting error to zero yields

$$\varepsilon V_s(x) + \frac{\delta \varepsilon V_s(x)}{\delta t_g} \Delta t_g = 0 \tag{26}$$

Predicted velocity is a function of thrust and gravitational accelerations. Approximately the same magnitude of gravitational acceleration, and no thrust acceleration, enters into the desired velocity; but the gravity acts only for a miniscule time difference, $\Delta(\Delta t_g)$, by virtue of desired velocity being computed using Δt_{orb} (which contains most of the Δt_g effect). Therefore, only the thrust acceleration force acts along the vehicle longitudinal axis at injection and Equation 26 can be written as

$$\varepsilon V_s(x) + a_T \Delta t_g = 0$$

from which

$$\Delta t_g = \varepsilon V_s(x)/a_T \tag{27}$$

Equation 27 does not give a complete solution for the change in time to go. The $\varepsilon V_s(x)$ used in this equation is based on the time to go change already made, thus that contribution must be included to give the total change in time to go; therefore, each new computation is combined as an incremental change to the previous value. An additional consideration in the time to go computation is the acceleration error, $\Delta A_B(x)$, which acts along the thrust axis along with the velocity error. This acceleration error integrates into a velocity error over the next guidance computing interval. To avoid this effect, its contribution to velocity error over the upcoming compute cycle is taken into account in the Δt_g equation. The complete time to go change then becomes

$$\Delta t_{g_n} = \Delta t_{g_{n-1}} + [\varepsilon V_s(x) - \Delta A_B(x)\, \tau_c]/a_T \tag{28}$$

The actual time to go can then be computed as

$$t_g = T_f - t + \Delta t_g = T_f - t_{cf}$$

where the relationship from Equation 25 is evident.

4.12.1.4.5.3 Time To Cutoff. When time to go to engine shutdown drops below a preset value, closed loop guidance is terminated. When this occurs, countdown logic is established which enables engine shutdown to be commanded within 20 milliseconds of the desired value. Since only the hydrazine thrusters can be shutdown on command, the 20 millisecond resolution is acceptable because the thrust acceleration of about 3 feet/second/second will cause a velocity error of only 0.06 feet/second. This velocity error will result in an apogee minus perigee error of only slightly over 100 feet.

Although time to cutoff, Δt_{co}, is truly applicable only to the hydrazine burn phase, values are computed for the coast adjust phase and for the AKM powered phase to simplify the closeout logic mechanization. The desired Δt_{co} is

$$\Delta t_{co} = T_f - t + \Delta t_g + \Delta A_B(x)\ t_g/a_T - t_{To}$$

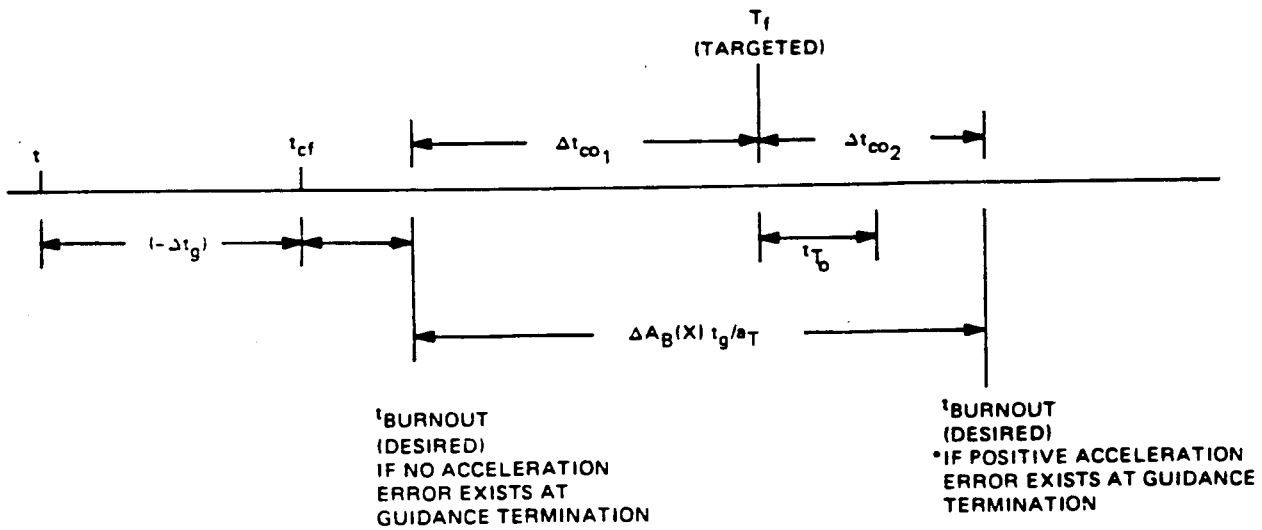
For coast adjust, this is actually the time to AKM ignition.

Figure 4.12.1-15 diagrams the above time relationships. Two possible situations are shown for a given clock time point, t, at guidance termination with a Δt_g such that t_{cf} is a time later than clock time. If no thrust axis acceleration error were prevalent, Δt_{co} would be such that burnout would be commanded at a time prior to the targeted burnout time. On the other hand, if an acceleration error existed such that an additional burn time given by $\Delta A_B(x)\ t_g/a_T$ were required to make up the needed acceleration, then burnout would be commanded at a time later than the targeted time. As indicated on the figure, the current convention for acceleration error is such that a positive error exists when the predicted acceleration is greater than the measured acceleration (the value deduced from summation of the velocity increments measured by the thrust axis accelerometer over the most recent 0.5 second guidance interval). In the derivation of Equation 28, it was indicated that the $\Delta A_B(x)\ \tau_c/a_T$ was a prediction over the succeeding guidance cycle of the thrust axis acceleration error effect on time to go that would be computed on the next cycle. The same line of reasoning suggests the use of $\Delta A_B(x)\ t_g/a_T$ to compute this effect over the time remaining from guidance cutoff to burnout.

Because of the manner in which the coast adjust guidance mode is processed, it was necessary to compute a value of Δt_{co} for that mode also. Rather than to effect cutoff, however, Δt_{co} is used in the coast adjust mode to trigger AKM ignition at the modified ignition time established during the processing of this mode. This is accomplished by use of Mode Control logic to be discussed later. At any rate, use of Δt_{co} for this purpose necessitated introduction of another time term, t_{adj}, to reduce the coding requirements in the software mechanization process. Thus, the last two terms in the above Δt_{co} equation are redefined as

$$t_{adj} = t_{To} - \Delta A_B(x)\ t_g/a_T$$

This allows t_{adj} to be set to a dummy value, or zero, during closeout of the coast adjust mode and allows use of the same equation as is used for the powered flight modes to compute Δt_{co}.



•POSITIVE ACCELERATION ERROR INDICATES PREDICTED ACCELERATION IS GREATER THAN MEASURED VALUE

6-0343

Figure 4.12.1-15. Time-To-Cutoff Diagram

4.12.1.4.6 Time Adjustments For Sequencing

Changes in time to go were discussed in the previous subsections. Other adjustments or discrete changes made to the various time parameters used by the guidance software are discussed in this section.

4.12.1.4.6.1 Time Adjustment During Active Guidance. The primary guidance time base is called guidance curve fit time, t_{cf}. This parameter had been defined previously as

$$t_{cf} = t - \Delta t_g \tag{29}$$

where t is the clock time maintained by the guidance computer. As the name indicates, t_{cf} is related to the acceleration curve fits that are input as the reference for nominal performance of powered stages. Since it is desirable to gear occurrence of trajectory shaping functions to the thrust terminations at burnout of each powered stage, discrete functions are sequenced relative to the acceleration curve fit times in the targeting process. It is, therefore, convenient to sequence in-flight events on the basis of t_{cf}, and it then becomes necessary to alter both t and t_{cf} in accordance with the desired thrust discontinuities. For this reason, t is reset to the nominal burnout time when AKM burnout is sensed, t_{cf} is set slightly larger than t by an ε time increment, and Δt_g reset to zero at that point, resulting in t_{cf} being almost equal to t until hydrazine ignition is commanded. The same thing is done when Titan II SECO is sensed so that all sequences occurring prior to the start of the

coast adjust guidance mode will be referenced to nominal SECO. Thus, hydrazine ignition occurs at approximately the nominal t_{cf} time (within a guidance compute interval minus ε) but not at the nominal clock time, since this latter time has been altered. As soon as guidance is initialized and steering is processed, non-zero Δtg values will be computed and then t and t_{cf} will again differ by Δt_g in accordance with Equation 29.

At burnout of a normal hydrazine velocity correction burn and at AKM ignition, which are commanded when Δt_{co} is counted down to zero in the Mode Control logic, t_{cf} will be set to the nominal burnout time to insure that the events will be initiated by the discrete sequencer which operates on the basis of t_{cf}. A time point at which it is necessary to set t equal to the nominal hydrazine burnout time is upon the anomalous occurrence of hydrazine depletion at an earlier time than that required by guidance via the Δt_g computation. In this event, the desired injection conditions would not be achieved, but post-injection guidance sequences would be initiated after the nominal time passage from the actual sensed burnout (anomalous depletion).

It should be noted that Δt_g is not set to zero at the end of the coast adjust guidance phase. This allows consideration of Δt_g when commanding the ensuing AKM ignition, since t_{cf} will continue to differ from t by the Δt_g adjustment.

Because of the ongoing modification to t_{cf}, it is conceivable that sequences which might be scheduled after the end of a stage could be sequenced before burnout actually occurred. To prevent this possibility, the curve fit time is limited to the nominal final time for the current stage before entry to the sequencer software is allowed. This does not affect the use of t_{cf} in the guidance computations because the sequencer is processed at the end of the guidance computation cycle and t_{cf} is recomputed at the start of the next guidance cycle. A difficulty which could occur if events were scheduled too closely before nominal burnout of the hydrazine burn is that if the t_{adj} discussed in the previous sections were such that cutoff would be commanded earlier than the scheduled event, that event would not be sequenced at the expected time. The same problem could occur if AKM burnout were to occur anonymously early and events were scheduled close to the end of the nominal burn time. For this reason, scheduling of events near burnouts should be carefully analyzed.

4.12.1.4.6.2 <u>Time Adjustments For Titan II/ATN-KLM Synchronization</u> (TBD)

4.12.1.4.7 Coast Adjust Guidance

The purpose of this mode is to modify the ignition time of the AKM stage and to change the vehicle attitude accordingly in order to compensate for non-nominal conditions during the Titan II burn phase. To accomplish this it is necessary to predict the position and velocity at AKM burnout so that they may be forced to a set of end conditions which will place the vehicle on the nominal AKM burnout orbit. This approach, in turn, makes it necessary to predict the position and velocity states at the predicted AKM ignition point and to add the predicted position-to-be-gained and velocity-to-be-gained during AKM burn.

A brief description of the coast adjust guidance mode was given in Section 4.12.1.4.1 where it was stated that this mode employs most of the software developed for the powered flight modes. Some additional software was developed to properly interface this mode with the powered flight equations.

Adaptation for use of the powered flight prediction is made by setting

$$t_o = T_f - t_b$$

where t_o is the entry time to the predictor, T_f is the AKM nominal burnout time, and t_b is the nominal AKM burn duration. Hence, t_o equals the nominal AKM ignition time and is kept constant throughout this mode. This forces the predictor t_o generate the position and velocity to be gained during AKM burn and the predicted ignition acceleration each time it is entered.

A pictorial description of the basic coast adjust concept is presented in Figure 4.12.1-16. The similarity to the figure shown in discussion of the error policy makes it evident that the same basic error criteria are used. $\bar{P}_o$ and $\bar{V}_o$ represent the predicted position and velocity vectors at the updated AKM ignition point. This prediction is based on the current position and velocity vectors determined by the navigation function, and uses the average gravity vector between the current position and the <u>nominal</u> AKM ignition position. The gravitational acceleration at this latter position can, therefore, be an input targeting constant. Its use is justified on the premise that changes in the ignition point position will be sufficiently small to render negligible gravitational variations. It is apparent from the figure that this gravity vector is

$$\bar{g}_{ao} = (\bar{g}_o + \bar{g}_n)/2$$

The time to go to ignition is determined as

$$t_{ig} = t_g - t_b$$

where t_g in this case is the time to go to AKM burnout. Using this time, the predictions of velocity and position at AKM ignition are given by

$$\bar{V}_o = \bar{V}_N + \int_o^{t_{ig}} \bar{g}_{ao}\, dt$$

and

$$\bar{P}_o = \bar{P}_N + \int_o^{t_{ig}} \int_o^{\tau} \bar{g}_{ao}\, dt d\tau$$

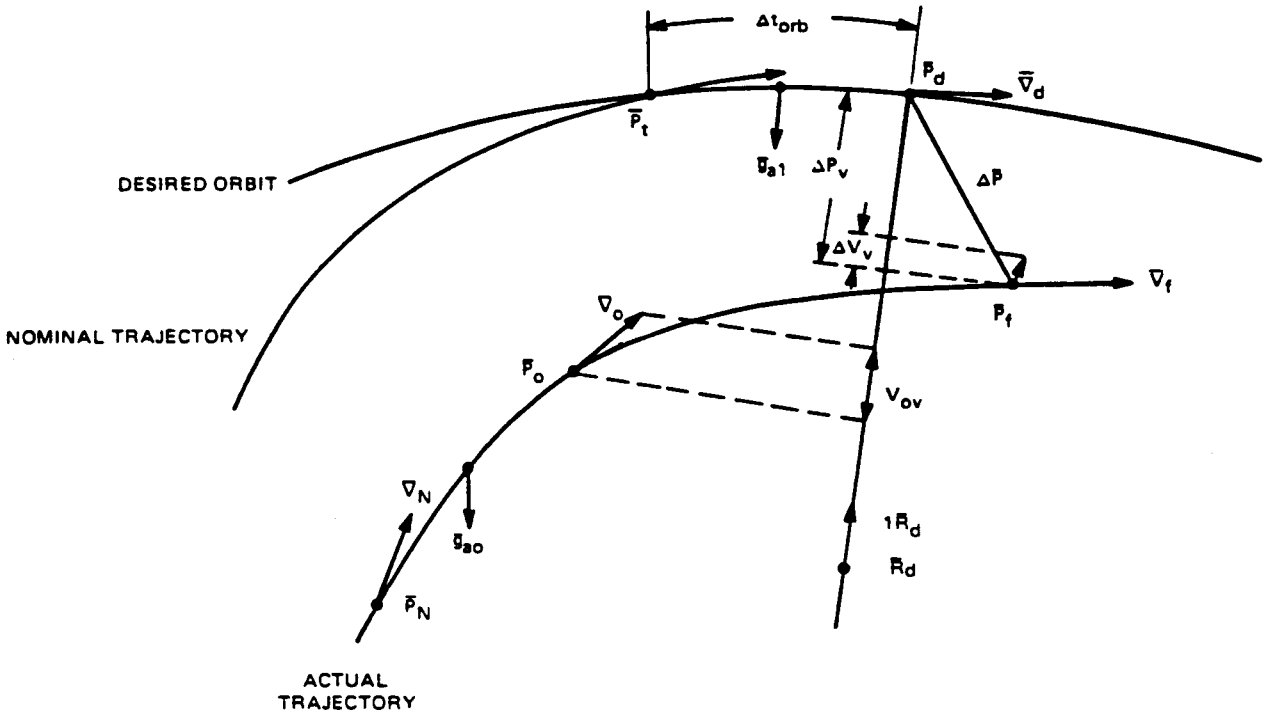


Figure 4.12.1-16. Coast Adjust Policy Geometry

Since $\bar{g}_o$ is the value computed for gravitational acceleration at AKM ignition, the incremental change in velocity over a guidance interval at ignition is given by consideration of the 0.5 second compute interval as

$$\Delta\bar{V}_o = \bar{g}_o/2$$

which is combined with the predicted ignition acceleration (from the powered flight predictor) to determine the total acceleration to be gained during AKM burn. At this point, the interface computations required to use the powered flight software are basically complete. Some special computations required to supplement the error policy will be discussed shortly. Addition of the $\bar{P}_o$ and $\bar{V}_o$ given above to the predicted increments to be gained during the AKM burn will yield the burnout position and velocity, $\bar{P}_f$ and $\bar{V}_f$, at AKM burnout.

Significant factors in the error policy for the coast adjust function are the vertical component, V_{ov}, of ignition velocity and the vertical components of burnout position and velocity errors, ΔP_v and ΔV_v, respectively, all of which are depicted in Figure 4.12.1-16. Each of these components is obtained as the dot product of the appropriate vector with a unit vector which defines the direction of the radius vector at AKM burnout. They are used as the basis for adjustment of the AKM stage ignition time. Only the burnout radius is used,

for simplicity, since the angular separation between the AKM ignition and burnout radii is only slightly over 2 degrees; thus, the projection of the ignition velocity on the burnout radius vector yields an insignificant error. A suitable value for the burnout radius vector is obtained by use of the targeted burnout position and this value may be used as a constant throughout the coast adjust computations since the direction is of prime interest and said direction changes insignificantly. The series of equations required to arrive at the ignition time adjustment, εt_g, follow. First, the vertical component of velocity at ignition may be found as

$$V_{ov} = \bar{V}_o \cdot 1\bar{R}_d \tag{30}$$

The burnout velocity and position projections on the burnout unit radius vector are

$$\Delta V_v = \Delta\bar{V} \cdot 1\bar{R}_d \tag{31}$$

and

$$\Delta P_v = \Delta\bar{P} \cdot 1\bar{R}_d \tag{32}$$

The vertical position error is driven to zero by adjusting the ignition time and accounting for the effect of AKM steering required to drive the vertical velocity error to zero. The steering effect is based on the steering law holding a constant vertical acceleration error during burn. This acceleration error is given by $\Delta V_v/t_b$, hence the position effect equals $\Delta a t_b^2/2$, which reduces to $\Delta V_v t_b/2$. Therefore, the change in ignition time required to account for the difference between the predicted position error and the position error introduced during AKM burn to null the velocity error is

$$\varepsilon t_g = (\Delta P_v - t_b\, \Delta V_v/2)/V_{ov} \tag{33}$$

and this increment is used to modify the change in time to go such that

$$\Delta t_g = \Delta t_g - \varepsilon t_g \tag{34}$$

The adjustment to the final position and velocity which will be made by the εt_g change in application of the ignition velocity will be given by

$$\Delta\bar{P}_f = -\varepsilon t_g(\bar{V}_o + \bar{g}_o t_b) \tag{35}$$

$$\Delta\bar{V}_f = -\varepsilon t_g \bar{g}_o \tag{36}$$

where $\bar{g}_o t_b$ yields an approximation to the velocity change caused by gravitational acceleration during the stage burn time, based on the assumption that the change in gravity during that time period is small enough that the initial value is representative of the average value. Use of the negative signs stems from the fact that a positive value of εt_g reduces the time to go to burnout.

Having established the necessary adjustment in the AKM ignition time and the effect on final position and velocity by use of Equations 30 through 36, the normal error policy software can then be processed to determine the steering requirements.

Functional diagrams of the supplementary coast adjust computations other than the normal predictor, error policy, and steering functions are shown in Figures 4.12.1-17 and 4.12.1-18. These figures are furnished to aid in understanding relationships between parameters computed in various areas of the software package.

4.12.1.4.8 Position Pointing Guidance

Position pointing guidance modes are used at several points along the trajectory. This guidance mode is basically an attitude pointing mode which uses position and velocity vector data to generate the steering commands required to achieve the desired attitude. The term position, as opposed to attitude, in naming the mode was purely to differentiate from the attitude pointing modes used in ATN-KLM and DIGS guidance systems, which employ acceleration vector data for steering command generation.

Current usage of the position pointing modes was delineated in Section 4.12.1.4.1. The primary purpose of the mode is to accomplish the attitude pointing required after orbit insertion and, as such, the software development was geared to the vehicle orientation with the thrust axis normal to the orbit plane and the vehicle keel (positive body z axis) pointing towards earth center along the radius vector.

The first application of this mode is shortly after separation from the Titan II, for the purpose of trimming the roll orientation only. To accomplish this, the same software developed for the post-injection modes can be used with the pitch and yaw channel gains set to zero. An additional use of this mode which will require a separate discussion in this section is its application for orienting the vehicle in the desired post-separation attitude in the event of accelerometer or navigation failures. The same software is employed for this situation but the targeting required is slightly different.

4.12.1.4.8.1 <u>Thrust Axis Normal to Orbit Plane</u>. Figure 4.12.1-19 shows the geometry for which the position pointing equations were developed. The inertial velocity and radius vectors shown define the orbit plane, whereas the direction normal to the orbit plane is defined by the cross product vector $\bar{V} \times \bar{R}$. The vehicle is shown in a skewed orientation with the nose roughly normal to the orbit plane and the body z axis roughly aligned with the radius vector. Such an orientation might result after completion of the 90 degree open loop yaw maneuver and the pre-defined roll maneuver which are performed shortly after orbit injection.

It is apparent that the inertial position and velocity vectors can be transformed into the body coordinates shown by use of the inverse of the TC matrix, which relates the 2 coordinate frames. The desired orientation requires that the negative body y axis be aligned with $\bar{V}$, the positive body x axis be aligned with $\bar{V} \times \bar{R}$, and the positive body z axis be aligned with $\bar{R}$. If such an orientation were achieved, the components of $\bar{R}$ on the body x and y axes would be zero, as would the component of $\bar{V}$ on the body x axis. Therefore, it can be

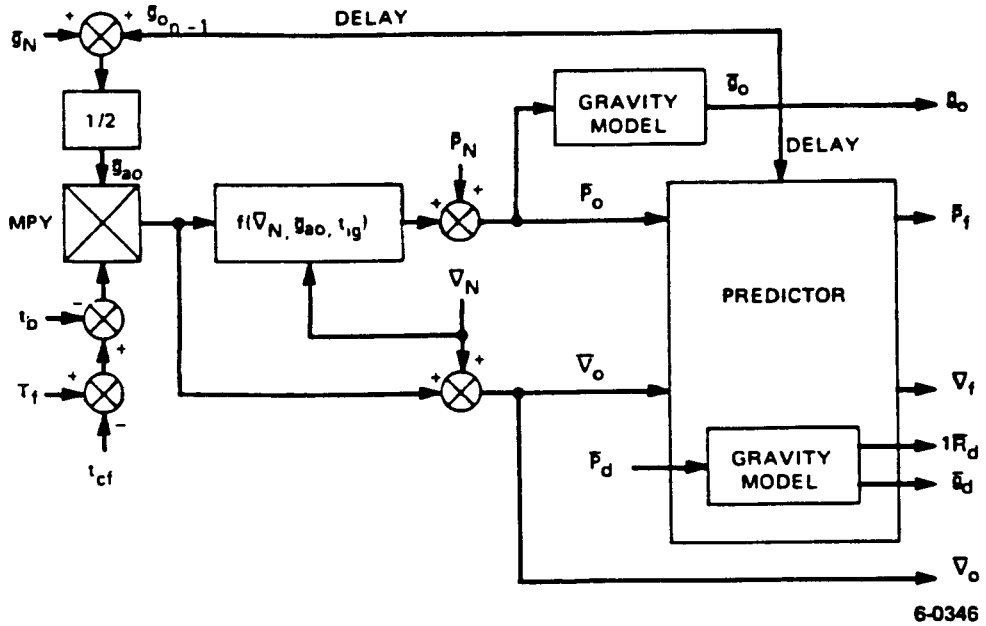


Figure 4.12.1-17. Coast Adjust Guidance Functional Diagram, Part 1

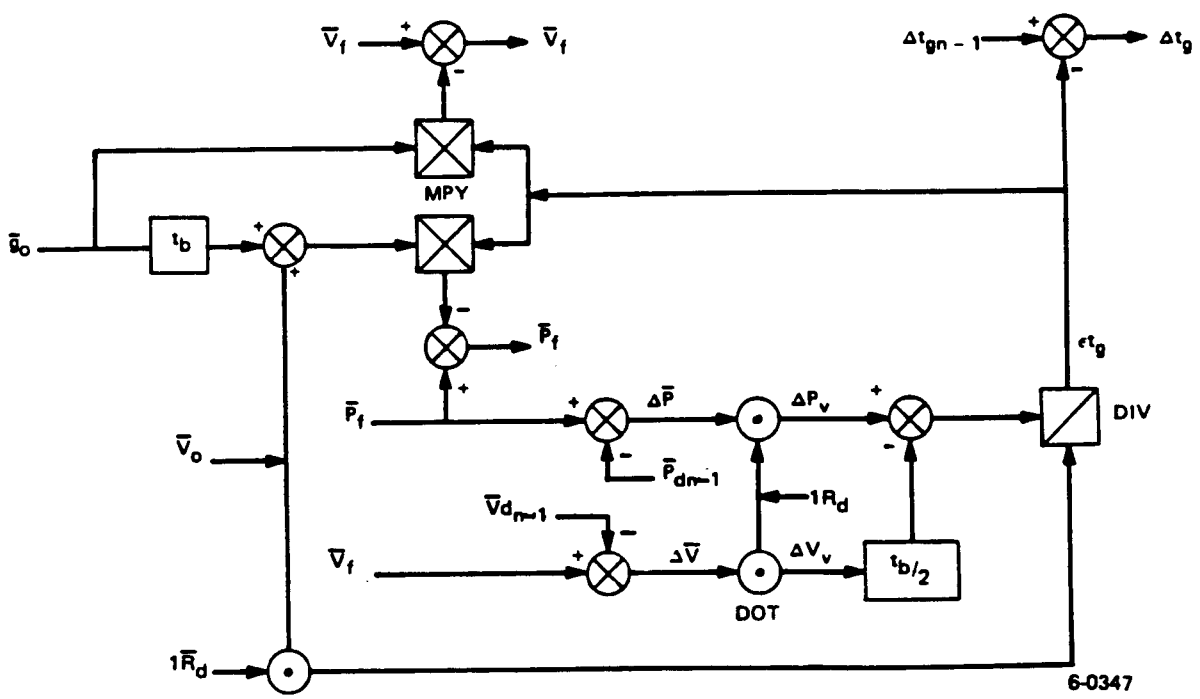


Figure 4.12.1-18. Coast Adjust Guidance Functional Diagram, Part 2

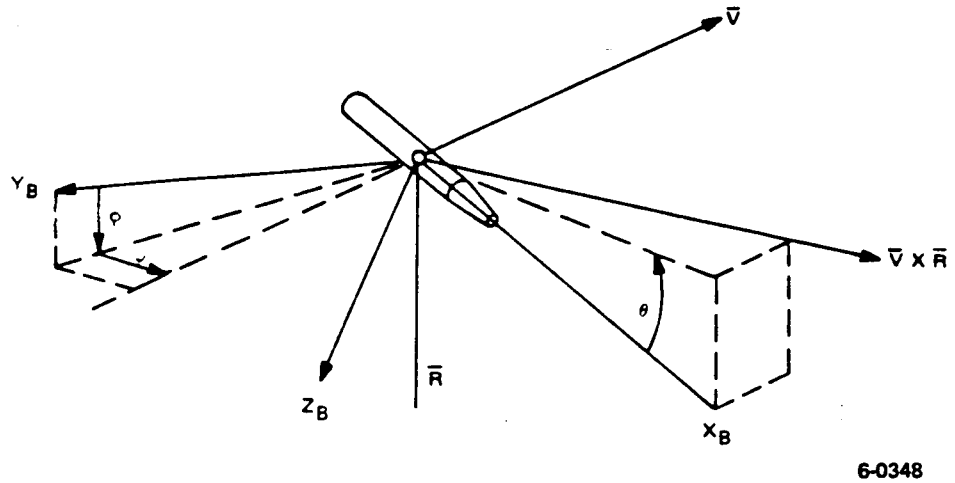


Figure 4.12.1-19. Position Pointing Geometry

seen that if non-zero components of those vectors exist on the specified body axes, the component magnitudes can be used to generate commands proportional to those magnitudes so as to null those values. In short, the desired end conditions are such that

$$R_{Bx} = R_{By} = V_{Bx} = 0$$

where the notation indicates the components of $\bar{R}$ and $\bar{V}$ on the x or y body axes. These components are obtained using

$$\bar{R}_B = [TC]^T \bar{R} \quad \text{and} \quad \bar{V}_B = [TC]^T \bar{V}$$

where the TC matrix transpose is used in place of the inverse due to its orthonormal properties. The equations needed to null non-zero components of the specified axes are

$$\dot{\phi}_g = G_\phi \cdot \frac{R_{yB}}{R_o}$$

$$\dot{\theta}_g = G_\theta \cdot \frac{R_{xB}}{R_o}$$

$$\dot{\psi}_g = G_\psi \cdot \frac{V_{xB}}{V_o}$$

where G_ϕ, G_θ, and G_ψ are proportionality constants construed as guidance gains. The above equations can be modified to include the effects of control system attitude errors resulting from the control system dead zone.

By adding feedback for these control system attitude errors, the guidance system will not cause the vehicle to cycle through the dead zone, thus using control fuel more efficiently. The resulting equations are

$$\dot{\phi}_g = G_\phi \left(\frac{R_{yB}}{R_o} + \Delta\theta(1)\right) \tag{37}$$

$$\dot{\theta}_g = G_\theta \left(\frac{R_{xB}}{R_o} - \Delta\theta(2)\right) \tag{38}$$

$$\dot{\psi}_g = G_\psi \left(\frac{R_{xB}}{R_o} + \Delta\theta(3)\right) \tag{39}$$

The gains are significant in that they affect system stability as well as system response. The upper limits of those gains are established on the basis of stability considerations and the lower limits are based on response considerations.

It was felt that a fast response was not necessary, therefore eliminating any stability problems. A time span of 30 to 50 seconds for completion of corrections was considered suitable. It was further anticipated that 10 degrees was a realistic initial angular error to be corrected, based on consideration of the geometry existing at shutdown of the hydrazine velocity correction phase. An initial commanded rate of 1 degree per second was also assumed reasonable; this results in a gain of 0.1.

Bearing in mind that the commands will be applied by the control system incrementally at a 50 per second rate, the gains required to satisfy the 1 degree per second rate criterion are

$$G_{\phi,\theta,\psi} = \frac{0.1\ \text{sec}^{-1}}{(50\ \frac{\text{cyc}}{\text{sec}})} = 2 \times 10^{-3}$$

In keeping with the classical body rate sign convention, a positive rate about the positive y_B axis is required to raise the nose of the vehicle from the orientation shown in Figure 4.12.1-19 to the desired plane defined by $\bar{V}$ and $\bar{V} \times \bar{R}$. Yet it should be apparent from the figure that the projection of the radius vector on the x_B axis will yield a negative-valued component. In order to achieve the proper sign on the pitch rate command it is therefore necessary to use a negative value for G_θ.

In summary, Equations 37 through 39 will generate the steering commands required to orient the vehicle with the nose normal to the orbit plane and the keel aligned with the radius vector.

4.12.1.4.8.2 Thrust Axis in Orbit Plane. One exception to the orientation shown in Figure 4.12.1-19 occurs during the first scheduled position pointing task, which is used only for roll orientation. In that instance, the body x axis will be approximately in the orbit plane with the nose forward and the

vehicle keel will be downward in the vicinity of the radius vector. In spite of the different orientation it can be seen that the radius vector projection on the body y axis will still control the roll channel; therefore, the desired roll commands can be achieved by using the system in the normal manner. However, the G_θ and G_ψ gains (more importantly G_ψ) must be set to zero so that an erroneous 90 degree yaw command and some unnecessary pitch command will not be generated.

4.12.1.4.9 Mode Control (TBD)

4.12.1.4.10 Limited Variables

Certain key guidance parameters in the software were limited to avoid guidance system failures which could result from occurrence of one-pass computer errors or from anomalous vehicle performance. The parameters selected were the change in time to go (Δt_g), guidance steering commands (ϕ_g, θ_g, ψ_g), and lateral body components of incremental velocity change ($\varepsilon \bar{V}B$ (y, z)).

The Δt_g limit is established on the basis of the maximum time to go adjustment expected for a conservative estimate of slightly worse than 3 sigma vehicle performance. Limiting the value will protect against computer errors in the guidance computational process leading up to computation of velocity errors in body coordinates. Since the parameter is computed as a function of the inverse of thrust acceleration, it will also avoid computer overflow in the event of a momentary failure which would cause an erroneously low indication of thrust acceleration during powered flight guidance phases. A limit of 35 seconds is currently being used.

Limiting the guidance steering rates protects against the possibility of gyro saturation which could result not only from a momentary computer failure, but also from large velocity or acceleration errors which might exist at guidance initiation during a highly perturbed flight. A 1.5 degree per second limit for each control channel is currently being used. In the event of a navigation failure, this limit becomes 3.0 degrees per second.

Components of incremental velocity in body coordinates determined from the lateral accelerometer measurements are limited to zero values if their values exceed maximum limit values of 2.41 feet per second per cycle. System operation then continues using the zero values for the lateral components. This limiting process would be invoked whether the erroneous velocity increments resulted from computer failure, anomalous vehicle maneuvering, or lateral accelerometer failure.

Other parameters for which limits are set within the software, such as time and attitude errors, are not limited as a result of failures but purely to aid the computational processes in which they are employed.

4.12.1.5 Curve Fit Accuracy

The guidance equations determine errors in position and velocity at the end of a stage by comparing nominal burnout values with predicted values. Current errors in acceleration are established by comparison of actual values obtained from navigation data and values predicted backwards from the end of the current stage to the present time. An extensive derivation of the prediction process was presented in Section 4.12.1.4.2. The predictor utilizes second-order curve fits of inertial acceleration vectors to arrive at the desired data. Conditions imposed on the curve fit are that acceleration at the start of a segment be equal to that at the end of the previous adjacent segment, that the integral of acceleration over each segment be equivalent to the velocity to be gained over the segment, and that the double integral yield position to be gained over the segment. The choice of the number of curve fit segments to be used for

each powered stage must be determined on the basis of curve fit accuracy and the computational load imposed on the computer. Based on experience with Block 5D and TIROS-N, two segments were deemed suitable for the ATN-KLM AKM stage and one segment was used for the hydrazine powered burn phase.

Performance loss can result from errors in the curve fits. These errors are caused by the manner in which a second order curve fit traverses the actual curve being fit, and are usually oscillatory in nature. One way in which the performance loss occurs is that the oscillatory curve fit errors will cause the guidance steering commands for the lateral axes to oscillate about the truly necessary command, thus causing unnecessary steering. A second contribution to performance loss occurs in stages for which engine shutdown is commanded by guidance. This results from the fact that curve fit errors along the vehicle thrust axes are transformed to errors in time to go to engine shutdown.

In view of the possible performance loss, it is desirable to keep curve fit errors as small as possible. Figure 4.12.1-20 shows the curve fit velocity errors for the AKM stage. The performance loss caused by the lateral axis errors was such that it resulted in an additional hydrazine consumption of 0.01 pound for the velocity correction burn phase, because of a slight adjustment in burn time. Negligible additional hydrazine consumption is anticipated from use of the hydrazine thrusters for attitude control during AKM burn because of the low amplitude and low frequency of the velocity errors. On this basis, the accuracy of the curve fits was considered highly acceptable.

4.12.2 CONTROL SYSTEM ANALYSIS (TBD)

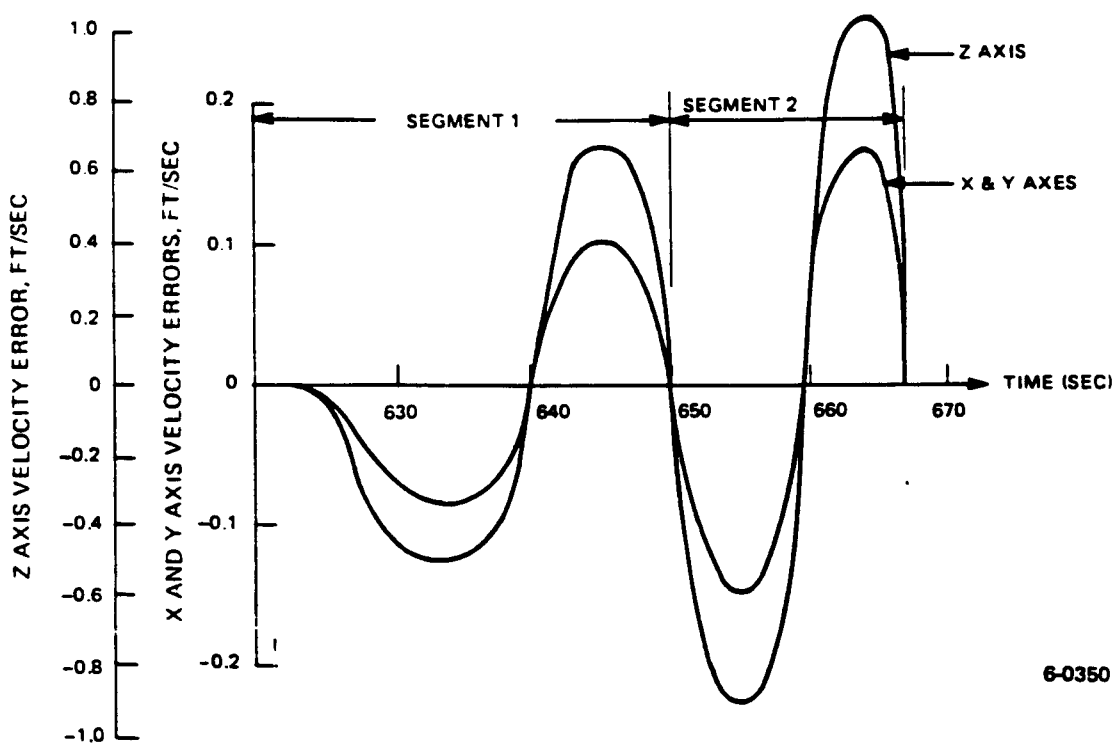


Figure 4.12.1-20. Errors in Inertial Velocity to Go from Curve Fits, AKM Stage (TIROS-N SAR)

4.12.3 ASCENT GUIDANCE SOFTWARE MECHANIZATION

The Ascent Guidance Software (AGS) provides the capability to: 1, support pre-launch checkout of the ascent phase software/hardware systems; 2, initialize the system, including alignment and key IMU parameter updates; 3, sense lift-off and navigate position, velocity, and attitude throughout the ascent phase; 4, provide for transfer from Titan II to ATN-KLM control; (5) provide open loop sequencing for a nominal system from Titan II separation to on-orbit handover; 6, provide closed loop guidance for apogee kick motor (AKM), hydrazine velocity trim, and payload orientation phases of the mission; and 7, mechanize all these within the capability of the SCP-234 computer.

4.12.3.1 System Definition

The AGS utilizes the spacecraft computer, strapdown Inertial Measurement Unit (IMU), and Controls Interface Unit (CIU) to provide intelligence to the ascent phase trajectory. The total launch vehicle configuration shown in Figure 4.12.3-1 consists of an Titan II booster and sustainer vehicle, a solid propellant apogee kick motor stage (AKM), and hydrazine and nitrogen thrusters for velocity trim and attitude control after separation from the Titan II vehicle. The trajectory sequence utilizes the Titan II guidance and control system for vehicle control through the second stage shutdown command. ATN-KLM navigates independently of Titan II during this phase, and uses acceleration-sensed Titan II sustainer engine cutoff (SECO) and ACS inhibit signals to synchronize its open loop sequencing with the Titan II separation command. The remainder of the ascent phase trajectory sequences are actively guided and controlled by the ATN AGS.

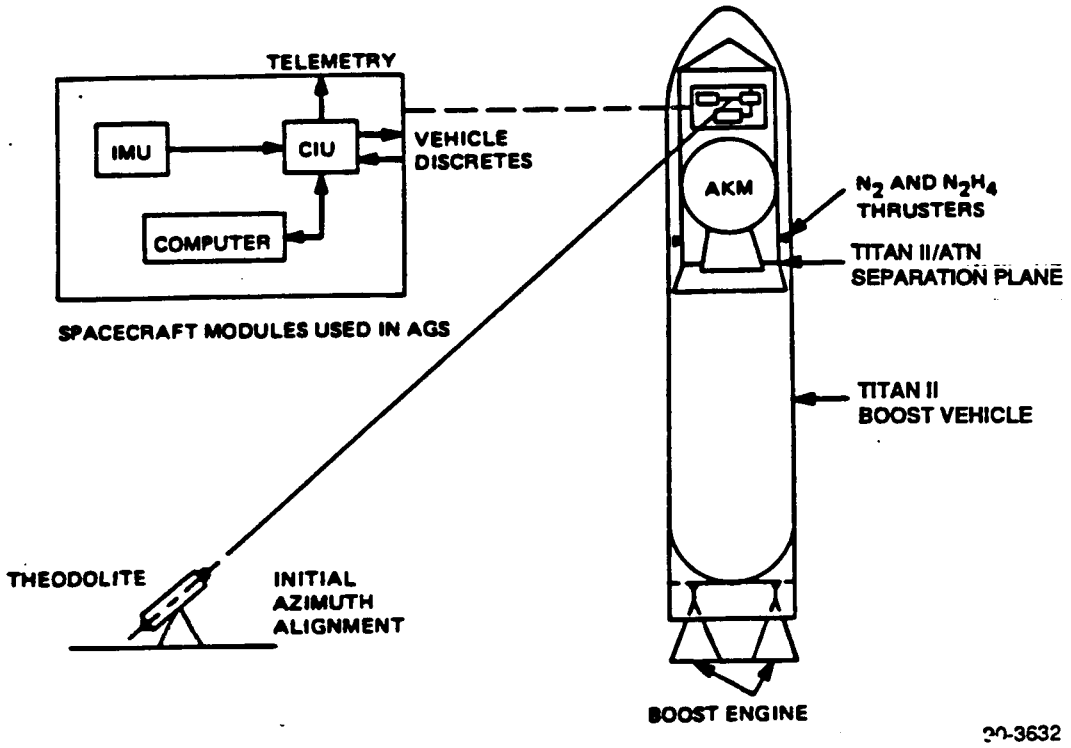


Figure 4.12.3-1. Pre-Launch Vehicle Configuration

4.12.3.1.1 Pre-Launch Description

During pre-launch activity, the software is required to support checkout in Building 1610 and on the launch pad after integration with the Titan II boost vehicle. In Building 1610, the spacecraft is in a horizontal position with any 1 of the principal IMU axes in the vertical direction, as shown in Figure 4.12.2-2. In these positions, the software is capable of exercising all of its test capabilities including alignment, navigation, and flight simulation. On the launch pad, the software is capable of alignment, azimuth update, navigation, control mode sequence testing, and flight simulation. Alignment is based on the IMU level orientation defined by the lateral accelerometers and vehicle orientation data. Azimuth orientation is updated based on theodolite sighting of a porro prism mounted on the spacecraft. A schematic diagram of the alignment processing is shown in Figure 4.12.3-3.

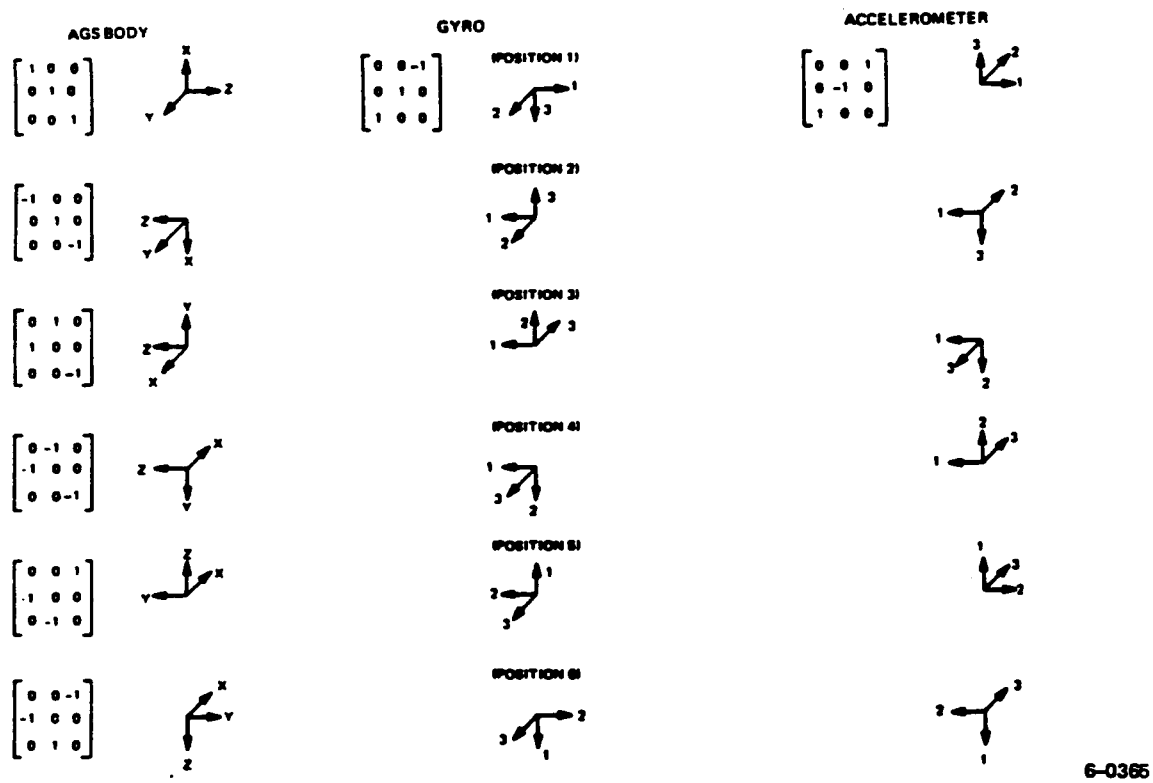


Figure 4.12.3-2. Vehicle Checkout Orientation Capability

4.12.3.1.2 Mechanization Description

The software is mechanized for the SCP-234 computer in machine language load format code. The software interfaces with on-orbit software described fully in Section 4.10; the overall software is mechanized within a 16 level priority interrupt structure. AGS is mechanized to use interrupt levels 11 (telemetry), 9 (IMU data), and 6 (2/second computations). Stub programs are also provided on levels 3 and 1 for use only during testing at MDAC.

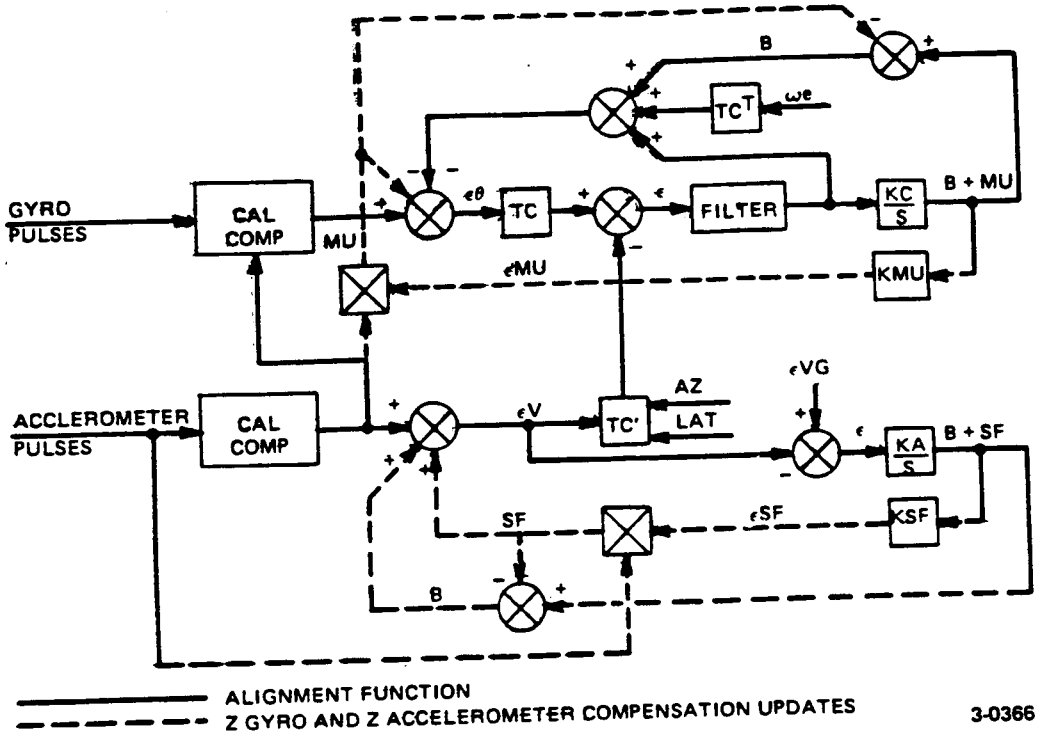


Figure 4.12.3-3. Alignment Loop Block Diagram

4.12.3.2 Level 11 Interrupt Requirements (Telemetry)

This level is the highest normally used level for AGS processing; the executive control of this interrupt level is shown in Figure 4.12.3-4. Level 11 is used for telemetry data output and handover from AGS to on-orbit control. The interrupt is generated every 10 milliseconds for telemetry output purposes, and is set via software control to exercise handover.

4.12.3.3 Level 9 Interrupt Requirements (IMU Data)

This interrupt is generated every 10 milliseconds when IMU data are available for input from the CIU; the executive logic flow is shown in Figure 4.12.3-5. Since data are input from only 4 registers, 2 input passes are made, hence, 2 interrupts occur for a complete cycle; this interrupt pair is therefore recognized as a single interrupt each 20 millisecond interval. This interrupt is the basis of time control for all the AGS real time equations. The level 9 interrupt control routine provides the logic for controlling entry to the Telemetry Store and/or the Orthonormalize routines as well as calling various routines processed at a 50/second rate.

The Telemetry Store routine is called whenever the TM flag has been set by the telemetry interrupt routine denoting a telemetry buffer is empty.

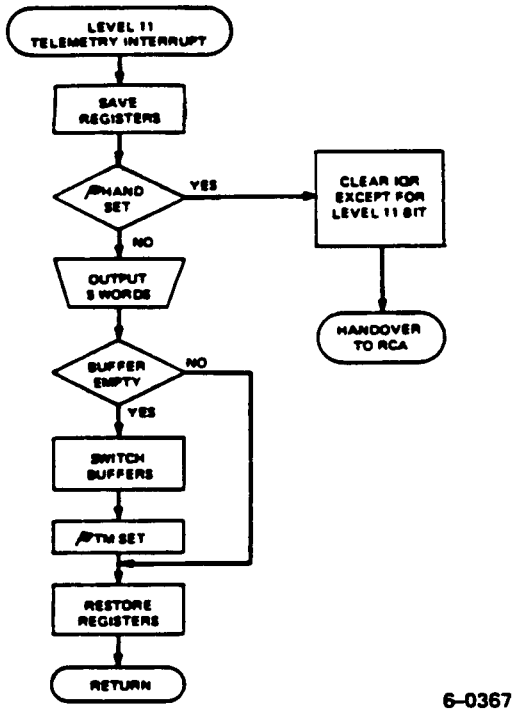


Figure 4.12.3-4. Telemetry Interrupt (Level 11)

The Orthonormalize routine must be processed periodically, but not necessarily on an absolute fixed interval. Therefore, the logic controlling entry to this routine prevents entry into Orthonormalize on the same computational interval in which either the Telemetry Store routine is processed or in which the integer counter negative condition exists. This entry constraint is imposed to avoid timing problems which could result from a high computation load during a given cycle (particularly during pre-launch alignment).

4.12.3.3.1 Gyro Data Processing

This routine inputs the IMU gyro data, compensates it with pre-defined IMU-specific calibration data and with alignment determined updates for bias and roll spin mass unbalance, and transforms it from gyro coordinates to body coordinates as defined by nominal vehicle position on the launch pad. The logic and equations flow for this routine are mechanized as shown in Figure 4.12.3-6.

This transformation accommodates any of 6 IMU positions as defined in Figure 4.12.3-2. The logic for setting up the elements of this transformation matrix are defined as a function of accelerometer sensing in the Initialization routine. Once the data are defined in body coordinates, they are processed through the control equations and the strapdown attitude matrix update equations. During pre-launch operations, the roll pointer, KROLL, is zero and allows summation of the gyro and accelerometer pulse outputs during pre-launch operations for telemetry output. Monitoring of the lift-off discrete in telemetry is made possible in this flow path by storing the vehicle status word in the pitch/yaw control pointer during pre-launch and Titan II boost.

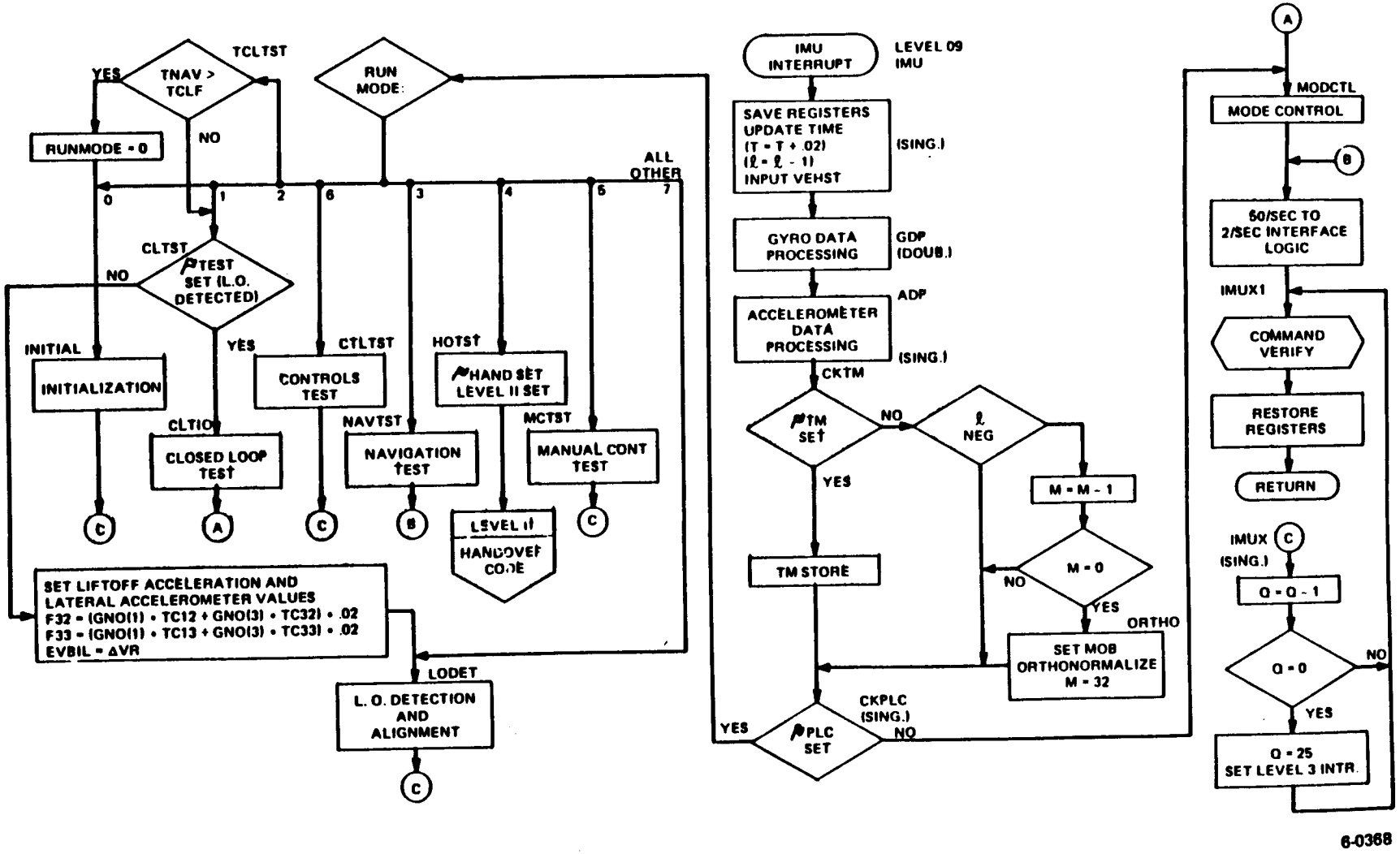


Figure 4.12.3-5. Level 9 Interrupt Flow Diagram

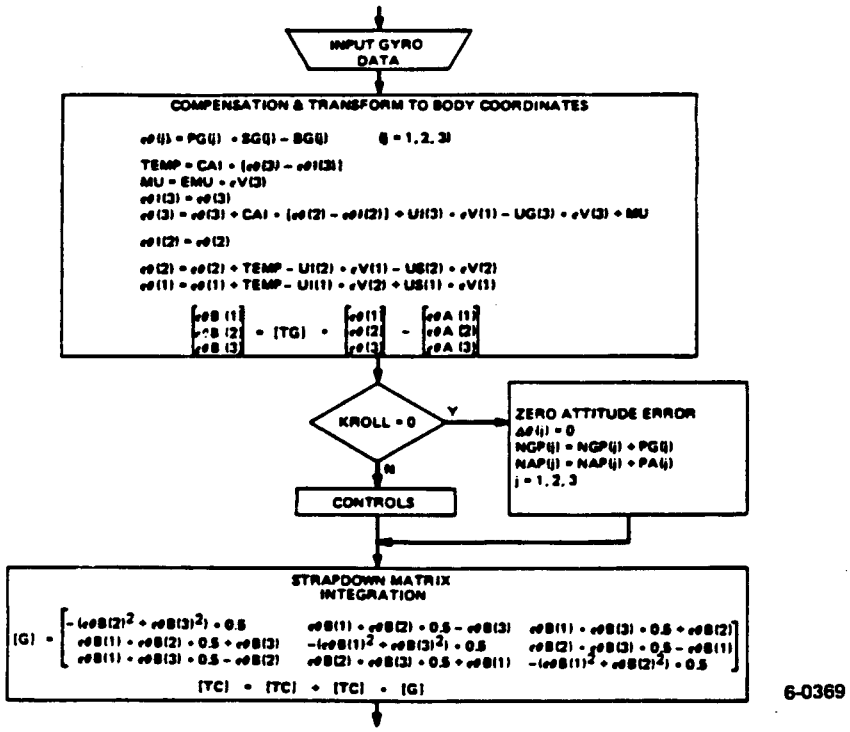


Figure 4.12.3-6. Gyro Data Processing Flow Diagram

4.12.3.3.1.1 Controls. The Controls equations' filter body rates compute the attitude errors in body coordinates, limit these parameters to prevent overflow, and resolve both the attitude error and vehicle rate data into the appropriate thruster coordinate frame. The logic and equations for the control equations are shown in Figure 4.12.3-7.

Rate data are actually incremental angular data integrated over the 20 millisecond IMU interval and then filtered as shown on Figure 4.12.3-8. Thruster coordinates are oriented as shown in Figure 4.12.1-5. On/off switching logic is applied in the thruster coordinate frame and used to set the appropriate thruster discretes.

The control system is used in several modes during the flight; these modes are controlled by a tabular control sequencer. Entries into the sequencer table include time and a control word for each mode. The control word (CW) contains the address of "BB" coefficients required for the phase plane on/off logic. If the CW is zero, the roll pointer is set to zero and used as a flag to bypass the controls logic.

4.12.3.3.1.1.1 On/Off Logic. The On/Off Logic controls the decisions for turning control thrusters on or off. These decisions are made based on a phase plane logic as shown in Figure 4.12.3-9; the logic and equations for the On/Off Logic are shown in Figure 4.12.3-10. The "BB" coefficients in this logic are referenced by address pointers, one for roll and one for pitch and yaw, defined by the control sequencer. Characteristics of this logic include the capability to have either an on-to-control or off-to-control system. Also,

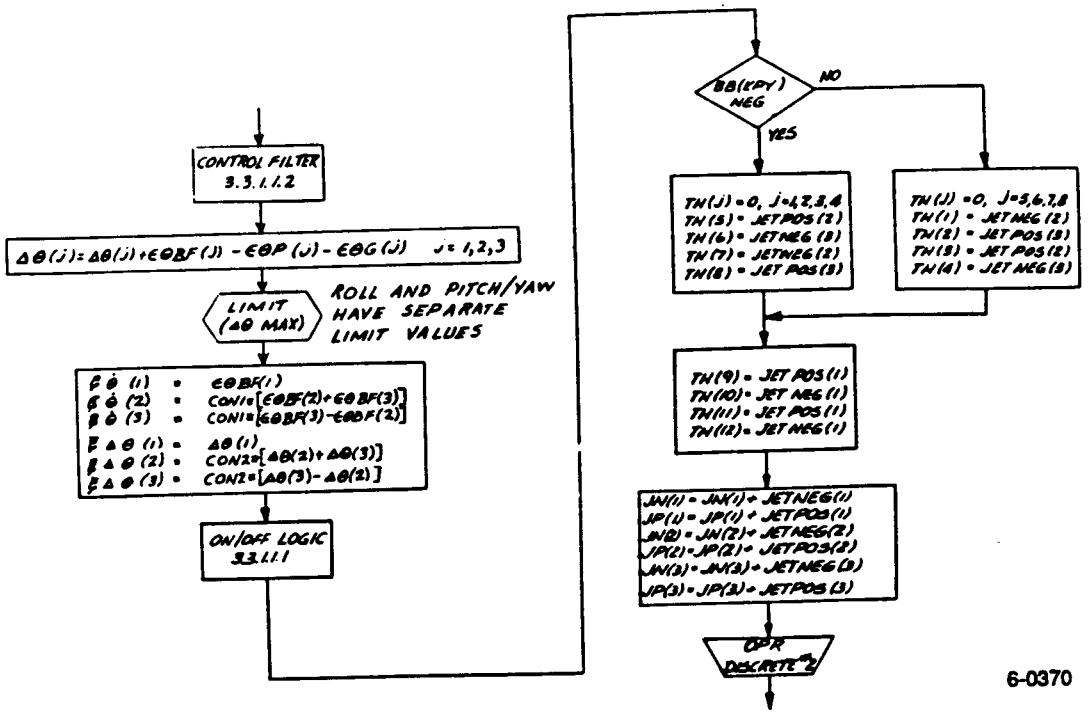


Figure 4.12.3-7. Controls Equations

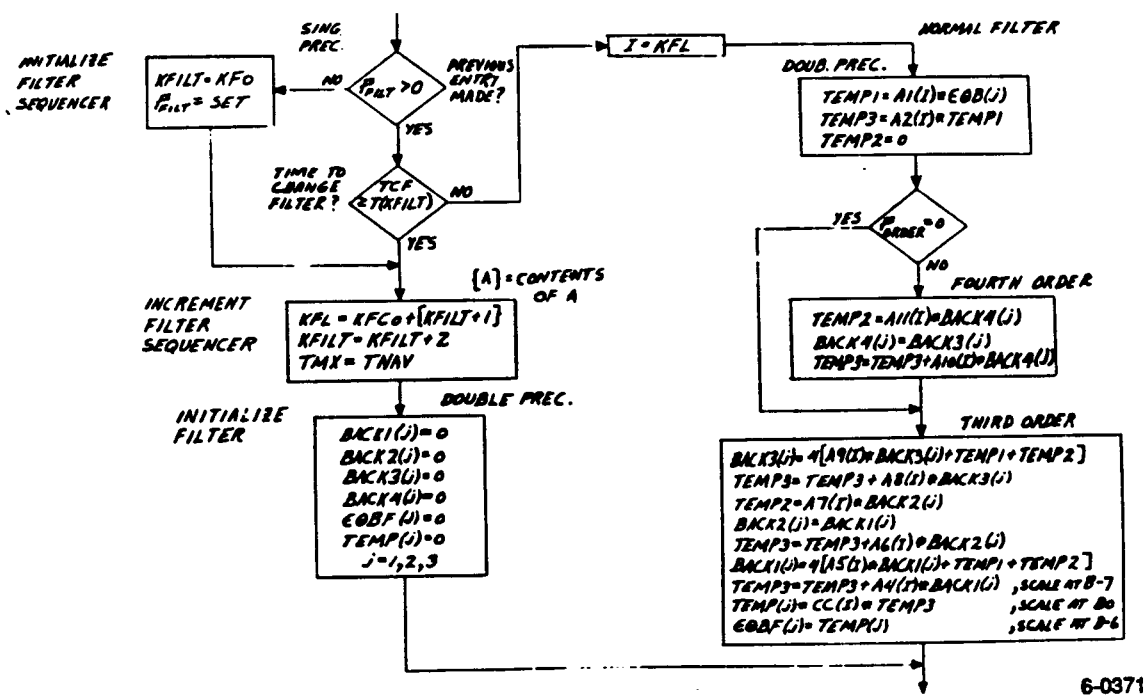


Figure 4.12.3-8. Control Filter Equations

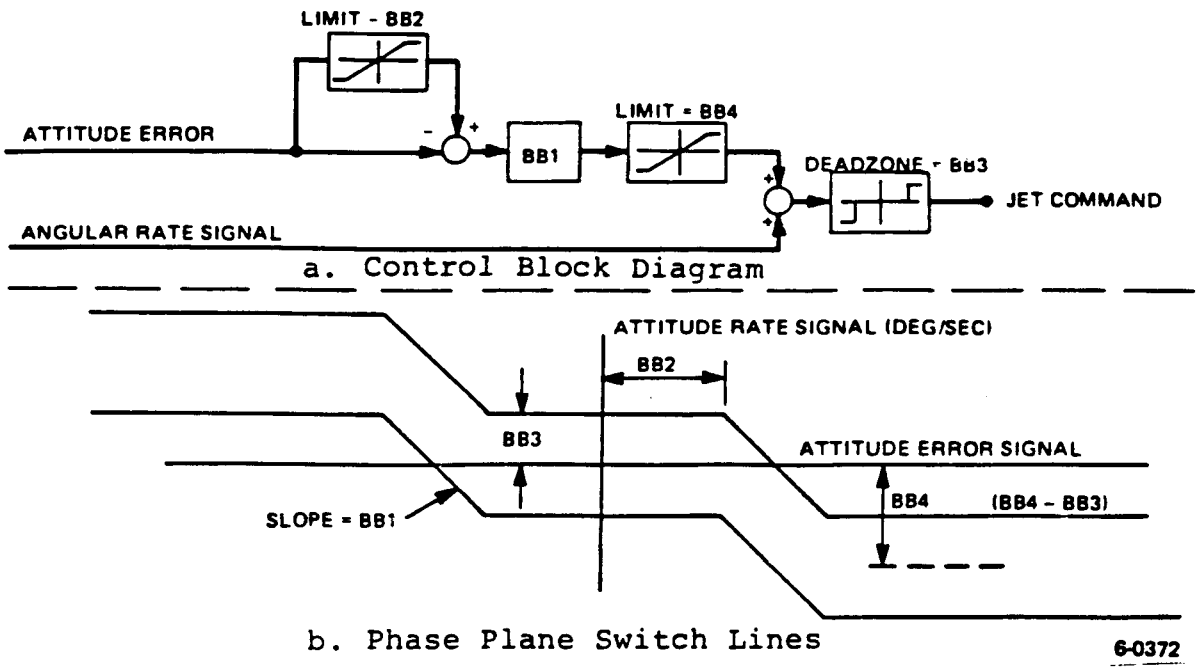


Figure 4.12.3-9. Control System Switch Line Characteristics

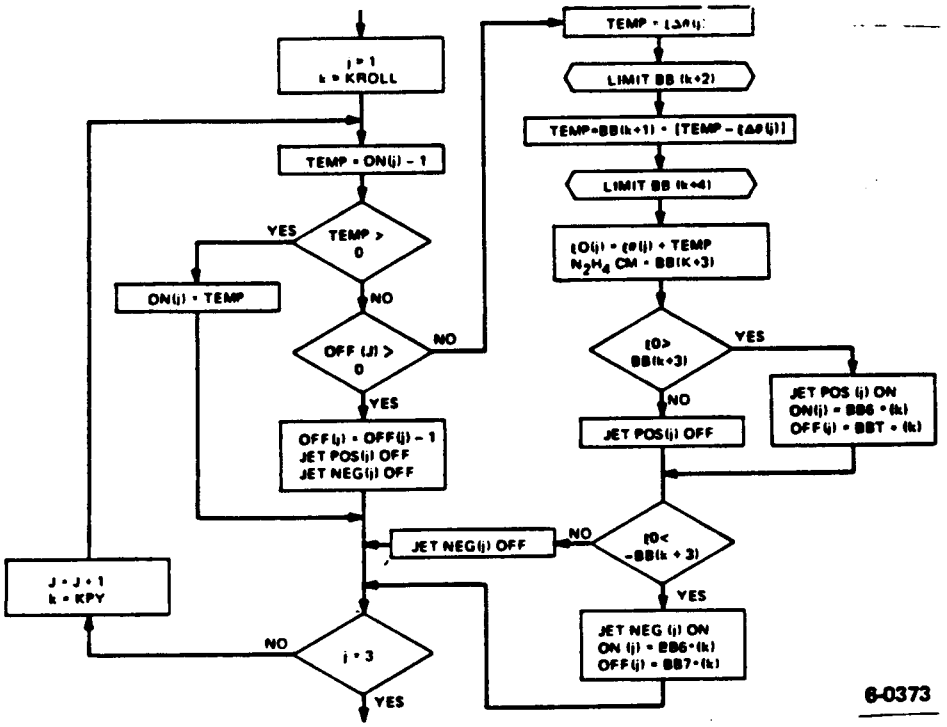


Figure 4.12.3-10. On-Off Logic Flow Diagram

the on and off times can be controlled an integer number of 20 millisecond intervals. These values as well as a flag to specify N_2 or N_2H_4 control are stored in a single "BB" coefficient as shown in Table 4.12.3-1.

TABLE 4.12-4. CONTROLS COEFFICIENT TABLE FORMAT

Table Entry	Parameter	BBX Word Makeup		
		1	2 3 4 5 6 7 8	9 10 11 12 13 14 15 16
1	BBX	X	X X X X	X X X X
2	BB1	1=N_2	Off Count	On Count
3	BB2	0=N_2H_4		
4	BB3			
5	BB4			
o				
o				
o				
.				
.				

The first entry in this table is a packed word containing the data for defining N_2 vs N_2H_4 control, and forced on and forced off control cycles as shown by the bit configuration above.

The BB coefficients 1, 3, and 4 are scaled by 1/50 to accommodate using rate data in the form of incremental angles over a 20 millisecond period.

4.12.3.3.2 Accelerometer Data Processing

The logic and equations for Accelerometer Data Processing are shown in Figure 4.12.3-11. This routine reads in the accelerometer data, compensates it for calibration-determined coefficients of scale factor and bias, and provides additional compensation for vertical axis scale factor and bias corrections as defined by the alignment equations. It then transforms the data to body coordinates in one of several possible orientations, allowing for test data to be added to the measured IMU data. Lateral accelerations are tested for unusually high values (failure indication); an observed high value is replaced with a zero value. Continuous sums of this data for 0.5 second periods are provided in each body axis and are used as averaged data in alignment and 2/second computations.

4.12.3.3.3 Telemetry Store

This routine moves 25 words of computational data into 1 of 2 telemetry storage areas for efficient telemetry output processing. There are 2 frame-length 25-word buffer memory storage areas used in a ping-pong fashion to store the telemetry data. The details of the telemetry processing are given in Section 4.12.4.

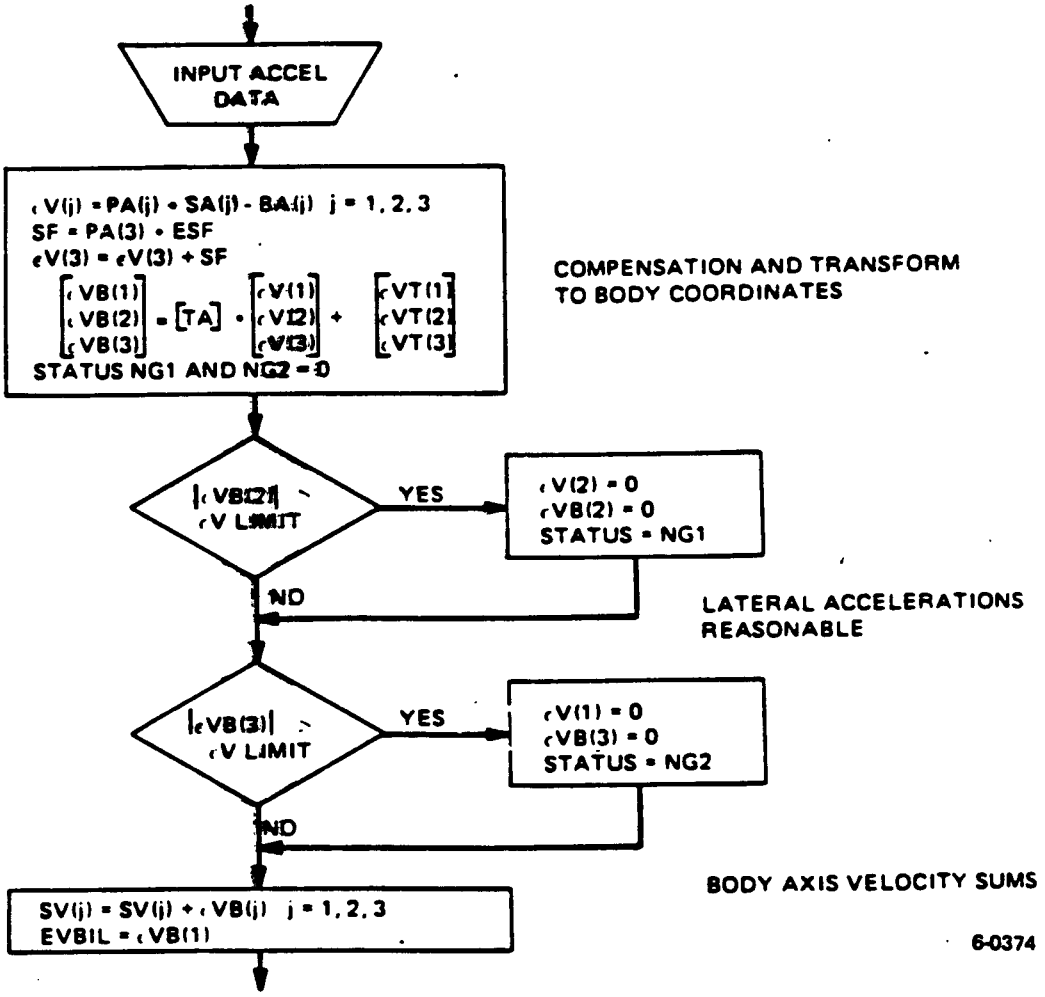


Figure 4.12.3-11. Accelerometer Data Processing Flow Diagram

The logic for moving these telemetry words into the buffer storage areas is shown in Figure 4.12.3-12. The flag controlling entry to this routine is set by the TM Interrupt routine. Telemetry words 11-16 are variable words which may be modified via loading of mission constants. On occurrence of a level 16 error interrupt, 3 of these words are reassigned as error status words and remain so for the remainder of the flight. The level 16 status is part of the normal telemetry stream.

4.12.3.3.4 Orthonormalize

This routine restores orthogonal and normal characteristics to a 9 element body to inertial transformation matrix; the equations and logic flow are mechanized as shown in Figure 4.12.3-13. The routine uses the second row (pitch axis) as the reference element for restoring the orthogonal characteristics. First order approximations for M≈1 are used to eliminate the divide and square root functions for $1/M^2$ and its square root.

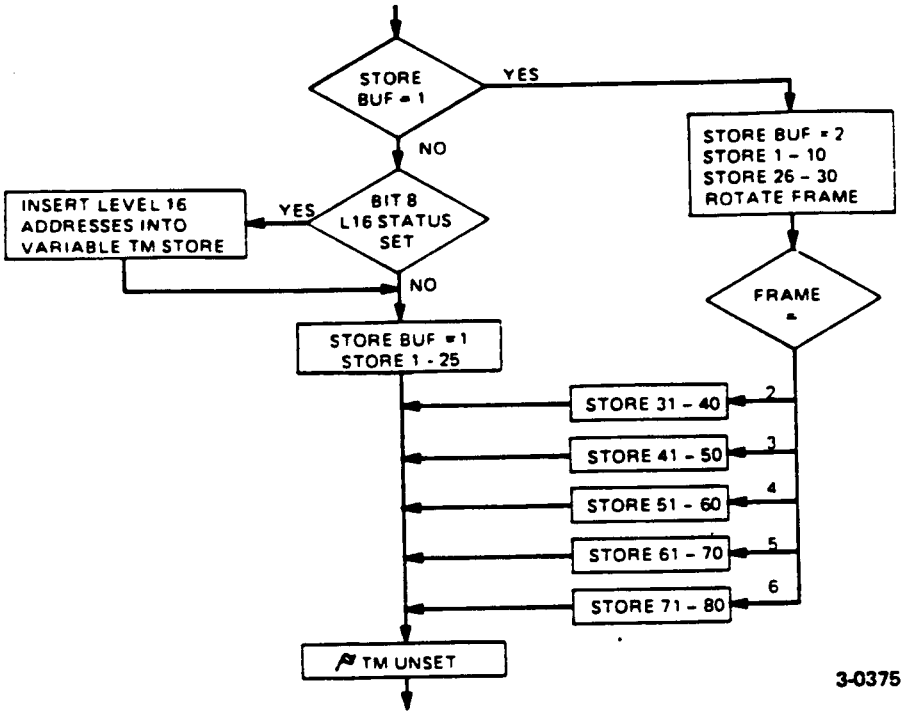


Figure 4.12.3-12. Telemetry Store

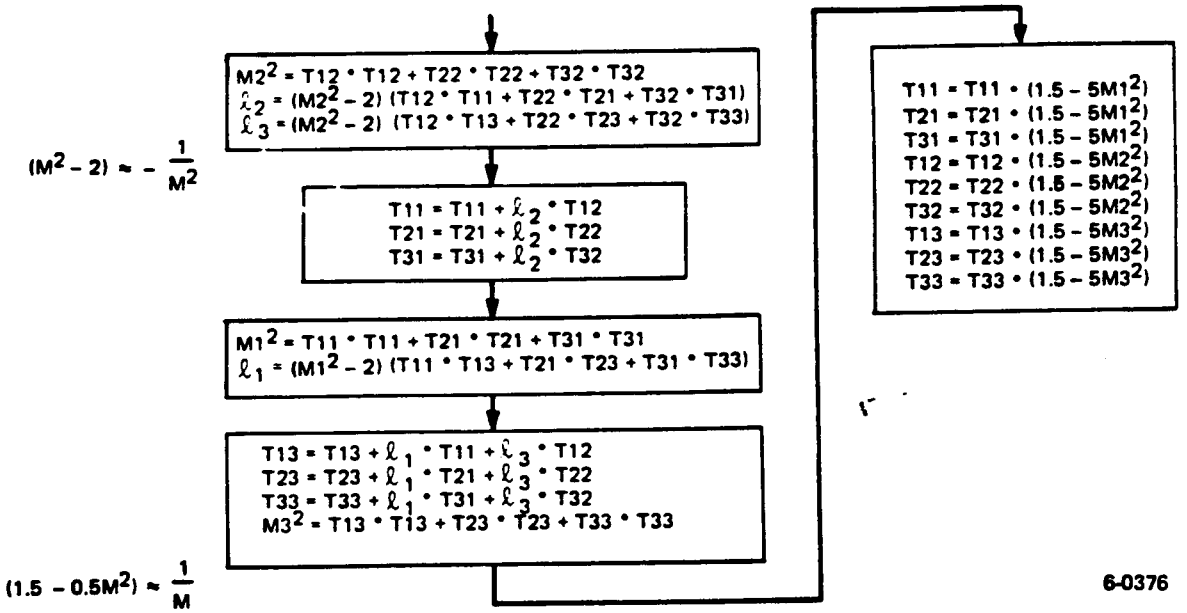


Figure 4.12.3-13. Orthonormalize

4.12.3.3.7 Initialization

This routine initializes all flight and pre-launch parameters to insure proper equation operation for all program modes. The parameters to be initialized and logic flow for IMU orientation determination are shown in Figure 4.12.3-15 (TBD).

All parameters which are normally updated via a test mode, including a simulated flight, are capable of reinitialization without program reload. IMU orientation determination utilizes acceleration data, $\varepsilon V(j)$, to establish the accelerometer and gyro sensor to body transformation matrices. If a determination cannot be made, i.e., no output approximates 1 g, these matrices are zeroed and psuedo IMU data are provided through the gyro and accelerometer alignment bias terms. This routine also outputs a zero to the 2 discrete word registers in the CIU.

4.12.3.3.8 Closed Loop Test

These equations provide the stimuli to simulate the Titan II burn phase of the mission as well as the ATN acceleration and control functions. During the Titan II burn, the acceleration profile is curve-fit in inertial coordinates, and pitch and yaw rates are determined by resolving this data into body coordinates and commanding rates to null the pitch and yaw components. The logic and equation mechanization for this routine is defined in Figure 4.12.3-16 (TBD).

The curve fit coefficient acceleration data is shown in Table 4.12.3-1. This is a bootstrap arrangement and requires high gains to maintain a small acceleration pointing error. Roll attitude change is provided by a constant rate over a fixed interval early in the Titan II burn phase of the trajectory. After second stage shutdown is achieved, vehicle simulation is converted to the ATN-KLM model for the remainder of the closed loop test time.

The model provides the control moments and vehicle acceleration created by the control system and AKM burn and hydrazine velocity trim burn. The control system, consisting of 12 thrusters, has 4 hydrazine thrusters (1-4) which create both moment and acceleration, and 8 nitrogen thrusters (5-12) which create only moments.

The moment and thruster acceleration equations are written to reflect a unity value for an "on" thruster and a zero value for an "off" thruster. External moments, MO(j), during the AKM burn are provided as mission constants, MX(j). AKM acceleration is mechanized as a time function of remaining burn time (TAC). This equation is mechanized by directly scaling to increments of velocity; therefore, acceleration magnitude parameters are divided by 50 to take into account the 20 millisecond computational rate. Expected IMU output data is subtracted from the X axis velocity increment data so that it can be added in its normal manner in the IMU acceleration processing equations.

TBD

Figure 4.12.3-15. Initialization (TBD)

TBD

Figure 4.12.3-16. Closed Loop Test Flow Diagram (TBD)

TABLE 4.12-5. GUIDANCE CURVE FIT COEFFICIENTS TABLE

Table Entry	Parameter	Comment
1	TX(IS)	Curve Fit Segment End Time
2	X(I+1)	X Axis Coefficients
3	X(I+2)	
4	X(I+3)	
5	X(I+4)	Y Axis Coefficients
6	X(I+5)	
7	X(I+6)	
8	X(I+7)	Z Axis Coefficients
9	X(I+8)	
10	X(I+9)	
.		
.		
.		

These coefficients continue for as many segments as necessary to completely define a guidance interval. It is a requirement that the end time TX(IS) for the last segment must be identically equal to the end time TF (K+1) for the guidance mode in which it is used. These curve fits need only be defined over the trajectory interval where guidance is active.

4.12.3.3.9 Control Test

These equations provide a means of exercising all the entries in the control sequencer via a fixed attitude error pattern. The logic and equations for this routine are shown in Figure 4.12.3-17 (TBD).

The system is stepped through each control sequence mode for 10 seconds and, at each change, the attitude error pattern shown in Figure 4.12.3-18 is exercised. Roll and pitch attitude errors only are generated, since pitch error will cause all the pitch/yaw jets to be exercised. At the conclusion of this test, the system will reinitialize the control system and revert back to the Initialization mode.

TBD

Figure 4.12.3-17. Controls Test Flow Diagram (TBD)

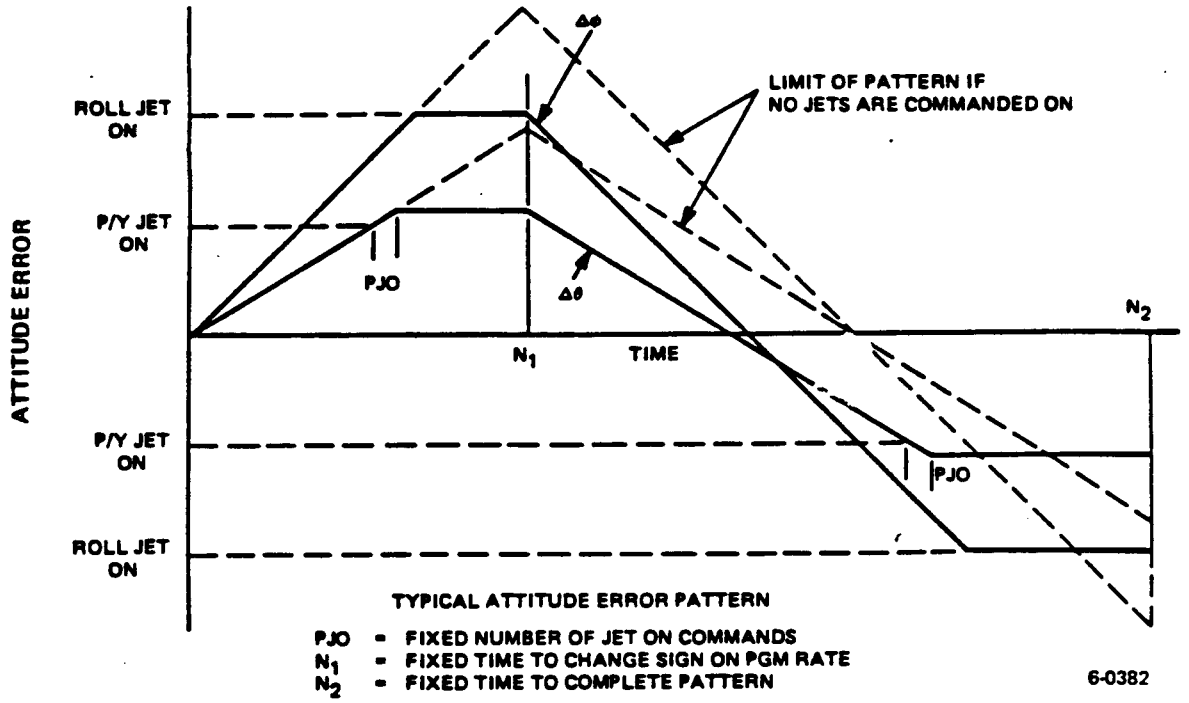


Figure 4.12.3-18. Control Test Attitude Error Pattern

4.12.3.3.10 Navigational Test

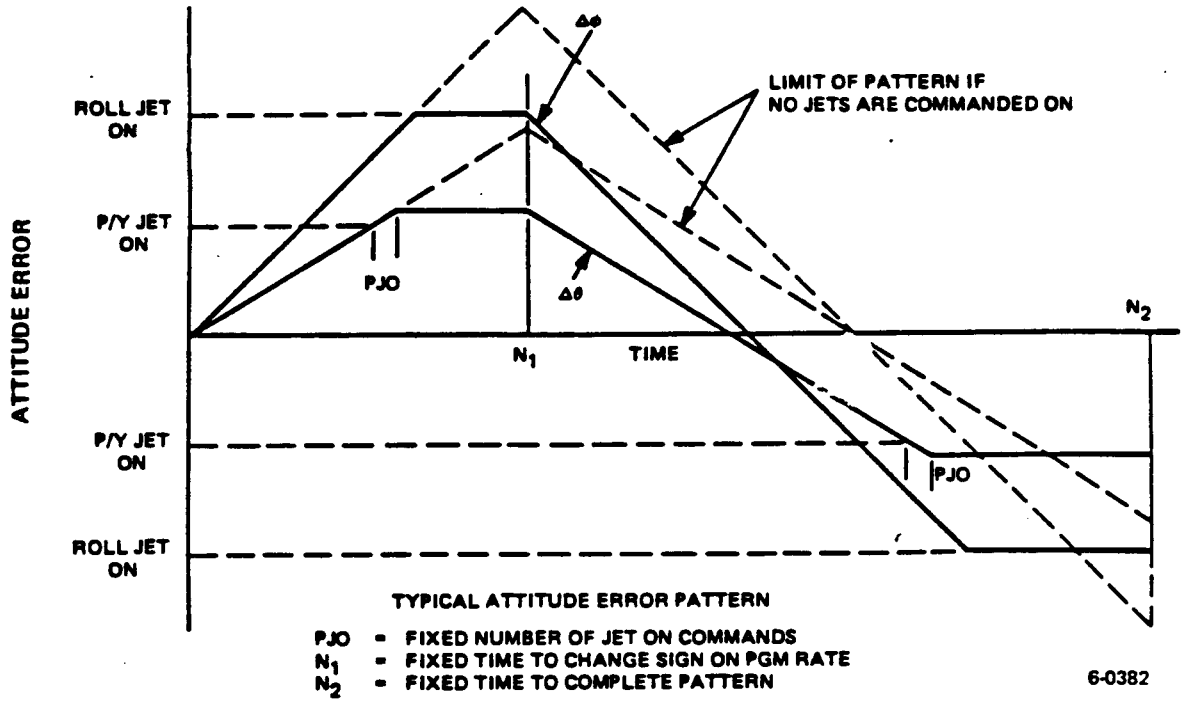
This routine transfers the system from an alignment mode to a navigation mode and provides timing control for a fixed navigation run. The logic and equations for this routine are shown in Figure 4.12.3-19.

The TEST flag is used as an initialization flag for setting gyro and accelerometer correction coefficients based on alignment data, and zeroing the necessary parameters to start an accurate navigation run. During the run, navigation time is the only time base updated. When navigation time exceeds a preset value, translational navigation is terminated by setting the AFAIL flag. Actual termination of the test is held off for 60 seconds via a KNAVTST counter to allow ample time for telemetry processing of the final navigated position and velocity vectors. Run termination is automatically enacted by zeroing the Run mode to force return to the Initialization mode.

4.12.3.3.11 Manual Control Test

This routine, exercised by run mode number 5, initializes the control configuration to the flight configuration at time TMCT. The logic for this test mode is defined in Figure 4.12.3-20 (TBD).

After initialization of this routine to the desired control sequence, the test flag is set to avoid further incrementation of the sequencer. The controls equations are in an uncaged configuration and all inputs from the IMU will be acted upon by the controls equations in a normal manner for the selected control mode. Termination of the test requires that run mode be set back to zero



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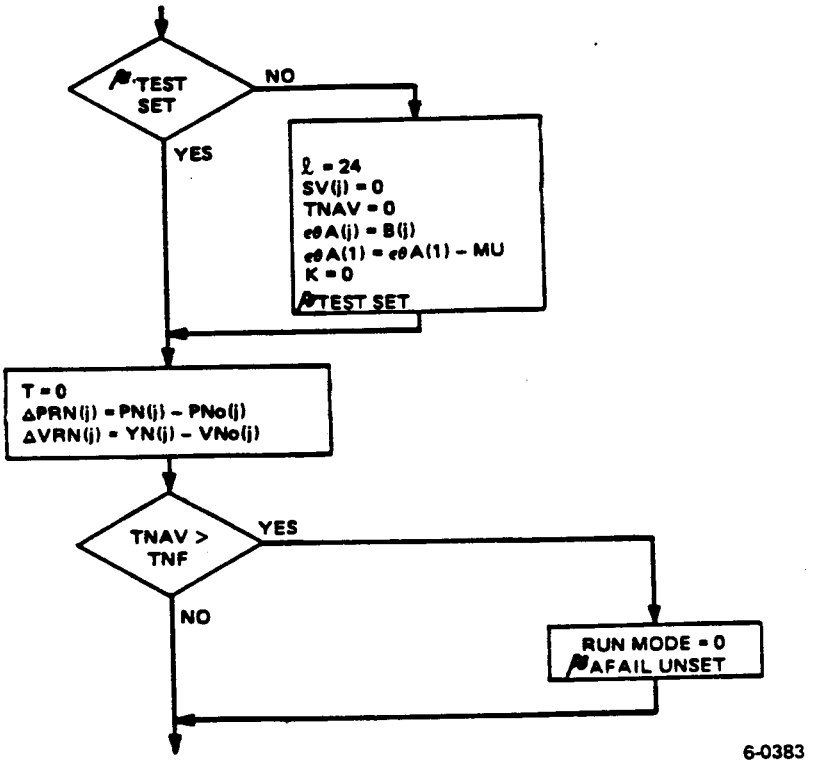

Figure 4.12.3-19. Navigation Test

TBD

Figure 4.12.3-20. Manual Controls Test (TBD)

so that the Initialization routine may reinitialize the control system. All response will be determined by the manual input and normal control system response. Thrusters will be turned on and off as dictated by the rate and integrated attitude errors.

4.12.3.3.12 Liftoff Detection/Alignment

This logic first tests both the vertical (axial) acceleration level (sum of the last and current cycle data) and a vehicle input discrete for an indication of a liftoff. The logic control for implementing liftoff detection is shown in Figure 4.12.3-21 (TBD).

If commitment to liftoff is not made, flow proceeds into the vertical accelerometer compensation and the alignment equations. Accelerometer compensation is accomplished by using axial accelerometer data and comparing it to the 1 g reference value; the difference is summed using a low gain to form a total error. This error is used to generate a scale factor coefficient which in turn generates a scale factor correction in the accelerometer processing loop. The residual error is then used to correct the axial accelerometer bias as the difference between the total error and the scale factor correction.

TBD

Figure 4.12.3-21. Liftoff Detection/Alignment (TBD)

Liftoff commitment requires three detections; liftoff detection reset requires two successive non-detections. During the transient stages of liftoff detection, the axial accelerometer compensation is bypassed based on the detect flag being set. This prevents liftoff accelerations from degrading the axial accelerometer bias and scale factor compensation terms.

The liftoff logic is exercised both for the real liftoff and for a closed loop test simulated flight. For the latter case the run mode is less than 3 so the PRELAUNCH flag is not committed and a TEST flag is set to indicate simulated liftoff. Liftoff commit exercises the appropriate initialization to transform the system from alignment to a flight mode.

4.12.3.3.12.1 Alignment. Alignment is achieved by generating the angular errors between the TC matrix based on gyro and alignment correction data and a reference TC matrix based on horizontal accelerometer data and a fixed azimuth. The equations and logic for this routine are shown in Figure 4.12.3-22.

The azimuth data will be updated as a step input based on a porro prism measurement taken while the system is operating in the alignment mode. The required reference matrix elements (6 total) are updated on a larger time scale than the 50/second computation rate to allow more averaging of the horizontal accelerometer data.

The error signal is filtered using a first order filter having a long time constant. This attenuates the effects of vehicle sway, since this dynamic effect is not adequately measured by the accelerometer data. When the squared sum of the alignment errors gets below a threshold value, this signal is summed to provide a bias correction to the alignment scheme. The bias in the axial channel is converted to a mass unbalance coefficient proportional to the total bias. The earth rate components are then added to the biases and the mass unbalance correction coefficient is subtracted from the axial channel data. The mass unbalance coefficient is calculated in the gyro processing loop so the last computed value is used in the axial channel correction. The corrections defined by these effective biases observed during alignment will be left in the system after liftoff for in-flight compensation.

4.12.3.4 Level 6 Interrupt (2/Sec Computations)

The computations mechanized at this interrupt level include the position and velocity navigation equations, guidance control for sequencing guidance events, sequencer control including the time limiting function used to sequence at discontinuous events, and discrete-off logic for generating pulse length discretes. The equations and executive control of the 2/second interrupt level are shown in Figure 4.12.3-23. Setting of the level 6 interrupt is controlled by the 50 to 2/second interface equations in the IMU level interrupt.

The position and velocity computations represent trapezoidal integration of inertial velocity increments summed over 0.5 second intervals in the IMU interrupt loop. Guidance phasing is controlled through targeting tables which contain start and stop times for each phase as well as data peculiar to the phase. The guidance initialization routine provides initialization and sets the closed loop guidance flag, CLG. Closed loop guidance provides three types of guidance

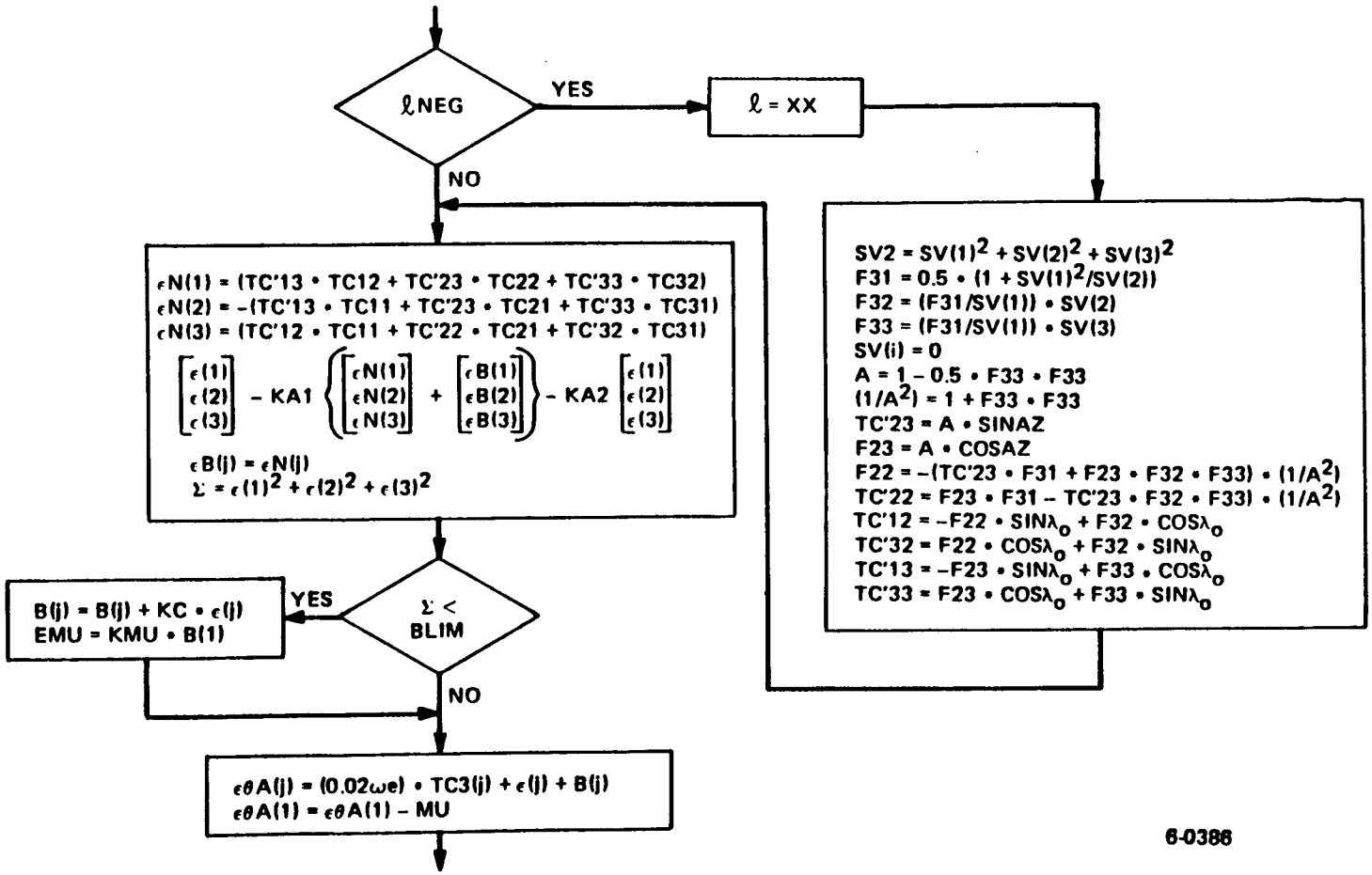

Figure 4.12.3-22. Alignment Logic Flow Diagram

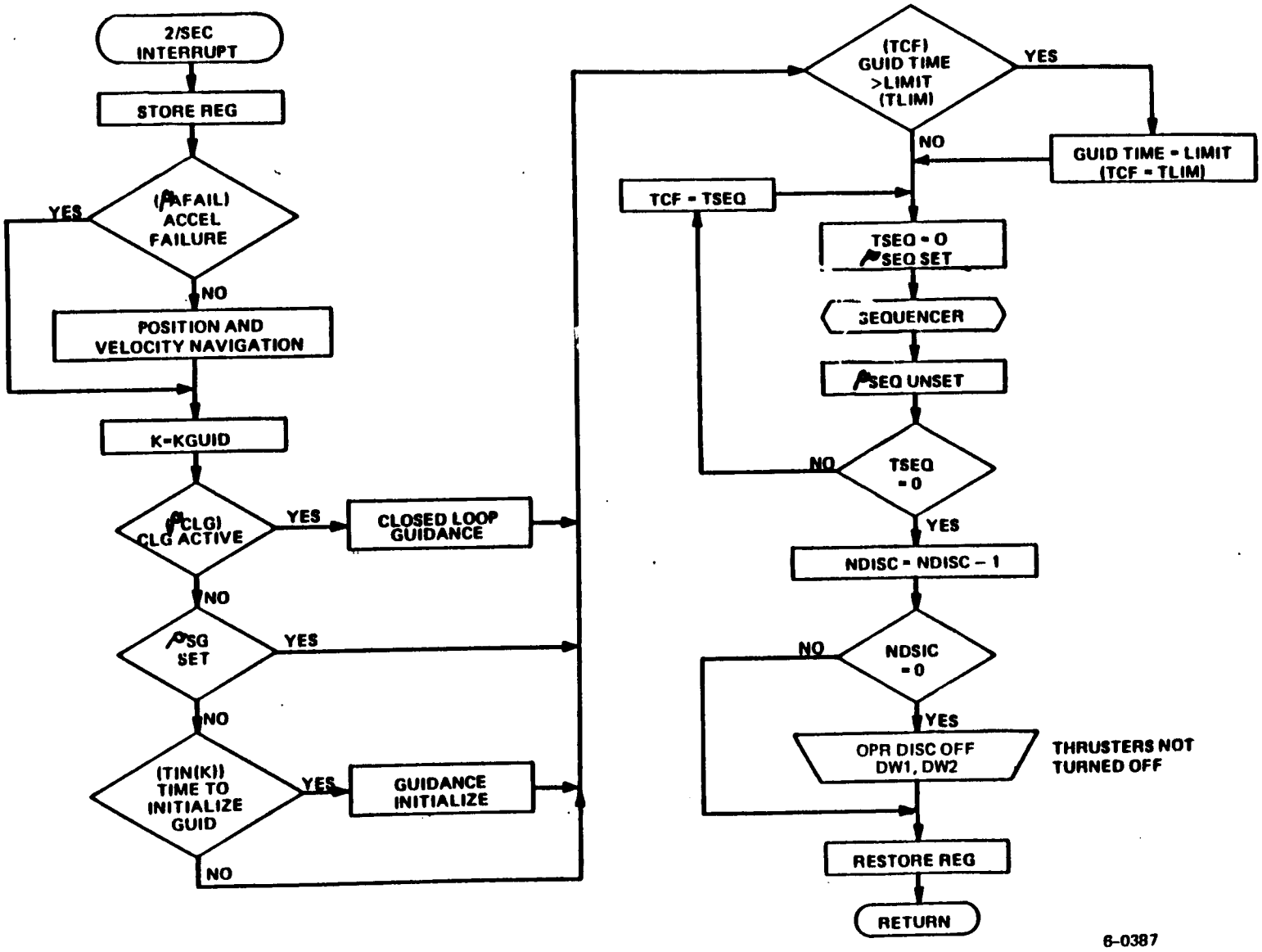

Figure 4.12.3-23. Level 6 Interrupt Logic Flow Diagram

modes: attitude pointing, coast guidance, and powered flight guidance. Close-out of these routines increments the guidance targeting pointer (KGUID) to the next set of targeting constants, allowing the system to continue for "N" modes.

4.12.3.4.1 Position and Velocity Navigation and Gravity Subroutine

Position and velocity calculations are propagated in this routine using summed inertial velocity over the previous 0.5 second as the forcing function. The equations for both the position/velocity navigation and the gravity subroutine are shown in Figure 4.12.3-24.

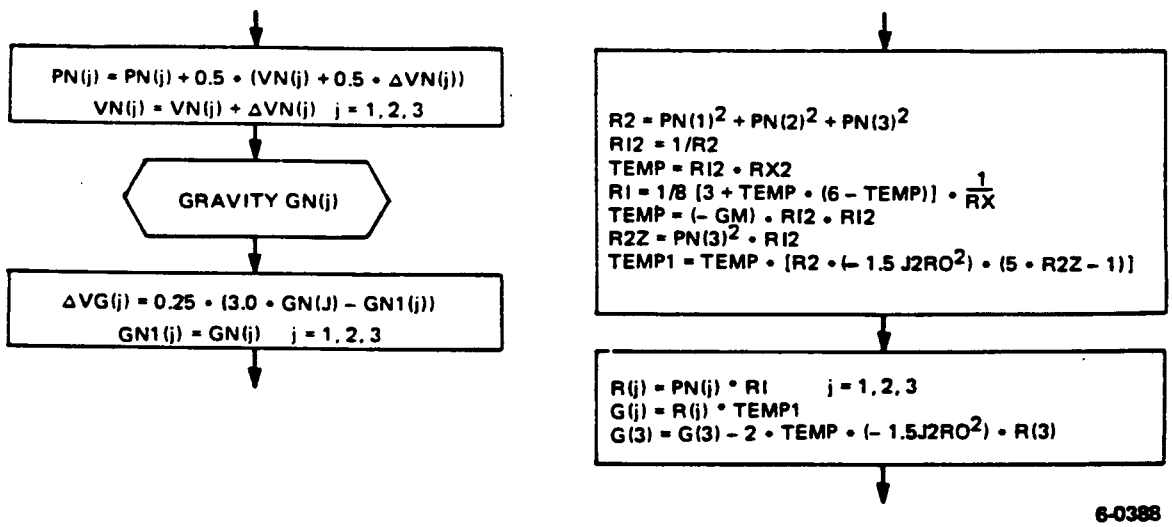

Figure 4.12.3-24. Navigation and Gravity Flow Diagrams

The gravity subroutine is called after the position vector has been updated and the data is combined with the last gravity data to predict a velocity increment due to gravity to be used during the next 0.5 second. The gravity subroutine uses a normalizing radius vector square, RX2, to allow an approximation for the square root such that RX2/RI2 ≈1.0. After the approximation for the square root, the resultant parameter is re-scaled to the true value of RI by multiplying by (1/RX). The two parameters, RX2 and 1/RX, will take on three different pre-set values during the mission. The first value is established by initialization, the second value is assigned by a special guidance mode prior to Titan II SECO, and a third value is assigned during coast guidance initialization. The values of RI and R(j) as well as the gravity values G(j) are used outside this subroutine.

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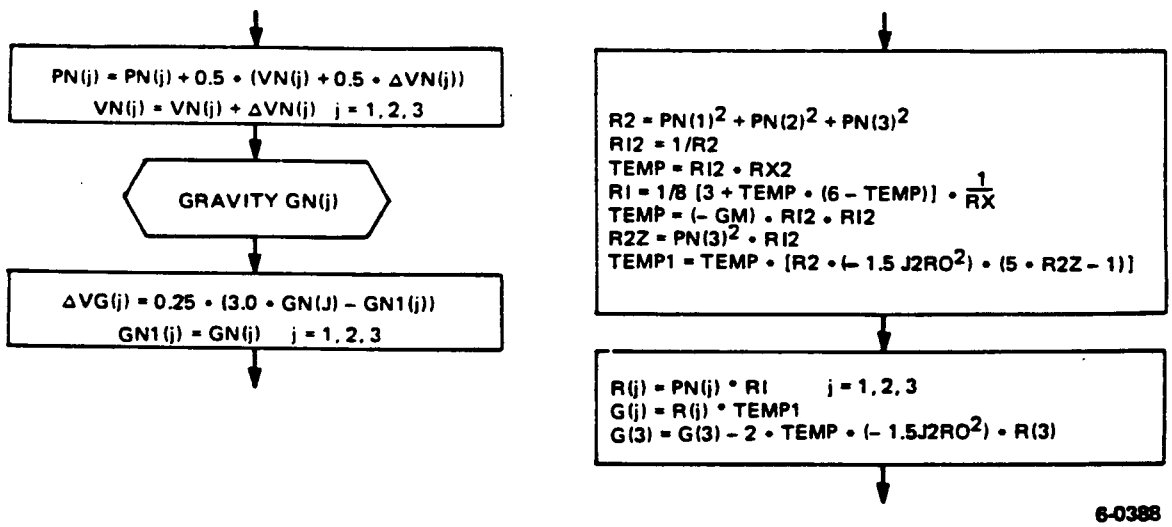

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4.12.3.4.2 Closed Loop Guidance

This routine contains the equations and logic to exercise the three modes of closed loop guidance (powered flight, coast guidance, and attitude pointing). The logic and equation definitions for this routine are shown in Figure 4.12.3-25.

These equations and logic are intermixed in a manner to minimize duplication between the three modes. When time to go is less than the targeted time to guidance stop, ΔTSG, for a given guidance mode, closed loop guidance is terminated and the targeting table pointer (KGUID) is advanced to the next set of data.

In the powered flight mode of guidance, axial acceleration data are tested against upper and lower reasonableness bounds and guidance is terminated if outside of these bounds. The parameters PF and VF represent working variables that will be updated through the logic and end up defining the predicted final position and velocity.

In the coast guidance mode, AKM ignition conditions are predicted using an average gravity acceleration and the computed time to ignition. The navigational velocity increment over the last 0.5 second is overlayed with an equivalent value due to gravity at AKM ignition. This is to allow the powered flight predictor to compute total thrust acceleration as the acceleration error during coast guidance. A flag is set and the value of ignition velocity (VO) is retained for iteration on ignition time. Based on the predicted ignition position, the gravity routine is called to update gravity to be used in the next pass through these equations. Having either present vehicle or predicted AKM ignition position and velocity, a common set of powered flight predictor, guidance error, and steering equations are used to complete the closed loop guidance for either powered flight or coast guidance modes.

In the attitude pointing guidance mode, pertinent position and velocity components in the vehicle axes are steered to a null condition. This provides orientation of the vehicle relative to the orbit. Steering gains are furnished as targeting parameters. Control system attitude error feedback is used to provide steering stability. Closeout logic provides for advancing the guidance table pointer, setting the cutoff time TCO for 20 millisecond resolution on calling the sequencer, activating the acceleration sense logic in mode control, and zeroing out guidance steering and the closed loop guidance flag. The accelerometer fail logic provides for either terminating all further closed loop guidance by setting the fail flag and setting the next guidance table entry time to Tmax or, in the case of N_2H_4 depletion, setting up for continued normal sequencing as though it were a planned shutdown.

The last function of this routine is to limit all guidance steering commands and sum the limited commands for telemetry output.

4.12.3.4.2.1 Powered Flight Predictor. This routine computes predicted final position and velocity and current acceleration error; the logic and equation flow for this routine are shown in Figure 4.12.3-26.

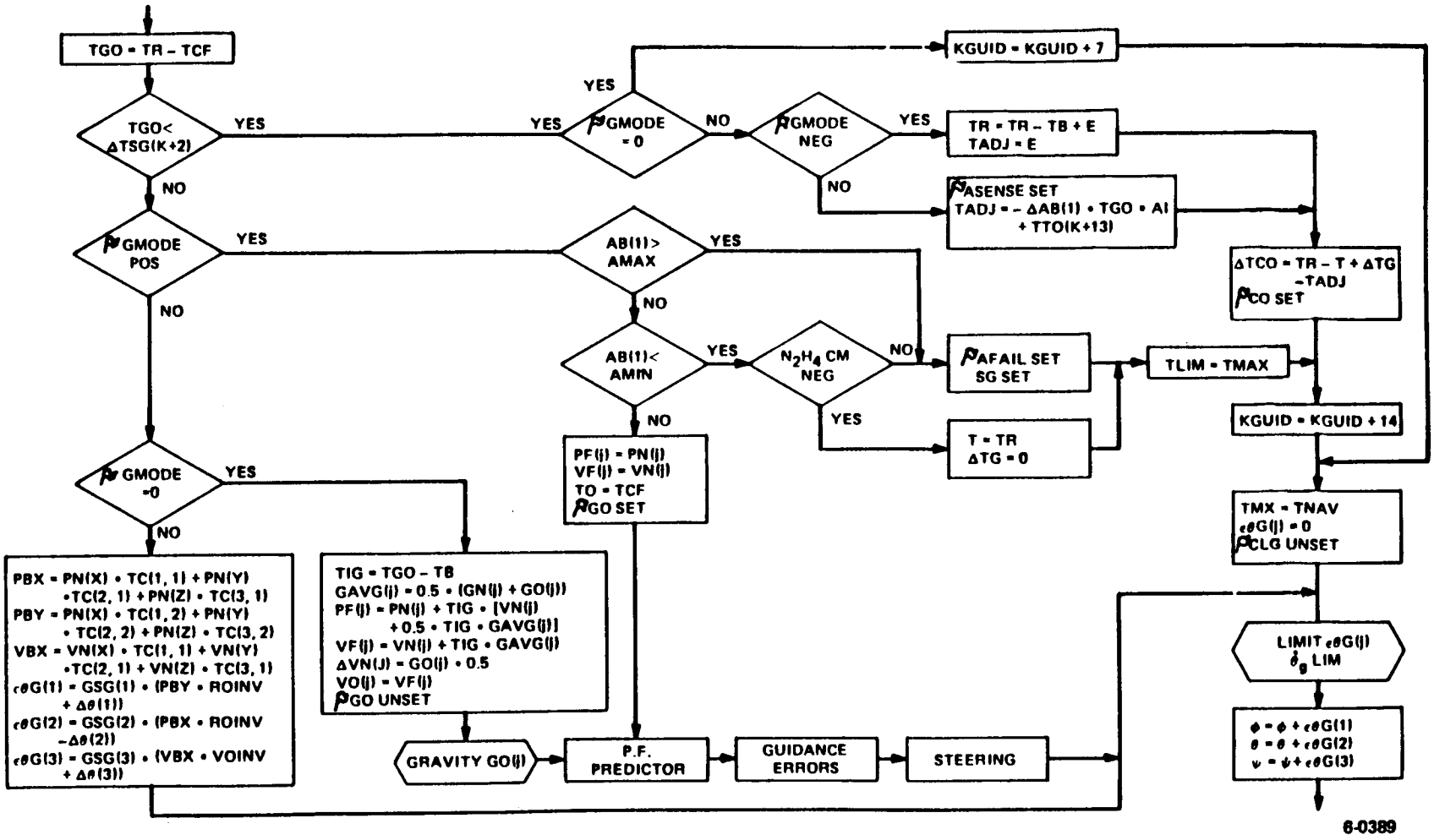

Figure 4.12.3-25. Closed Loop Guidance Flow Diagram

The primary predictor uses second order curve fits of total inertial acceleration as the basis for prediction. The coefficients for successive segments of these curve fits are stored as tabular data in a format shown in Table 4.12.3-1. The acceleration curve fits represent total acceleration in inertial coordinate components and satisfy the constraints that the first and second integrals over each segment equal the velocity and position gained in that segment.

An alternate predictor is available during the velocity trim burn using an average gravity plus constant inertial acceleration. It is implemented when the TSV value is set greater than Tmax. The TSV value is input in the guidance targeting tables for powered flight guidance modes. The alternative predictor is the preferred approach for the low thrust acceleration trim burn where gravity is predominant and significant Δt_{orb} and Δt_g adjustments cause the gravity direction to be non-nominal.

4.12.3.4.2.2 Guidance Errors. This routine defines position and velocity errors at the desired end conditions, utilizes these errors to drive ignition time and targeted position so as to null position errors, and establishes a velocity/acceleration relationship in body coordinates which satisfies the steering law. The logic and equation flow for this routine are shown in Figure 4.12.3-27.

The flag used to iterate the ignition time adjustment equations is originally set in the closed loop guidance equations and changed in the iteration cycle. In the ignition time iteration for coast guidance, time to go is set equal to the burn time to accommodate proper conversion of velocity error to acceleration required in the steering equations which follow. Ignition velocity along the desired final position vector, VOV, is generated and tested against a minimum positive value prior to its use in scaling position error to time. The ignition time adjustment is made such as to null position error along the desired final position vector.

These equations take into account the velocity error along the final position vector which will be nulled by a constant acceleration error during AKM burn. This in turn will create a position change during AKM burn not seen in the predicted position error. Ignition time changes are implemented on successive 2/second computations by modifying the guidance time adjustment parameter, ΔTB. Effects on predicted final position and velocity due to time change determined on the current cycle are computed and used to update position and velocity error prior to defining changes in the desired orbit injection condition.

Changes to the targeted position and velocity in terms of defining a desired position and velocity are generated through the time parameter Δt_{orb}. This parameter represents a time shift along the orbit such that the position error along the orbit velocity vector is nulled. Using this parameter, the desired final position and velocity are updated based on average gravity between the targeted position and the desired position computed during the previous cycle. From this updated position and velocity, the position and velocity errors are again calculated and these errors, along with acceleration error defined by the powered flight predictor, are resolved into body coordinates. These data are next acted upon by the steering equations which compute incremental guidance steering commands for use in the controls equations.

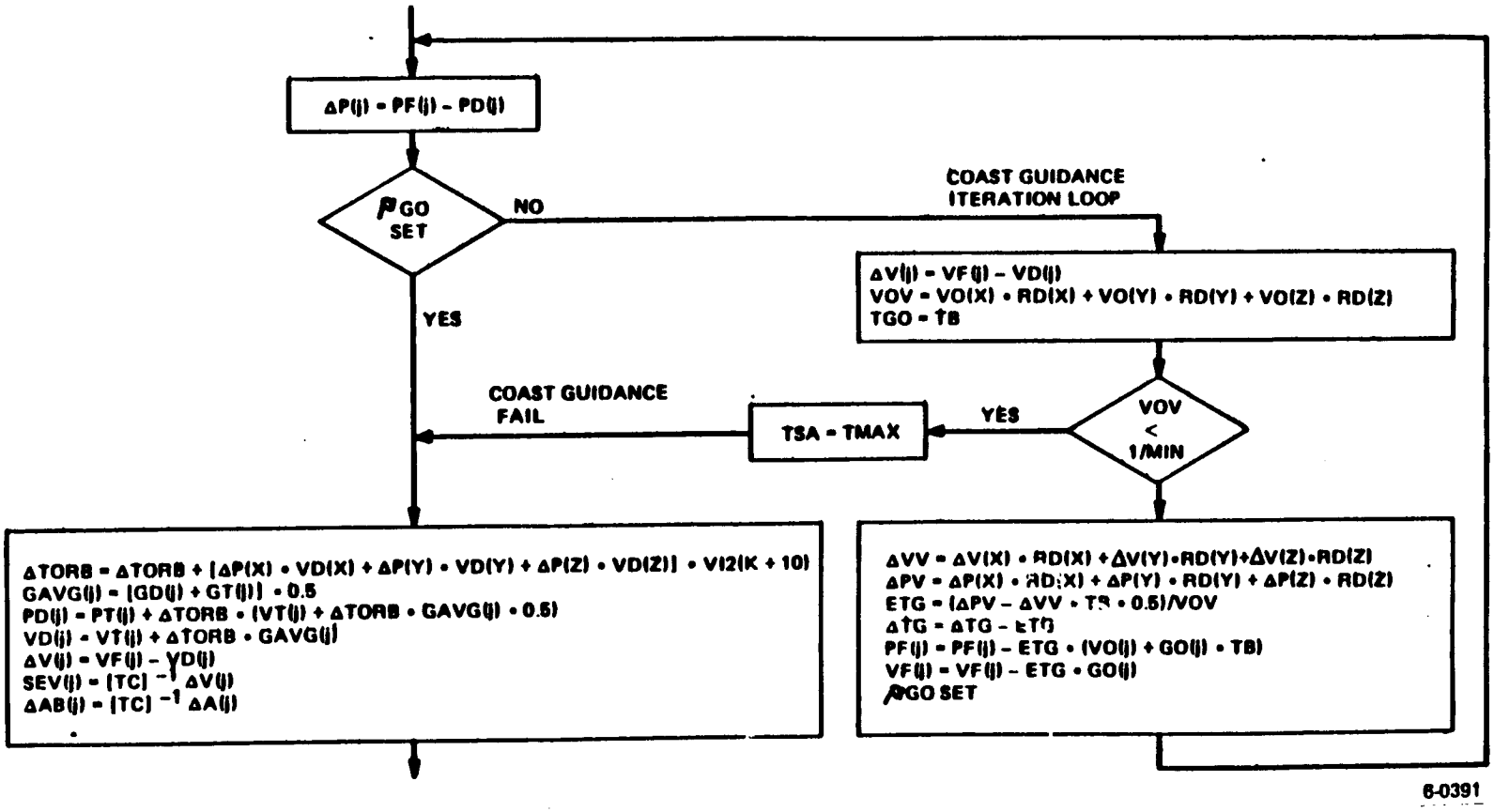

Figure 4.12.3-27. Guidance Error Flow Diagram

4.12.3.4.2.3 Steering. The steering routine processes guidance error signals in velocity and acceleration and generates corrective steering rates. The equations and logic for this routine are shown in Figure 4.12.3-28.

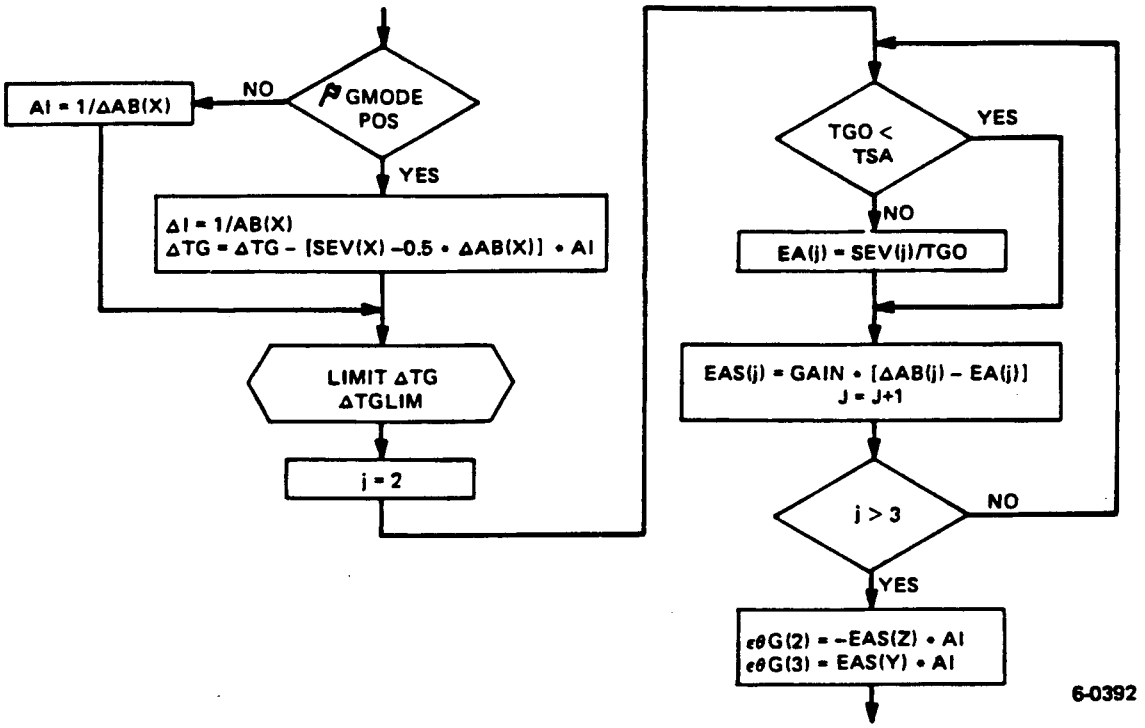

Figure 4.12.3-28. Guidance Steering Flow Diagram

To create total loop response independent of the acceleration level, the inverse of acceleration is used as part of the total proportional gain. For powered flight guidance the inverse is based on measured X body acceleration, AB(X). For coast guidance it is determined from the powered flight predictor acceleration error resolved into the body X axis. This acceleration error represents the difference between total acceleration defined in the predictor and gravity at ignition and is, therefore, the total thrust acceleration. With the body axes near nominal the X component will reflect the proper steering gains.

During powered flight guidance, time to go changes are computed proportionally to observed velocity and acceleration errors in the X body axis. For coast guidance, time change is handled in the guidance error routine. Steering rate computations for both these guidance modes are the same; they use position and velocity errors and time to go to define desired acceleration corrections. These are compared with measured acceleration corrections and the steering errors are proportional to these differences.

At a targeted time to go, TSA, the velocity error updates are discontinued and corrections are made based only on changes in acceleration errors. The outputs are scaled into increments of angles representing the desired steering rates applied over a 20 millisecond period.

4.12.3.4.3 Guidance Initialize (TBD)

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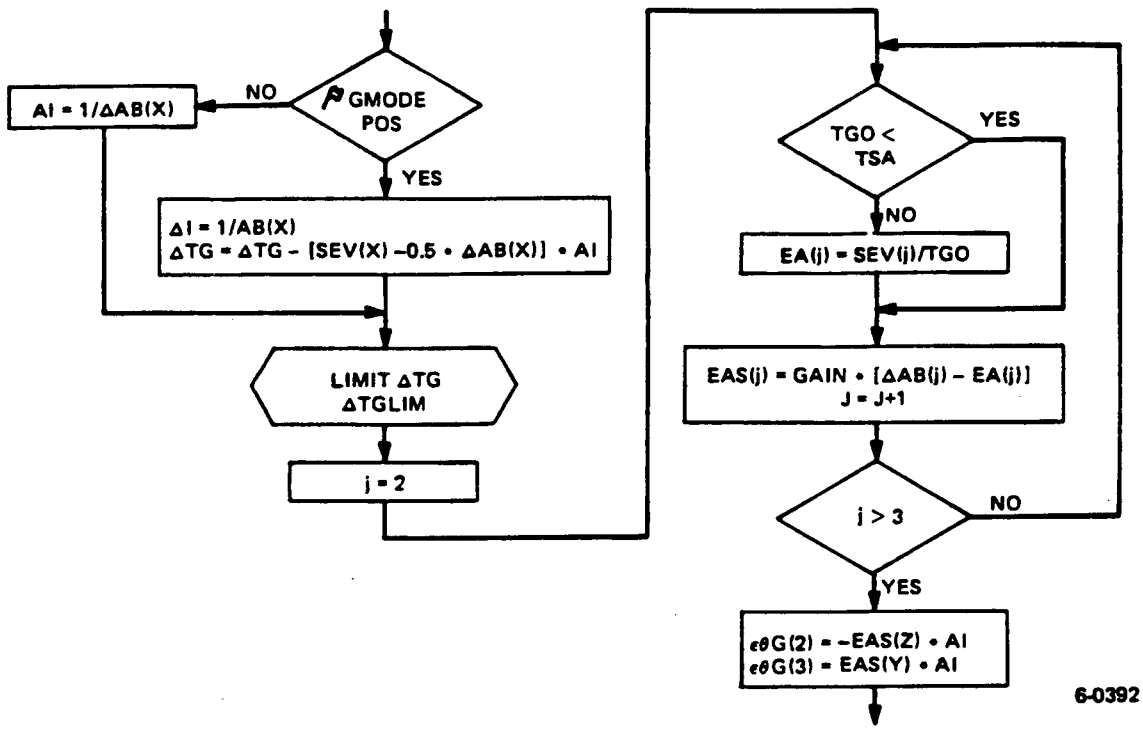

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4.12.3.4.3 Guidance Initialize (TBD)

4.12.3.4.4 Sequencer Subroutine

The sequencer subroutine is used to provide the time dependent sequences to complete the mission after commanded separation from the Titan II booster. It provides for programmed rates, programmed discretes, and programmed control system configuration changes. The detailed flow and logic processing for this subroutine is shown in Figure 4.12.3-29; the data formats for sequencer data arrays are shown in Table 4.12.3-2.

The constants defining these sequences are not an integral part of the flight software, but are included in a separate software package designated as the mission constants. Use of this subroutine is controlled by both the IMU and 2/sec level interrupts.

4.12.3.5 AGS Startup Routine

Program startup is accomplished at Level 9 using the AGSTART routine. The basic logic for this interrupt level is shown in Figure 4.12.3-30.

Immediately upon entry, all external interrupts are disabled to prohibit a higher level interrupt from transferring flow out of this routine before it is completed. Parameters initialized in this area are those required for processing program areas which are exercised prior to reaching the flow into the Initialization routine. The program interrupt vector (location) is assigned within this routine. Prior to exiting the routine, the CPU1 B bus assignment is issued, Level 11 is enabled, and the interrupt quotient register is reset for all interrupt levels.

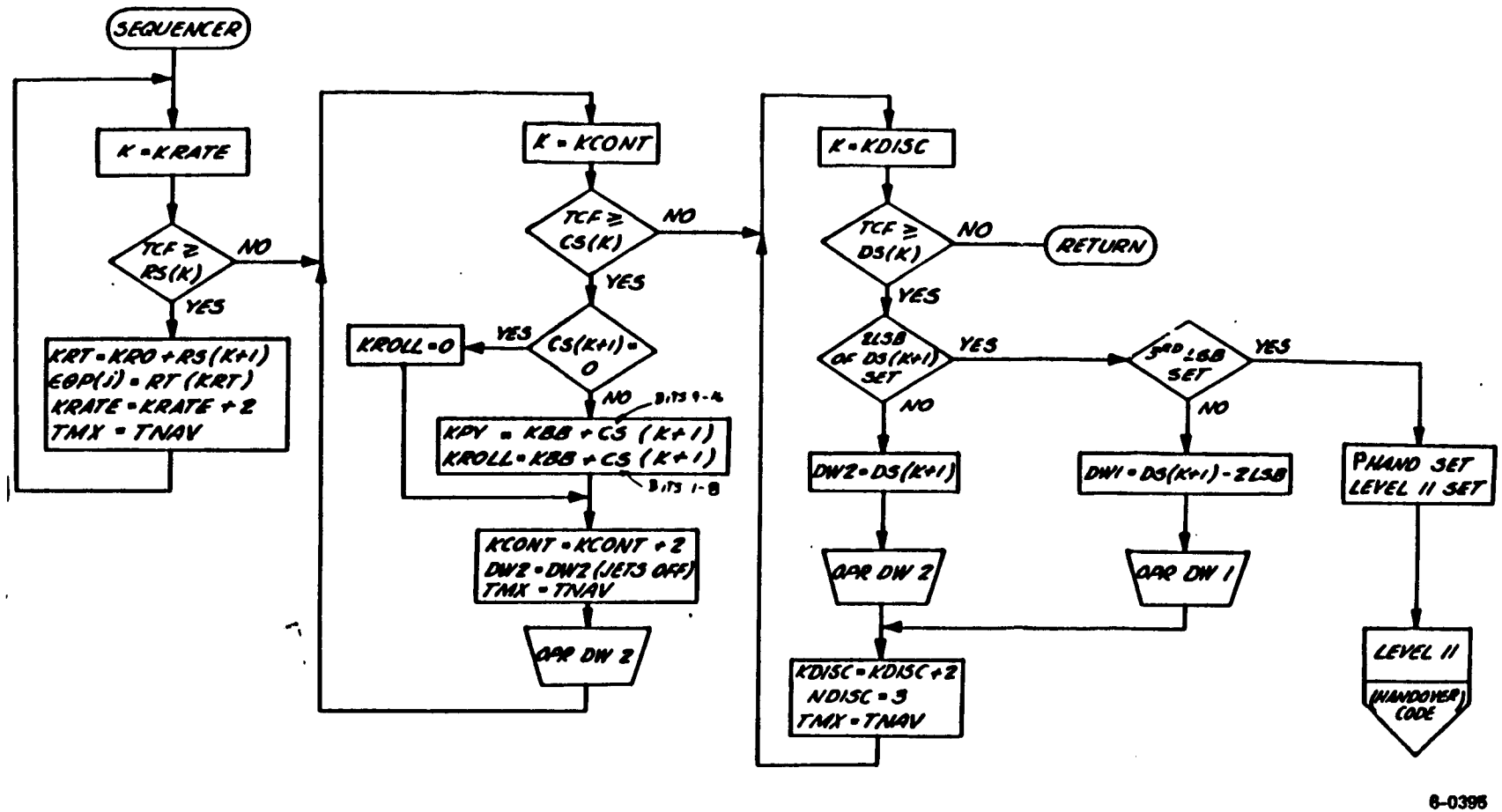

Figure 4.12.3-29. Sequencer Routine Flow Diagram

TABLE 4.12.3-2. SEQUENCER TABLE FORMATS

Table Entry	Parameter	Description			
Rate Sequencer RS(K)		CW Bit Makeup			
1	Time	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16
2	CW	Roll	Pitch	Yaw	Not Used
.		Additive Pointer Address to Locate PGM Rate			
.					
Discrete Sequencer Table DS(K)		Discrete Word Identification			
1	Time	Bits 14, 15 and 16 Set	011 DW1		
2	Discrete Word 1		000 DW2		
			111 Set Level 11		
.					
.					
Controls Sequencer Table CS(K)		CW Bit Makeup			
1	Time	1 2 3 4 5 6 7 8		9 10 11 12 13 14 15 16	
2	CW	Roll		Pitch/Yaw	
.		Additive Pointer Address to Locate BB Coefficients			
.					
All tables are variable length; first entry is located by a table pointer.					

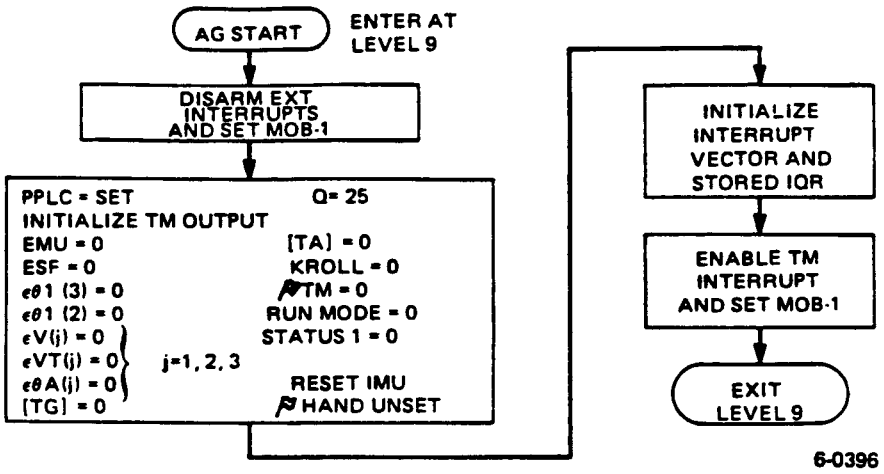

Figure 4.12.3-30. AGS Start Up Logic

4.12.4 TELEMETRY (TBD)

A detailed discussion of ascent phase or boost mode telemetry will not be available until after the AGS PDR/CDR with MDAC.

TABLE 4.12.4-1. AGS TELEMETRY PARAMETERS (TBD)

There are TBD discrete words in the telemetry output stream. In order, these are:

Word	Name
29	Vehicle Discrete 1
30	Vehicle Discrete 2

The contents and format of each of these words is shown in Tables 4.12.4-2 and 4.12.4-3.

Frame synchronization is provided by words TBD and TBD. These words always have the hexadecimal values EB90 and 146F, respectively.

TABLE 4.12.4-2. VEHICLE DISCRETE 1 (WORD 29) TELEMETRY BIT ASSIGNMENTS (TBD)

TABLE 4.12.4-3. VEHICLE DISCRETE 2 (WORD 30) TELEMETRY BIT ASSIGNMENTS (TBD)

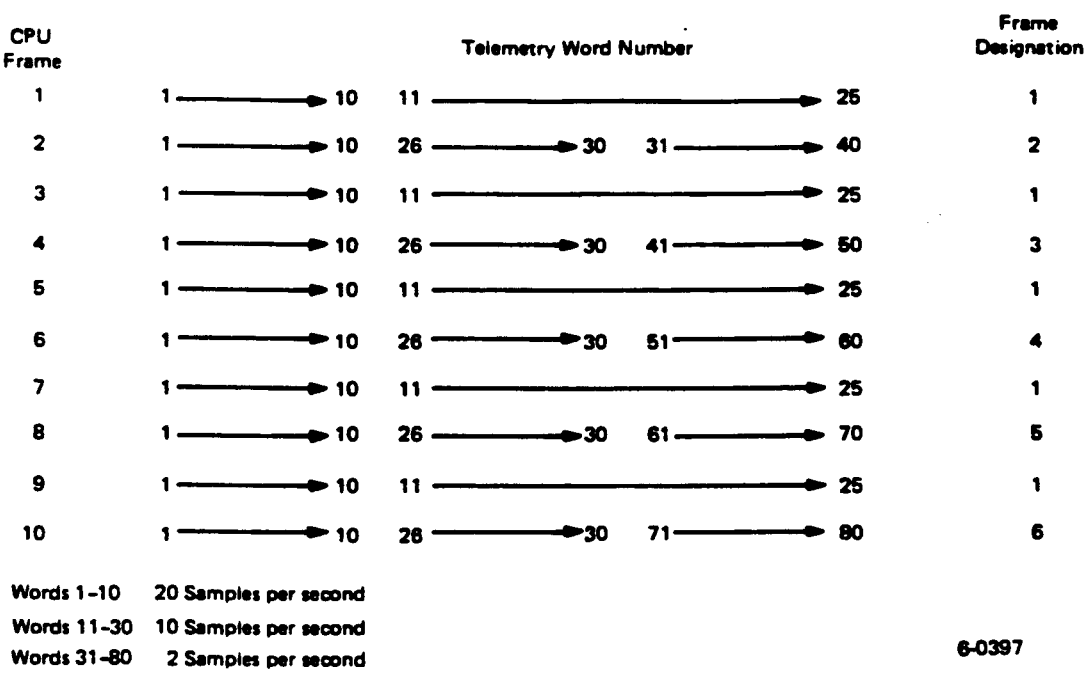

Figure 4.12.4-1. Ascent Guidance Telemetry Master Frame Format

4.12.4 TELEMETRY (TBD)

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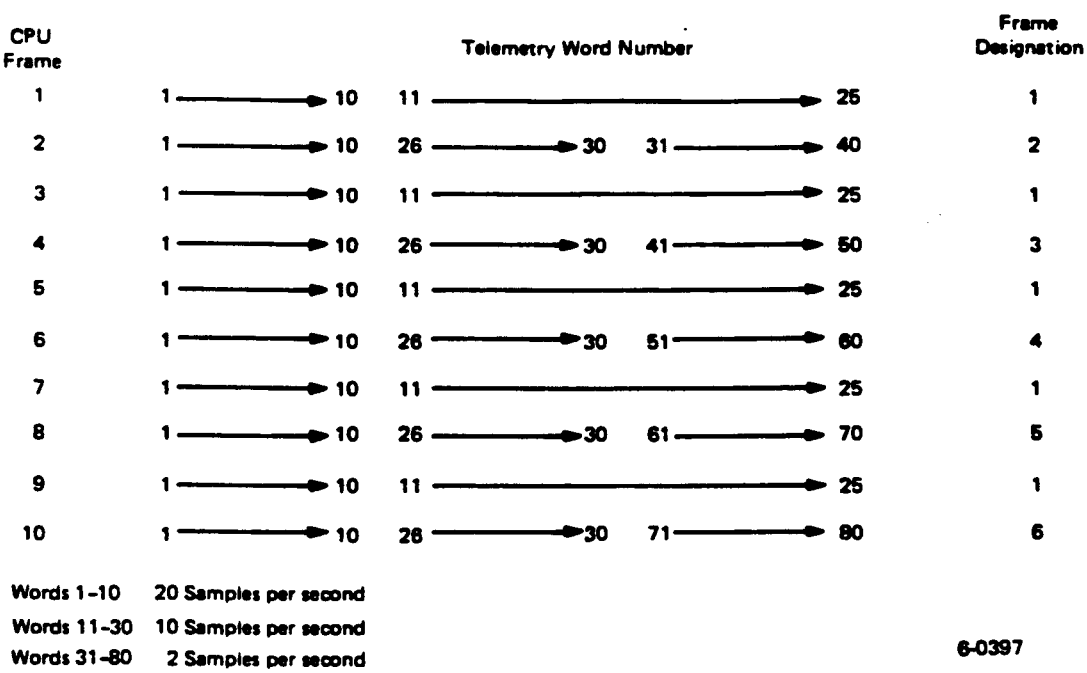

Figure 4.12.4-1. Ascent Guidance Telemetry Master Frame Format

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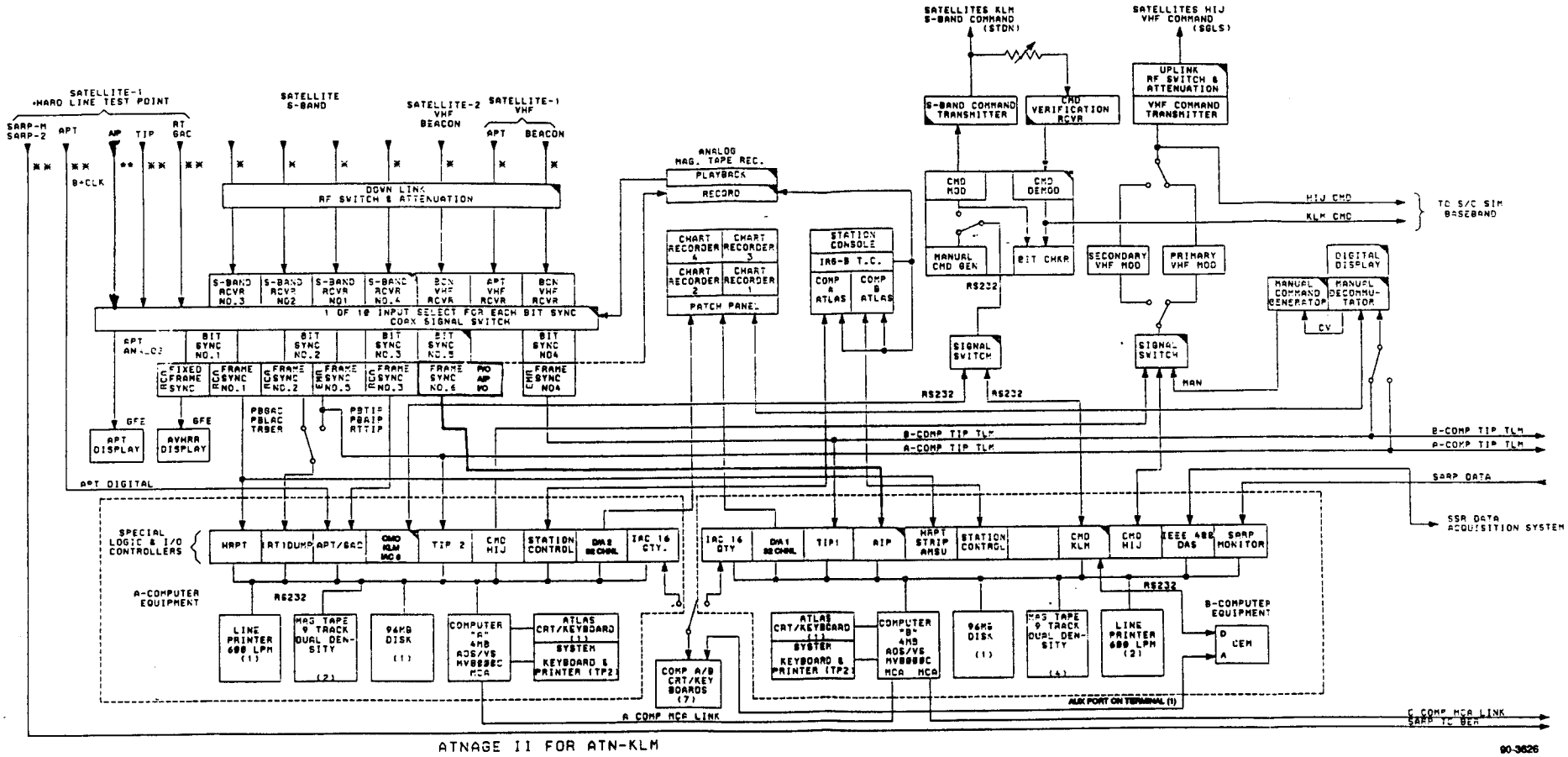


ATNAGE II FOR ATN-KLM

90-3626

NOTES:
1. BLOCK DESIGNATIONS

MODIFY/NEW EXISTING

3. * DENOTES RF LINK, SWITCH SELECTABLE BETWEEN SATELLITE AND SATELLITE SIMULATOR

4. * * DENOTES BASEBAND INTERFACE, SWITCH SELECTABLE BETWEEN SATELLITE SSR AND SATELLITE SIMULATOR

Figure 5.2.1-1a. ATNAGE II Hardware Configuration (Part A): ATNAGE II For ATN-KLM

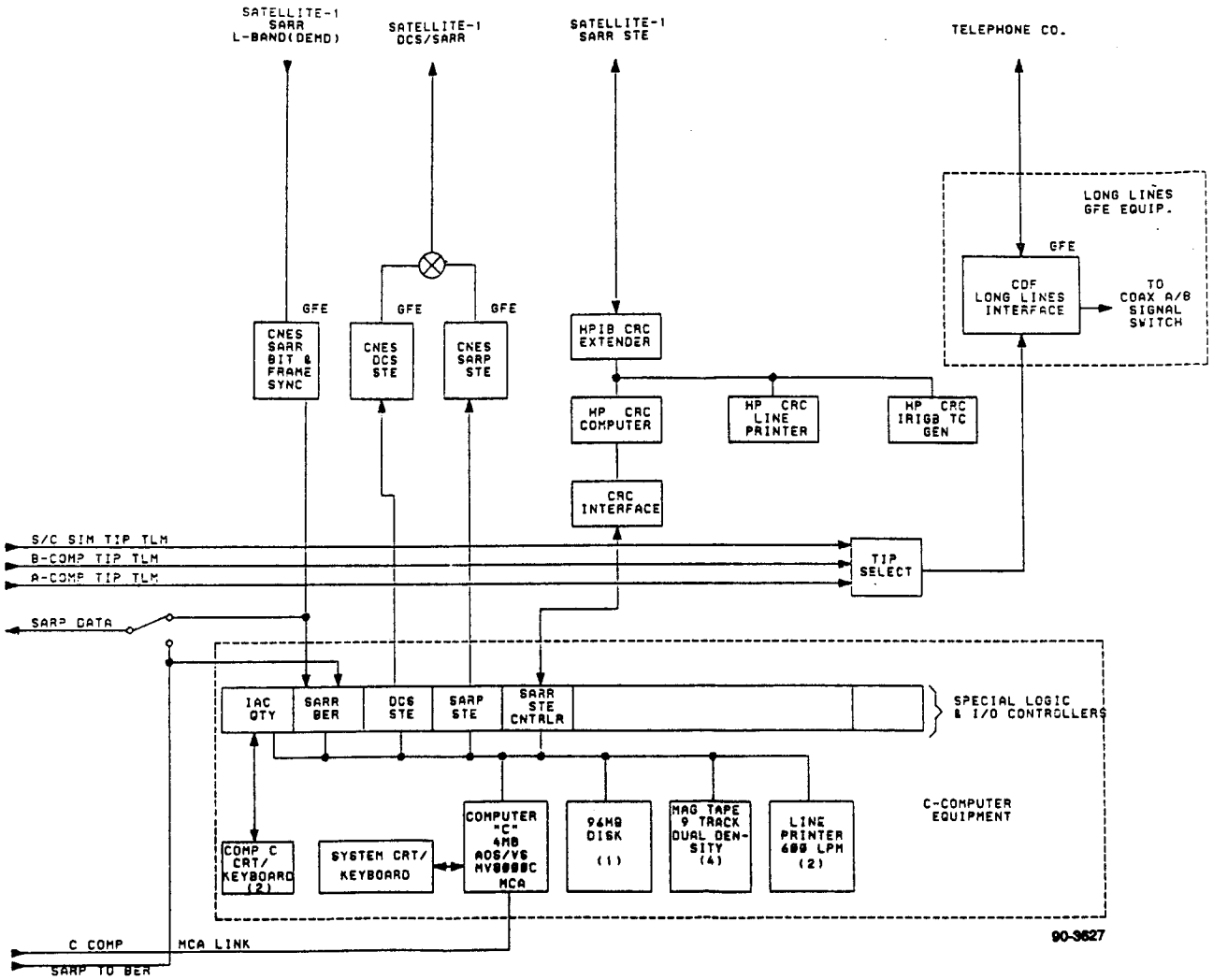
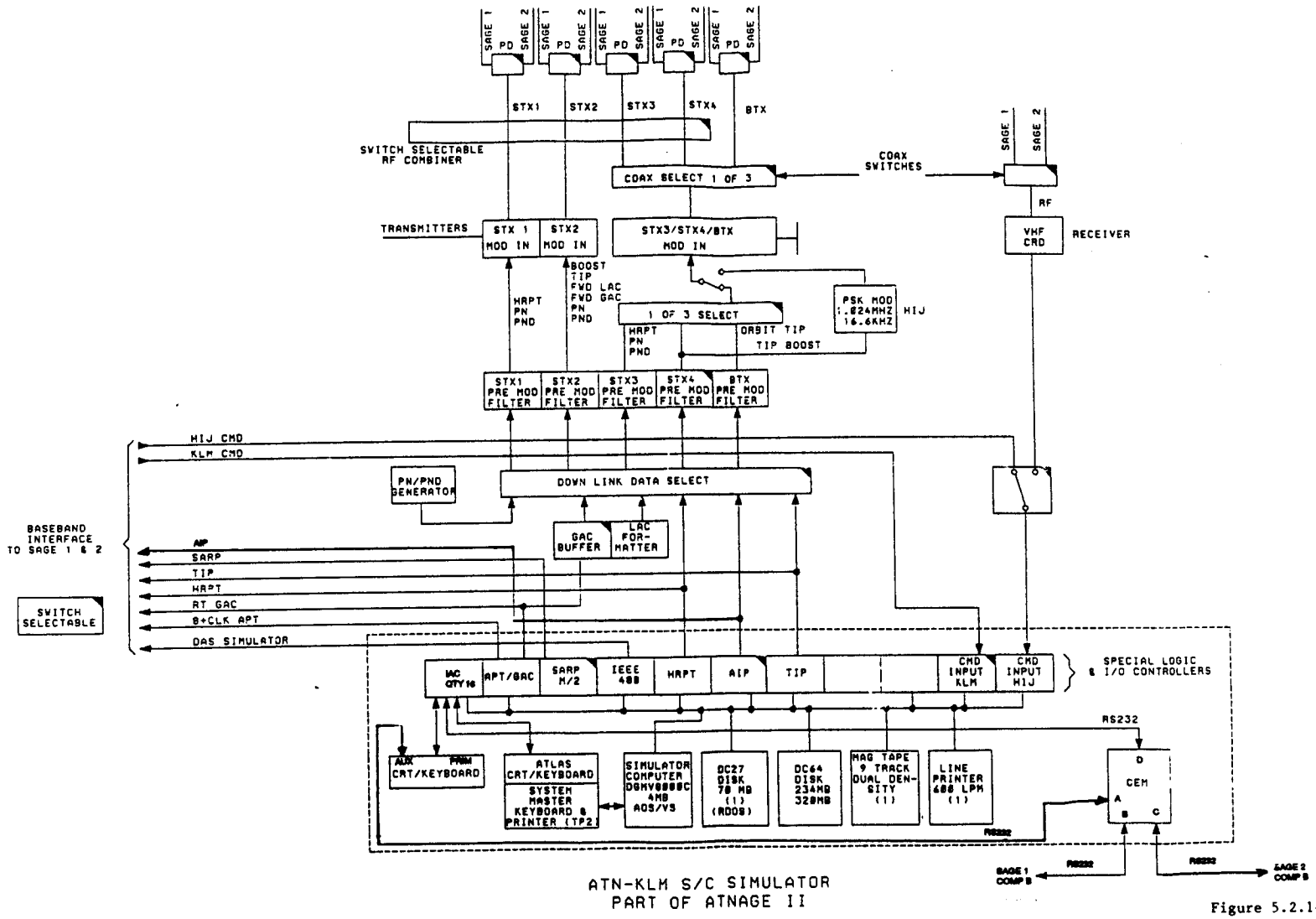


Figure 5.2.1-1b. ATNAGE II Hardware Configuration (Part B): ATNAGE II For ATN-KLM



ATN-KLM S/C SIMULATOR
PART OF ATNAGE II

Figure 5.2.1-1c. ATNAGE II Hardware Configuration (Part C): ATNAGE II For ATN-KLM

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SECTION 5.0

ADVANCED TIROS-N AEROSPACE GROUND EQUIPMENT (ATNAGE)

5.1 GENERAL ATNAGE ARCHITECTURE

The Advanced TIROS-N AGE hardware system comprises two identical stationary AGE (Aerospace Ground Equipment) stations, two identical spacecraft support racks, one AVHRR video display, two APT video displays, and Ordnance Support Equipment. Each stationary AGE station is nominally non-mobile, and provides the capability to test one fully-integrated ATN spacecraft (Bus plus all Payload) on a stand-alone basis . Each of the mobile spacecraft support racks is designed to operate in close proximity to a spacecraft in all test phases and provides for the control and monitoring of spacecraft power, simulators, stimuli, and special test functions. The Ordnance support equipment are portable units capable of interfacing directly with a spacecraft in launch configuration in order to support test operations at the launch site. DCS/ SARP-2, SARR STE's and all video displays are GFE.

5.2 ATNAGE EQUIPMENT GROUPS

5.2.1 STATIONARY AGE (SAGE)

The ATNAGE system includes two independent computer-based modular test stations having the functional configuration shown in Figures 5.2.1-1a, 5.2.1-1b, and 5.2.1-1c. Each of the test stations has the capability of testing a fully configured ATN spacecraft under control of automated test routines or an operator. One of the two test stations (SAGE 1) has the capability to provide back-up command and telemetry processing in support of launch operations.

The SAGE provides the following basic functional capabilities:

(a) All beacon telemetry (TIP) data from a powered spacecraft are continuously processed and evaluated for anomalies whether or not an active spacecraft test is in progress.

(b) A continuous record of all received telemetry, command (CMD) transmission and verification, telemetry anomalies, test results, and any other significant events is generated. A complete recoverable record is generated on IBM-compatible digital tape, and the latest 60 minute (minimum) segment of this record retained in an on-line data store.

(c) For a fully integrated spacecraft, the capability to simultaneously process, in real-time, all low-rate instrument data plus global (GAC) and high resolution video (HRPT) data or data from one spacecraft tape recorder or digital APT dump (real-time dump). For a dual spacecraft recorder dump, the capability exists to sort, then retrieve and process data from the second recorder in non-real time (playback dump).

(d) The capability to bulk-transfer, in real-time, either to or from an "intelligent" external device via a synchronous 9600 buad modem interface.

(e) The capability to transfer, in real-time, DCS and SARP-2 message control data to DCS/SARP-2 Special Test Equipment via a RS-232 serial interface.

(f) Thirty-two standard (40 Hz) analog strip chart recorder channels are provided for test data recording; all channels are accessible from Computer B during a fully-integrated spacecraft test.

(g) The capability to monitor Automatic Picture Transmission (APT) data in real-time via an APT video display; computer processing of analog APT data is not provided.

(h) The capability to continuously monitor advanced high Resolution Radiometer (AVHRR) data in real-time on an AVHRR video display.

(i) The capability to continuously process <u>either</u> APT data <u>or</u> Global Area Coverage (GAC/APT) data supplied digitally via hard-wire test points by the spacecraft (simultaneous processing of APT and GAC data is not provided). The selection of either APT or GAC data for processing is under software program control.

(j) The capability to manually generate, transmit, and verify spacecraft command messages in clear mode.

(k) The capability to decommutate and display up to 8 analog and 8 digital spacecraft telemetry channels under manual control.

(l) The capability to encrypt and decrypt (NSA KI-23 EMS) command and up-link messages via a command encryption module (CEM).

(m) The capability to receive and process AIP real-time data.

(n) The capability to receive and process AIP tape recorded play back data.

(p) The capability to extract and process, from the HRPT data stream, AMSU and TIP instrument data.

5.2.1.1 Computers

Each of the two SAGE computer systems consists of three Data General Corporation Eclipse MV/8000C with 4 MBytes of solid state memory. The characteristics of the basic Eclipse MV/8000C computer are:

- Microprogrammed architecture
- Pipelined instruction processor
- Comprehensive 16 and 32-bit instruction sets
- 16 KByte Cache memory
- Continuous memory error checking and correction
- Powerful hardware-interrupt servicing
- Compatible operating systems and high-level languages
- Operator console program debugging

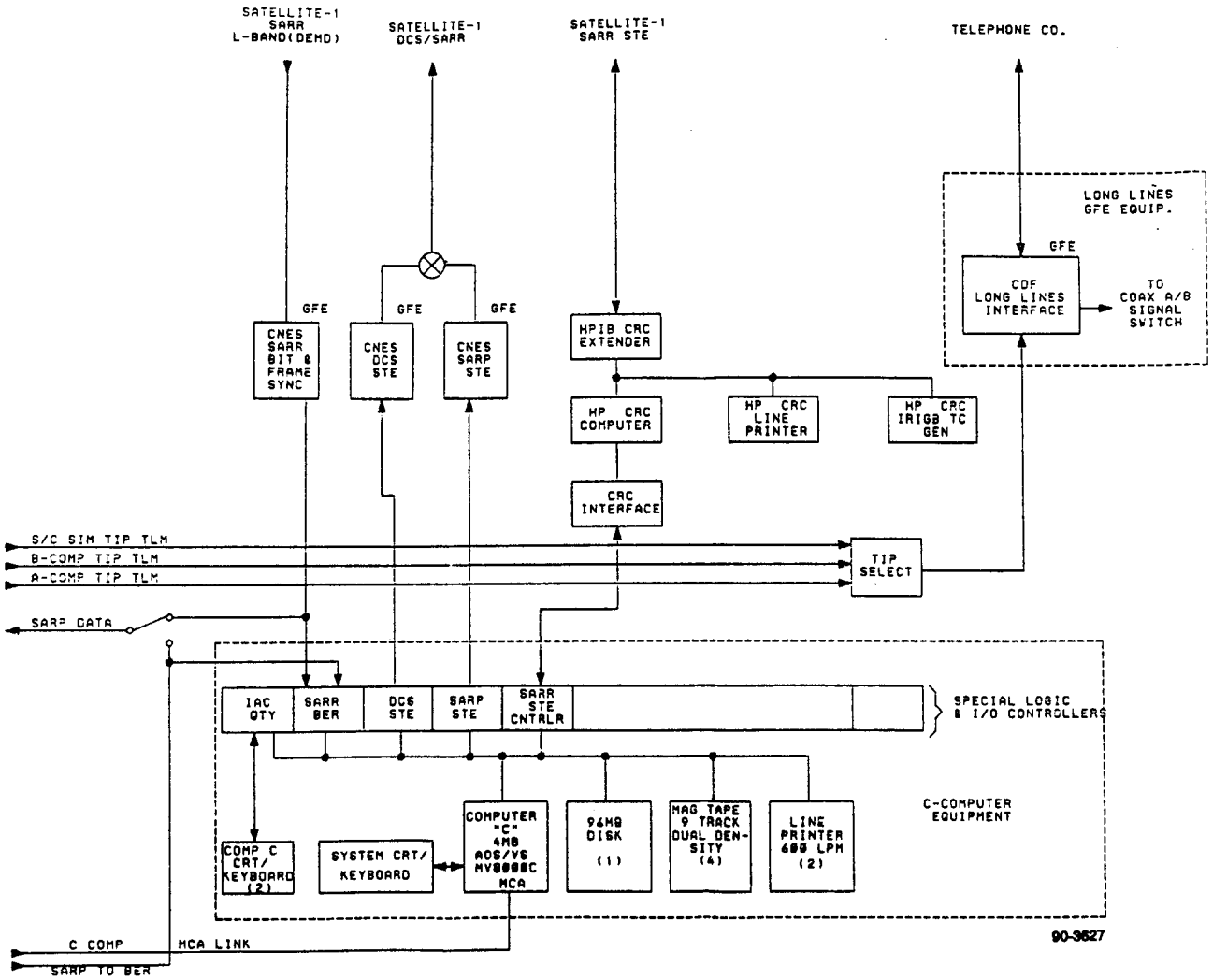
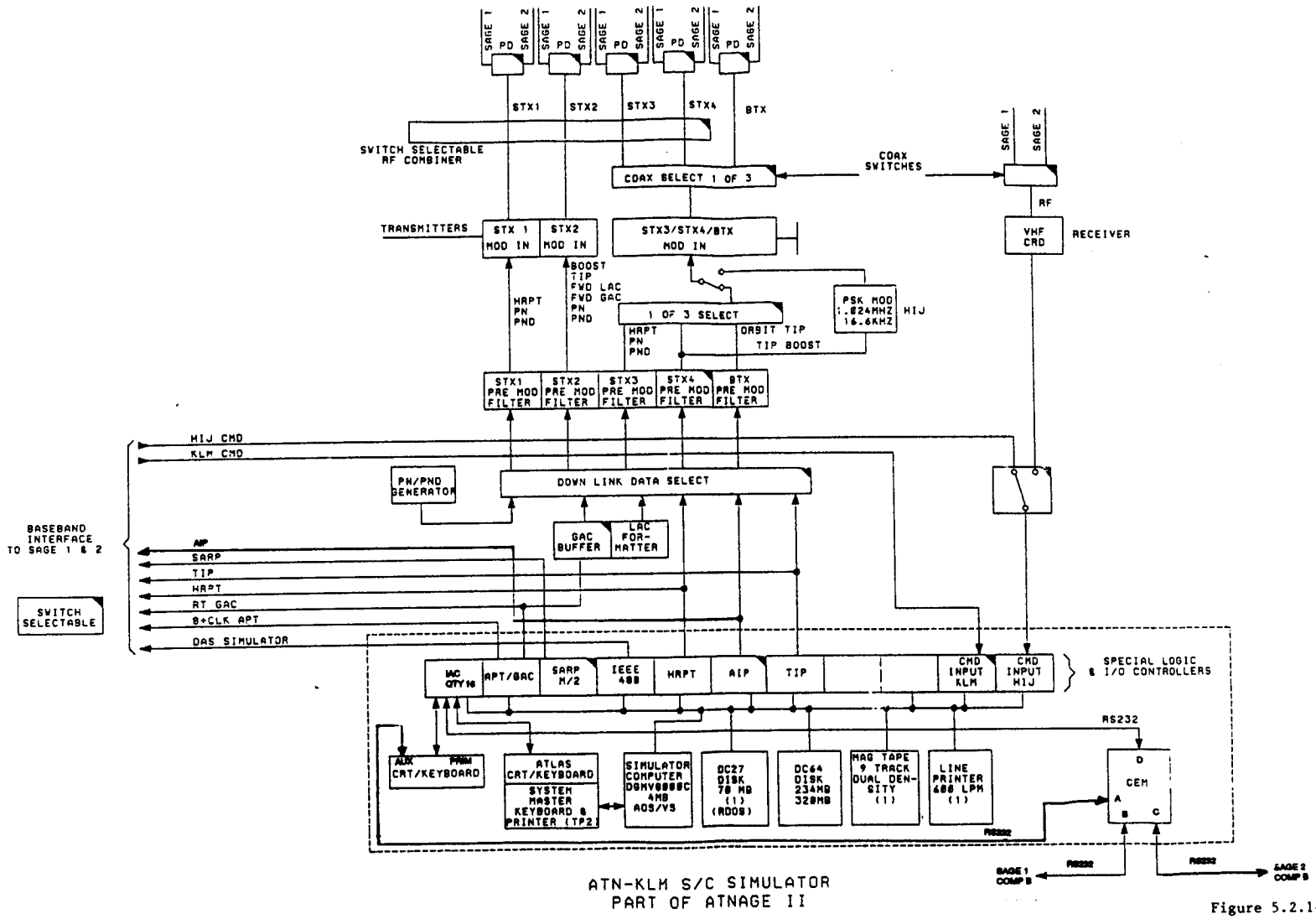


Figure 5.2.1-1b. ATNAGE II Hardware Configuration (Part B): ATNAGE II For ATN-KLM



ATN-KLM S/C SIMULATOR
PART OF ATNAGE II

Figure 5.2.1-1c. ATNAGE II Hardware Configuration (Part C): ATNAGE II For ATN-KLM

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- Data channel rates: 2.27 MBytes/seconds; 1.29 MBytes/second output
- Burst MPX rates: 16.16 MBytes/second input; 14.54 MBytes/second output
- I/O System: 53 devices addressable; 16 priority interrupt levels
- Real-time clock
- Thermal cutout switch

A Data General floating point processor, Model 8704, is also used with the ECLIPSE MV/8000C computer. This unit features:

- 64-bit floating point accumulators
- Ultra-high-speed, floating point arithmetic
- Operation parallel with central processor
- Single- and double-precision arithmetic
- Comprehensive single- and double-word instruction set
- High-level language support

5.2.1.2 Nine-Track Tape Recorders

Each station has nine Model 6026A nine-track 1600/800 bpi dual density tape recorder.

Features of the Model 6026/6026A, nine-track, 800/1600 bpi tape recorder system are:

- 1600 bpi phase encoded or 800 bpi NRZI .
- Transfer rate of 120K bytes per second at 1600 bpi and 60K bytes at 800 bpi
- 75 ips tape speed
- 40 Mbytes capacity at 1600 bpi and 2400 ft. tape
- Self-loading vacuum column
- 200 ips rewind speed
- Microprocessor based controller
- Single capstan drive
- Industry compatible nine-track system
- Up to 10 1/2" reel size
- Read-after-write checking
- Write and read de-skewing
- Microprocessor controlled read threshold
- Supported by AOS software

5.2.1.3 Alpha-Numeric Display Terminals

The primary operator interface is through Data General Model 6347 and 6501A CRT-display/ keyboard terminals. Ten such terminals are provided. One terminal is used for operator interface and the other(s) for general data display in all test configurations.

5.2.1.4 Line Printers

Each SAGE test station has three Data General Model 5040A (upper case only) line printers, each of which operates at 600 lines per minute. The line

printers are distributed as follows: one with Computer A, one with Computer B, and one with Computer C. A fourth line printer, Data General Model E4596, with upper and lower case character sets is dedicated to the B computer and is required for AOS/VS software development. The print rate of the Model E4596 is also 600 lines per minute. Each printer can handle, in real-time, ten test events per second with an event formatted as one line of data. This corresponds to one event per minor frame of TIP data, on the average. Test events occurring more frequently are stored for later playback. The second line printer, connected to Computer B, is used for general data printouts under operator or ATLAS control.

5.2.1.5 Multiprocessor Communications Adapter

Each of the two SAGE's employs a Data General 4206 Multiprocessor Communications Adapter (MCA) which provides interprocessor communications between the three SAGE computers. It has independent interfaces which permits simultaneous transmission and reception of blocks of data using the DMA channel. Characteristics of data transmission are established by convention in the software.

Significant characteristics of the MCA are:

- Maximum transfer rate 1 Mbyte per second
- Maximum distance between all computers on MCA link -- 45 meters
- Two MCA links maximum on any computer

5.2.1.6 Time Code Reader/Generator

A Systron-Donner Model 8155 Time Code Reader/Generator is used to inject time code information into the computer software. The external input to the time code reader can be a standard IRIG 36-bit serial time code signal. One unit is connected to each SAGE computer. The time code reader is interfaced to the processor via a Data General Model 5535C Interface Unit.

The IRIG time code is used to periodically update the Data General real-time clock. Thus, even if the IRIG time code source fails for a short period of time, the processors will still have timing information. However, there will be an accumulated timing error until the time code reader can update the real-time clock.

5.2.1.7 Moving Head Disk

Primary storage for each of the SAGE computers is provided by a 96-million bytes moving head disk drive. Each disk drive is a Data General Model B6060H, interfaced to the computer through a Model B6060 controller. Each controller handles one master disk drive and up to three additional slave drives. Features of the Model B6060 moving head disc pack drives are:

- 95.956 million bytes capacity per drive
- 806,000 bytes per second transfer rate
- Average access of 43.3 ms.

- Storage format: 19 surfaces, 411 tracks per surface, 24 sectors per track, 512 bytes

- Full RDOS and AOS support

- Dual-port access

5.2.1.8 Digital-to-Analog System

The digital-to-analog system drives the multichannel chart recorders used for evaluation. It includes D/A converters for driving up to 32 chart recorder channels from the B computer. On SAGE 1 only the 32 DIA channels may be driven from the A computer through a patch cable network.

The D/A system is a Data General unit, and includes the following:

- Four Model 4056 A/H I/O system interface units, each of which supports up to 24 D/A converters. Two are resident in Computer B and two are resident in Computer A.

- 32 Model 4056D 12-bit D/A converters, (16 per I/O system), are dedicated to the B computer to drive 32 strip chart recorder channels. The 32 DIA converters may be patched to the A computer when the A computer is used as a command and telemetry back-up during launch support.

5.2.1.9 Strip Chart Recorders

Four strip chart recorders are associated with each SAGE. They are standard eight-channel brush recorders, using ink for writing. In addition, each standard eight-channel recorder has two digital channels. The standard chart recorder will handle most signals up to approximately 55 Hz.

The standard eight-channel recorder is a Gould, Brush Model 200, having the following features:

- 8 channels, 40 mm full scale/channel

- two-event (digital) channels on left and right margins. Additional seven-event channel option available.

- Horizontal readout in low-boy cabinet

- Pressurized fluid marking system

- Trace width, 0.01 inch

- Frequency response: full scale (40 mm) at 55 Hz, 50% response at 80 Hz, 20% response at 140 Hz.

- Chart speed ratio 4000:1, 0.05 mm per second to 200 mm per second.

5.2.1.10 Printing Terminals

Dasher TP2 Printing Terminals are used as the primary off-line system console for the A and B computers.

The Dasher TP2 Printing Terminals have the following features:

- 180 characters per second printing, logic seeking, bidirectional
- 7 x 9 impact dot matrix characters
- Typewriter-style keyboard with 14-key numeric pad
- 20 MA current loop and EIA interfaces
- Normal, elongated, condensed and condensed/elongated character printing

5.2.2 SPACECRAFT SIMULATOR

The ATNAGE includes a spacecraft simulator capable of responding to spacecraft commands from the ATNAGE systems and generating simulated spacecraft telemetry and instrument data streams suitable for AGE checkout and self-test. The spacecraft simulator is a modular unit based on a Data General MV/8000C computer with four Mbytes of solid state memory and a Model 6160 73 Mbyte Winchester disc storage system, with a second disc system (Model 6446M).

5.2.3 SPACECRAFT SUPPORT RACKS

The Spacecraft Support Rack (SSR) includes the hardware required to turn on the spacecraft, to provide a source of ground power and to provide protection against out of limits power and temperatures. The SSR can provide power to the spacecraft in the internal mode (using the spacecraft batteries as a source of power), in the external mode or in a solar array input mode. A number of hard wire test inputs are monitored and limit checked to provide for immediate shut-down in the event of a critical out of limits condition or alarms if a less hazardous condition is detected. Some test point data is conditioned and powered for transmission to the computer room for processing. The SSR includes a Data Acquisition System which can, under SAGE control, scan some 300 analog test signals, digitize the voltage level of the selected signal and transmit it to the SAGE system for processing. The operation of the SSR, except for the DAS, is under manual control. Figure 5.2.3-1 shows the SSR functional configuration.

5.3 DISPLAYS

5.3.1 HRPT DISPLAY

The HRPT display with its associated buffer is government furnished equipment. It is a Harris Laserfax (Model 500) display and RCA buffer, which is a low-cost unit that requires no chemicals or separate processing facility, uses roll paper, and outputs a 10.5 x 16.5 inch format image on dry silver paper within 1 minute after receipt of a data "frame." The dry paper system has a dynamic density range of 0.2 to 1.5. The horizontal resolution is 2482 TV lines (50 percent response), with a line advance rate of 1.35 inches per minute. The unit incorporates a plug-in laser source, optics, electronics, and processor.

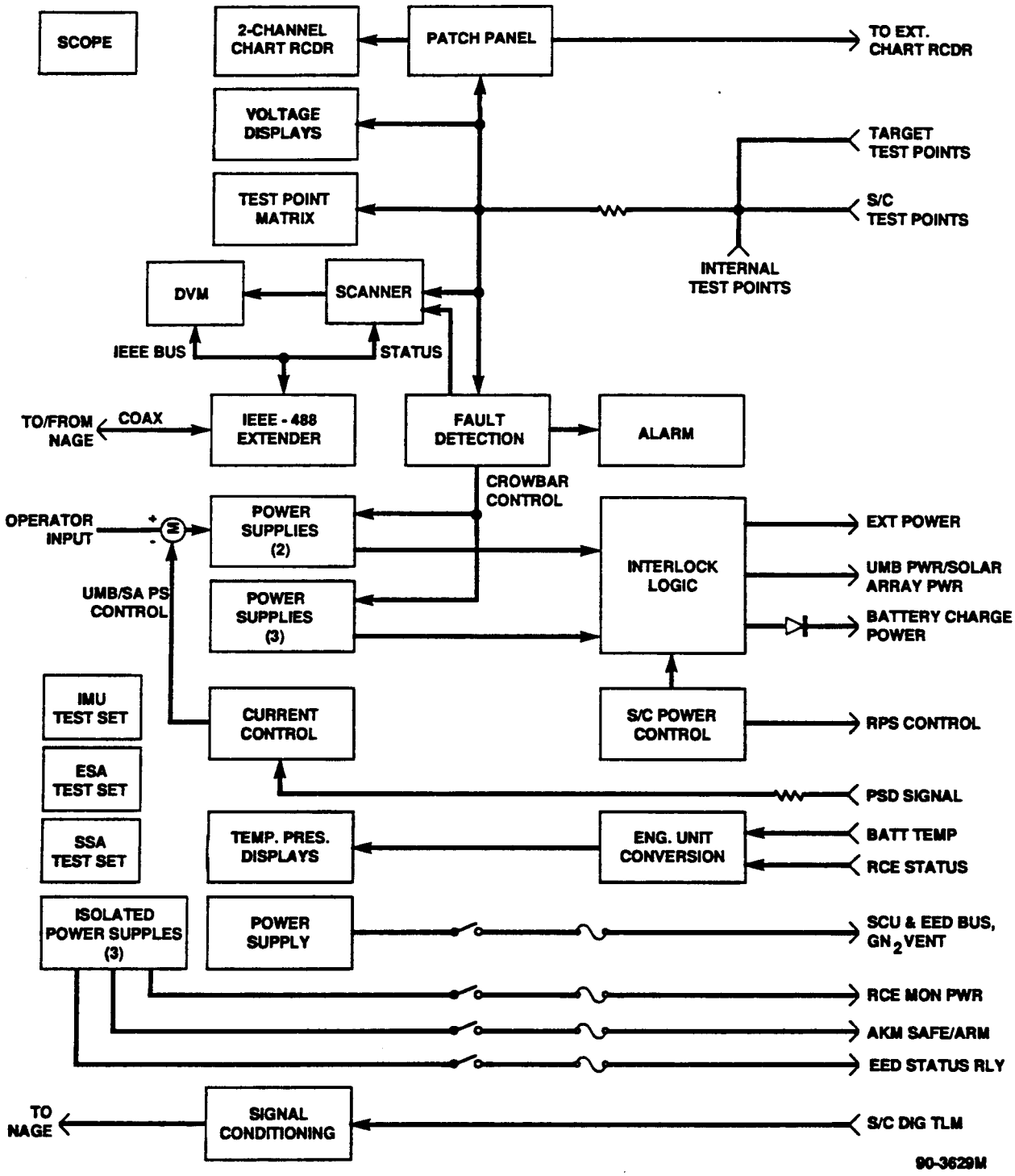

Figure 5.2.3-1. Spacecraft Support Rack (SSR) Functional Configuration

5.3.2 APT DISPLAY

The government supplies an APT display for producing hard copy of the APT signal transmitted from the spacecraft. The input to this unit is the standard analog APT signal, which consists of the baseband signal on a 2.4-kHz subcarrier, along with the appropriate line synchronization information. This unit is a facsimile unit similar to the HRPT display.

5.4 ATNAGE INTERFACES

5.4.1 SPACECRAFT POWER

The ATNAGE provides the following capabilities to supply, control, and monitor spacecraft power:

(a) A Ground Power Switch (GPS) unit provides remote control for turn-on of spacecraft power in either internal or external power mode. It is bracket mounted to the spacecraft to minimize IR losses in the internal mode of non-flight operation. The GPS connects either the spacecraft battery or the External Power supply to the spacecraft load.

(b) Programmable power supplies provide primary spacecraft power in either of two modes:

External Spacecraft Power. In this mode one power supply operates as a programmable voltage source of +15 to +28 volts with a current capability of 30 amps. Hardware overvoltage protection limits the maximum voltage at the spacecraft interface to +26 volts.

Solar Array Simulator. In this mode, another power supply delivers to the spacecraft power which is controlled by the partial shunt drive control voltage. This closed loop arrangement does not simulate the solar arrays completely since frequency responses, etc. are not identical, but all control circuitry is exercised.

(1) The maximum simulated array current at 0 volts (short circuit current) is manually adjustable over the range 0 amperes to 70 amperes, and is automatically reduced in a linear fashion from 70 amperes (or less) to 0 amperes in response to a partial shunt drive signal from the spacecraft which has a maximum drive capability of 59 mA at 14 volts with respect to the simulated solar array negative (return).

(2) The equivalent maximum simulated array voltage at 0 amperes (open circuit voltage) is manually adjustable over the range 28 volts to 40 volts. The actual output voltage of the Solar Array Simulator is limited to 36 volts when connected to the spacecraft.

(3) A manual switch at the operator's control panel provides immediate spacecraft power turn-off in any power mode.

5.4.2 SPACECRAFT RADIO FREQUENCY

The characteristics of the RF interfaces with the spacecraft are as follows in Tables 5.4.2-1, 5.4.2-2 and 5.4.2-3.

TABLE 5.4.2-1. DOWNLINK PCM DATA

PARAMETER	S-BAND	VHF BEACON
Center Frequency	1695-1707,2247.5 MHz	137.35 or 137.77 MHz
Freq. Stability	$\pm 2 \times 10^{-5}$	$\pm 2 \times 10^{-5}$
Xmtr Power	+38 dbm (1695-1707) +34 (2247.5)	+33 dbm
Carrier Modulation	Phase	Phase
Spectrum	3 MHz	400 kHz
Modulation Index	67 deg pk. (max)	67 deg pk. (max)
Data Rate	16.64 to 2662 KB/S	8.32 KB/S

TABLE 5.4.2-2. APT DOWNLINK

PARAMETER	VALUE
Center Frequency	137.50 and 137.62 MHz
Frequency Stability	$\pm 2 \times 10^{-5}$
Xmtr Power	+35 dbm
Carrier Modulation	FM, $\pm$17 kHz pk
Spectrum	40 kHz
Subcarrier Frequency	2.4 kHz
Subcarrier Modulation	AM-DSB
Subcarrier Mod Index	92% (max.)

TABLE 5.4.2-3. COMMAND UPLINK:

PARAMETER	VALUE
Frequency	2025.0 MHz
Frequency Stability	±.003%
Signal Level at spacecraft	-35 to -75 dbm
Carrier Modulation Index	1.0 ±./Radian, Peak
Subcarrier Modulation	PM/BPSK
Subcarrier Frequency	16,000 Hz (.002%)
Data Rate	2000 BPS

5.4.2.1 Analog Data Storage

The ATNAGE provides the capability of tape recording all data streams received from the spacecraft. In addition to a standard time code signal, each test station includes one wideband Honeywell Model 96 instrumentation recorder. The wideband recorder shall provide selective recording of the high data rates on demand and playback at real time or reduced rate for processing as shown in Figure 5.4.2-1. This recorder provides at least 15 minutes of recording of the highest rate signals (2.66 Mb/s) at a tape speed of 120 inches per second.

5.4.2.2 Uplink Data Generation and Verification

The S-band Spaceflight Tracking and Data Network (STDN) uplink is used for the command and CPU memory loads to the KLM spacecraft. As per STDN specifications, the uplink will consist of 32-bit data words at 2 Kbs, BPSK-modulated on a 16 kHz subcarrier. See Figure 5.4.2-2. This subcarrier is phase modulated on a RF carrier centered at 2025.0 MHz.

5.4.2.2.1 Command Generator

The command generator creates all of the acceptable spacecraft commands internally (local mode), accepting any commands from a host computer (remote mode), or accepting a serial command data stream from an external source.

The command generator shall provide 16 kHz phase shift keyed modulated commands for transmission to the spacecraft. The command generator provides baseband (NRZ-M) commands and clock to the spacecraft simulator.

5.4.2.2.2 Verification

Normal command verification is accomplished by software processing of the CV message contained in the TIP telemetry.

		RECORD (ips)	PLAYBACK (ips)
DUMP 1*	1	120	120, 30, 7-1/2
DUMP 2*	2	120	120, 30, 7-1/2
HRPT RT	3	120, 30	120, 30, 7-1/2
APT	4	120, 30, 7-1/2	120, 30, 7-1/2
GAC TP	5	120, 30	120, 30, 7-1/2
TIP RT	6	120, 30, 7-1/2	120, 30, 7-1/2
AIP RT	7	120, 30, 7-1/2	120, 30, 7-1/2
TIME CODE	8	120, 30, 7-1/2	120, 30, 7-1/2

*May be either 2.66, 1.33, or 0.332 MB/S.

Figure 5.4.2-1. Analog Data Record/Playback Configuration

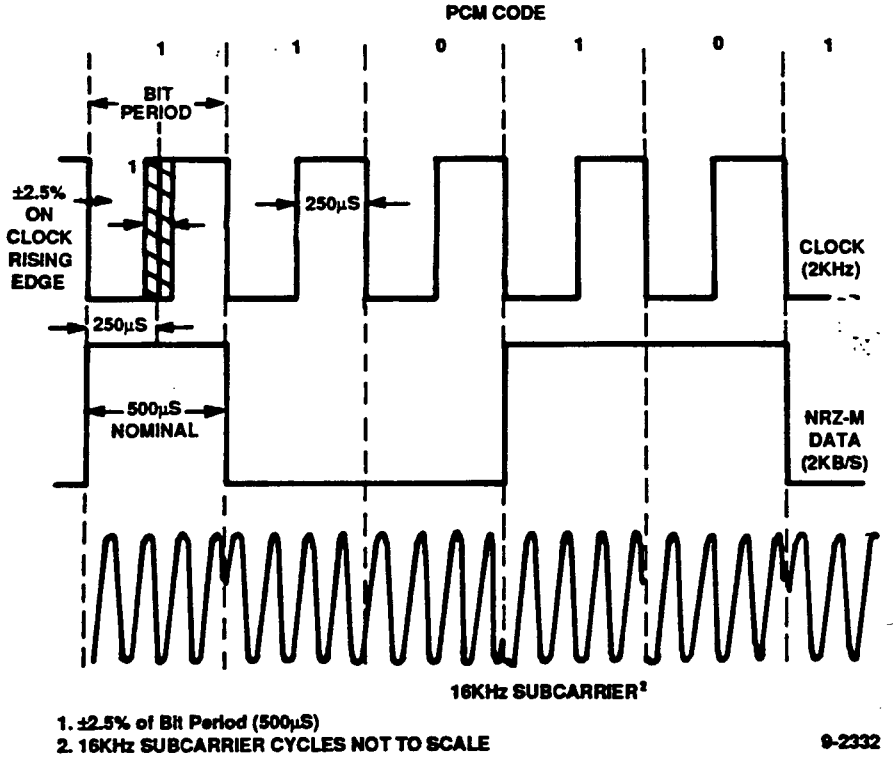

Figure 5.4.2-2. Uplink Data Modulation Format

5.4.2.3 Downlink Data Acquisition and Display

The ATNAGE provides simultaneous acquisition of real time TIP telemetry, AIP, APT data, and up to 4 high rate PCM data streams (3 S-Band +1 hardwire GAC/APT). The characteristics of the signals are as follows in Tables 5.4.2-4, 5.4.2-5, 5.4.2-6, 5.4.2-7, 5.4.2-8 and 5.4.2-9.

TABLE 5.4.2-4. REAL-TIME TIP SIGNAL CHARACTERISTICS

PARAMETER	ORBIT MODE	BOOST MODE
LINK	VHF BEACON	S-BAND
BIT RATE	8320 BPS	16640 BPS
CODE	BIPHASE - L	BIPHASE - L
FORMAT	AS SPECIFIED IN GE PS 2284374 SERIAL PCM BIT STREAM, 8-BIT WORDS, MOST SIGNIFICANT BIT FIRST	

TABLE 5.4.2-5. APT SIGNAL CHARACTERISTICS

PARAMETER	ORBIT MODE
LINK	VHF APT
VIDEO BW	2.4 KHz
FORMAT	AS SPECIFIED IN GE PS 2284391 AMPLITUDE MODULATING 2400 Hz SUBCARRIER

TABLE 5.4.2-6. REAL-TIME GAC SIGNAL CHARACTERISTICS

PARAMETER	ORBIT MODE
LINK	HARDWIRE TEST POINT
BIT RATE	66540 BPS
CODE	NRZ - L
FORMAT	AS SPECIFIED IN GE PS 2284391

TABLE 5.4.2-7. REAL-TIME AIP SIGNAL CHARACTERISTICS

PARAMETER	ORBIT MODE
LINK	S-BAND
BIT RATE	16640 BPS
CODE	BIPHASE - L
FORMAT	AS SPECIFIED IN GE PS 2284391

TABLE 5.4.2-8. HRPT (REAL-TIME AVHRR) SIGNAL CHARACTERISTICS

PARAMETER	ORBIT MODE
LINK	S-BAND
BIT RATE	665,400 BPS
CODE	BIPHASE - L
FORMAT	AS SPECIFIED IN GE PS 2284391

TABLE 5.4.2-9. SPACECRAFT RECORDER DUMP (S-BAND LINK) SIGNAL CHARACTERISTICS

DATA	BIT RATE	CODE
ORBIT TIP	332.7 KB/S	BIPHASE - L
GAC and LAC	1.3308 MB/S	BIPHASE - L
	2.6616 MB/S	NRZ - L
AIP	332.7 KB/S	BIPHASE - L
FORMAT	SAME AS REAL, TIME BUT IN REVERSE ORDER	

5.4.2.3.1 Real-Time TIP Processing

The ATNAGE continuously monitors the spacecraft status via the real time AIP data stream received over a hard-line test point and S-band link. The hardware demodulates the received signal, recovers the bit rate clock and frame sync and enters all the data into the computer for processing. The computer controls the synchronization and performs frame decommutation. The received data stream is recorded during testing and it remains possible to process from the recorder playback.

This processing separates the TIP and AMSU data from the AIP stream. The TIP data is then processed and the AMSU data is sent to the computer for processing. The source of AIP HRPT or TIP data streams is selectable by operator.

5.4.2.3.2 High Rate PCM Processing

The ATNAGE includes four Microdyne Model 1100 AR S-band receivers for the recovery of HRPT and spacecraft recorder dump signals. The EMR Model 720 programmable bit synchronizer provides bit reconstruction and clock recovery of any of the possible data streams received via the S-band link; the bit synchronizers are either manually or computer programmable and provide lock status to the computer interface.

Three computer interfaces on the ATNAGE provide for concurrent entry of up to three of the high rate MIRP-generated data streams into the computer via DMA.

Each high rate interface consists of a specially designed frame synchronizer, data selector, and buffer. Each frame synchronizer detects the MIRP 60 bit PN sync code running either forward (real time) or backward (spacecraft recorder dump), derandomizes the data (if required) by extracting the PN sequence inserted by the MIRP, alerts the computer whenever lock is acquired or lost, and accepts either 11,090 word or 3,327 word frames as programmed.

The high rate frame synchronizer acquires lock in a three stage process, progressing from SEARCH to CHECK to LOCK. In SEARCH, the synchronizer continuously monitors the data stream for the presence of the 60 bit sync pattern; upon detection of the exact 60 bit sync pattern, the synchronizer advances to the CHECK mode and checks the 60 bit sync in the next frame. If the number of bit disagreements is less than or equal to N, the synchronizer advances to LOCK mode; if the number of bit disagreements exceeds N, the synchronizer returns to SEARCH. In LOCK mode, the synchronizer continues to check the 60 bit sync pattern. If the number of errors exceeds M, the synchronizer increments a bad frame counter; when the bad frame count equals P, the synchronizer returns to SEARCH. If the number of bit errors in LOCK mode does not exceed M, the bad frame counter is reset to zero. N and M are independently computer programmable over the range of 0 to 63; P is programmable over the range of 1 to 7.

In addition, in the LOCK mode, the number of bit errors in the 1000 bit auxiliary sync pattern is counted and entered into the computer each frame. The number of bit errors in each 1000 bit pattern is also compared to a

5.4.2.3.1 Real-Time TIP Processing

The ATNAGE continuously monitors the spacecraft status via the real time AIP data stream received over a hard-line test point and S-band link. The hardware demodulates the received signal, recovers the bit rate clock and frame sync and enters all the data into the computer for processing. The computer controls the synchronization and performs frame decommutation. The received data stream is recorded during testing and it remains possible to process from the recorder playback.

This processing separates the TIP and AMSU data from the AIP stream. The TIP data is then processed and the AMSU data is sent to the computer for processing. The source of AIP HRPT or TIP data streams is selectable by operator.

5.4.2.3.2 High Rate PCM Processing

The ATNAGE includes four Microdyne Model 1100 AR S-band receivers for the recovery of HRPT and spacecraft recorder dump signals. The EMR Model 720 programmable bit synchronizer provides bit reconstruction and clock recovery of any of the possible data streams received via the S-band link; the bit synchronizers are either manually or computer programmable and provide lock status to the computer interface.

Three computer interfaces on the ATNAGE provide for concurrent entry of up to three of the high rate MIRP-generated data streams into the computer via DMA.

Each high rate interface consists of a specially designed frame synchronizer, data selector, and buffer. Each frame synchronizer detects the MIRP 60 bit PN sync code running either forward (real time) or backward (spacecraft recorder dump), derandomizes the data (if required) by extracting the PN sequence inserted by the MIRP, alerts the computer whenever lock is acquired or lost, and accepts either 11,090 word or 3,327 word frames as programmed.

The high rate frame synchronizer acquires lock in a three stage process, progressing from SEARCH to CHECK to LOCK. In SEARCH, the synchronizer continuously monitors the data stream for the presence of the 60 bit sync pattern; upon detection of the exact 60 bit sync pattern, the synchronizer advances to the CHECK mode and checks the 60 bit sync in the next frame. If the number of bit disagreements is less than or equal to N, the synchronizer advances to LOCK mode; if the number of bit disagreements exceeds N, the synchronizer returns to SEARCH. In LOCK mode, the synchronizer continues to check the 60 bit sync pattern. If the number of errors exceeds M, the synchronizer increments a bad frame counter; when the bad frame count equals P, the synchronizer returns to SEARCH. If the number of bit errors in LOCK mode does not exceed M, the bad frame counter is reset to zero. N and M are independently computer programmable over the range of 0 to 63; P is programmable over the range of 1 to 7.

In addition, in the LOCK mode, the number of bit errors in the 1000 bit auxiliary sync pattern is counted and entered into the computer each frame. The number of bit errors in each 1000 bit pattern is also compared to a

programmable limit L, and if the limit is exceeded, the frame synchronizer returns immediately to SEARCH mode. L is programmable over the range 0 to 1023.

Upon acquisition of sync, the interface formats the data into either 10 or 16 bit words for computer entry as programmed. The data selector provides the capability to enter only selected portions of a frame into the computer; the selector accepts start and stop locations from the computer I/O for each desired segment of a frame. It is possible to reprogram the selector on the fly during a frame to obtain more than one data segment. Selection of data frames is under software control. An input data buffer is included to permit entry of 100% of consecutive frames. The synchronization status of the frame synchronizer is made available for input to the computer under program control.

One interface in the SAGE provides for the transmission of HRPT data to the GFE AVHRR Display. This interface includes a frame synchronizer having the same characteristics as those used to input data to the computer except that:

a. The frame synchronizer does not check or utilize the 1000-bit auxiliary sync pattern for frame synchronization.

b. All frame synchronization control parameters are manually programmable, and the synchronization status is not input to the computer.

As a test mode, the MIRP can be commanded to continuously generate a 1023 bit PN sequence in place of its regular data outputs. This PN sequence may be used for BER tests on the spacecraft recorders and communication links. Each MIRP interface to the computer includes a means of checking this PN sequence either forward (real-time) or reverse (DUMP) and reporting a periodic count of detected errors to the computer.

An interface is provided for the entry into Computer A of a spacecraft recorder dump of TIP and AIP data. The interface includes an EMR Model 2731 frame synchronizer for the sync pattern received in reverse order and delivers the entire data frame to the computer data channel as 16 bit words. The frame synchronizer also provides lock status to the computer.

The APT subcarrier is demodulated and line sync derived to allow Go/No-Go A-scan monitoring on an oscilloscope. The APT subcarrier is also made available for input to the GFE hard copy display.

The SAGE has the capability to enter digital APT data into Computer A. The data shall be accepted from the spacecraft via hardwired test harness. The data is received as 8 bit parallel words with a word clock at a rate of 4,160 words per second and entered into the computer as 16 bit words. Frame synchronization is accomplished in software.

5.4.3 IRIG CLOCK

The ATNAGE is capable of either generating the IRIG time code or accepting and reading an external modulated code input to generate the clock. The acceptable characteristics of the external modulated code input are as follows in Table 5.4.3-1.

TABLE 5.4.3-1. ATNAGE IRIG TIME CODE INPUT

CHARACTERISTIC	VALUE
Carrier Frequency	30 Hz to 500 kHz
Modulation	IRIG-B Hours, Minutes, Seconds
Amplitude	100 mV to 20 V peak-peak
Modulation Ratio	2:1 to 6:1
Input Impedance	100k ohms or greater
Connector	BNC

5.4.4 GENERAL PURPOSE MEASUREMENTS

The ATNAGE provides the capability to make general measurements under program control of spacecraft test points, SSR internal test points, and test points on external support equipment such as sensor stimulators. The selection and routing of signals to the measurement devices is normally under program control and includes hardware interlocks to preclude connecting more than one signal source to a given point.

The measurement capabilities are as follows in Table 5.4.4-1.

TABLE 5.4.4-1. ATNAGE MEASUREMENT CAPABILITIES (IN DC VOLTAGE)

MEASUREMENT CHARACTERISTICS	CAPABILITIES (*dc voltage)
Range	0.1, 1, 10, 100 V
Accuracy	± (.007% of reading +3 counts) at +23°C, ±5°C on 01 V range
Sensitivity	1 μV or better on 0.1V range

Two-hundred-sixty two-wire (floating) signal input/measurement channels are provided. Fifty of these signals will be copper-constantan wire pairs representing direct connections to temperature sensing thermocouples; the ATNAGE provides for the input and controlled conversion of these signals to copper-copper wire pairs prior to monitoring or measurement device inputs.

Twenty thermocouple monitoring inputs will be allocated for general spacecraft temperature monitoring; the 40 remaining environmental sensor inputs are available for instrument STE temperature or status monitoring.

5.4.5 DCS/SARP-2 SPECIAL TEST EQUIPMENT (DCS/SARP-2 STE)

The DCS/SARP STE provides test messages to the DCS and SARP-2 equipment on the spacecraft under manual or ATNAGE control. This equipment is GFE.

5.4.6 SARR SPECIAL TEST EQUIPMENT (SARR STE)

The SARR is GFE and is capable of operating in a local mode or under the control of the ATNAGE. The testing of the SARR is under control of software in the SARR STE; the ATNAGE acts as a scheduler.

5.5 FRAME SYNCHRONIZERS

The frame synchronizers provide serial PCM baseband data for input to the ATNAGE computers. Two types of frame synchronizers are provided: a GE frame synchronizer processes GAC, LAC, and HRPT data; an EMR frame synchronizer processes TIP data.

5.5.1 GE FRAME SYNCHRONIZERS

The GE frame synchronizers operate as described in Paragraph 5.4.2.3.2. They provide the following standard functions:

- Accept TTL NRZ-L serial data as well as 0- and 90-degree clock signals from bit synchronizers.

- Detect and frame synchronize to following selectable formats and rates:

  - GAC (2.6616 or 1.3308 Mbps) in forward or reverse format
  - LAC (2.6616 or 1.3308 Mbps) in forward or reverse format
  - HRPT (0.6654 Mbps) in forward format

- Provide either 10-bit or 16-bit parallel TTL NRZ-L word output, plus word and frame clocks.

- Count bit errors in last 1,000 bits of each frame, and provide this information as a four-bit output.

- Provide status outputs.

5.5.2 EMR FRAME SYNCHRONIZERS

EMR Model 2731 frame synchronizers are purchased units that provide the following functions:

- Accept TTL NRZ-L serial data as well as 0- and 90-degree clock signals from bit synchronizers.

- Detect and frame synchronize to the following selectable formats and rates:

  - Real time TIP (8.32 or 16.64 kbps) in forward format.
  - Playback TIP (0.3327 Mbps) in forward or reverse format.
  - Playback AIP (0.3327 Mbps) in reverse format.

- Provide synchronized 16-bit parallel TTL NRZ-L word outputs plus I/O controls to the Data General computer interface.

- Provide status outputs.

- Accept front panel or computer control inputs.

Programming of each unit requires 17 sequential 16-bit words. Each word contains an 8-bit addressing code and an 8-bit instruction code. Items to be programmed include frame length, frame sync length, frame sync pattern, synchronization criteria, and bit slippage window width. (These units can handle data rates from 1 bps to 2 Mbps and frame sync patterns of 4 to 33 bits.)

5.6.1 ATNAGE SYSTEM OVERVIEW

The ATNAGE is an Aerospace Ground Equipment (AGE) test system designed to support testing of the ATN-KLM spacecraft during integration and pre-launch activities.

During such a test, the ATNAGE system sends commands to the spacecraft and monitors the status of the on-board hardware and software systems by processing the telemetry and the high-rate data streams, and displaying, printing and/or strip-charting the results in real time. In addition, some raw as well as processed data is stored in the on-line disk storage and/or tapes for subsequent non-real-time analysis.

An automated test procedure controls the system with minimal operator supervision. CRT/keyboard consoles provide operator interaction with the system, and allow manual intervention in the test procedure.

A simulator, which is an integral part of ATNAGE, enables the testing of the telemetry and command functions of the ATNAGE in the absence of a spacecraft.

The SAGE hardware system configuration, shown in Figure 5.6.1-1a consists of:

(a) Three Data General corporation MV8000C multiprocessing computers (referred to as A, B and C Computers), each with its own dedicated set of peripherals. Communication between computers A, B and C is accomplished via Multi-Processor Communication Adapter (MCA) units. Each computer is capable of running multiple processes simultaneously.

(b) GE customized data processing hardware

(c) GE customized and government furnished special test equipment and interfaces

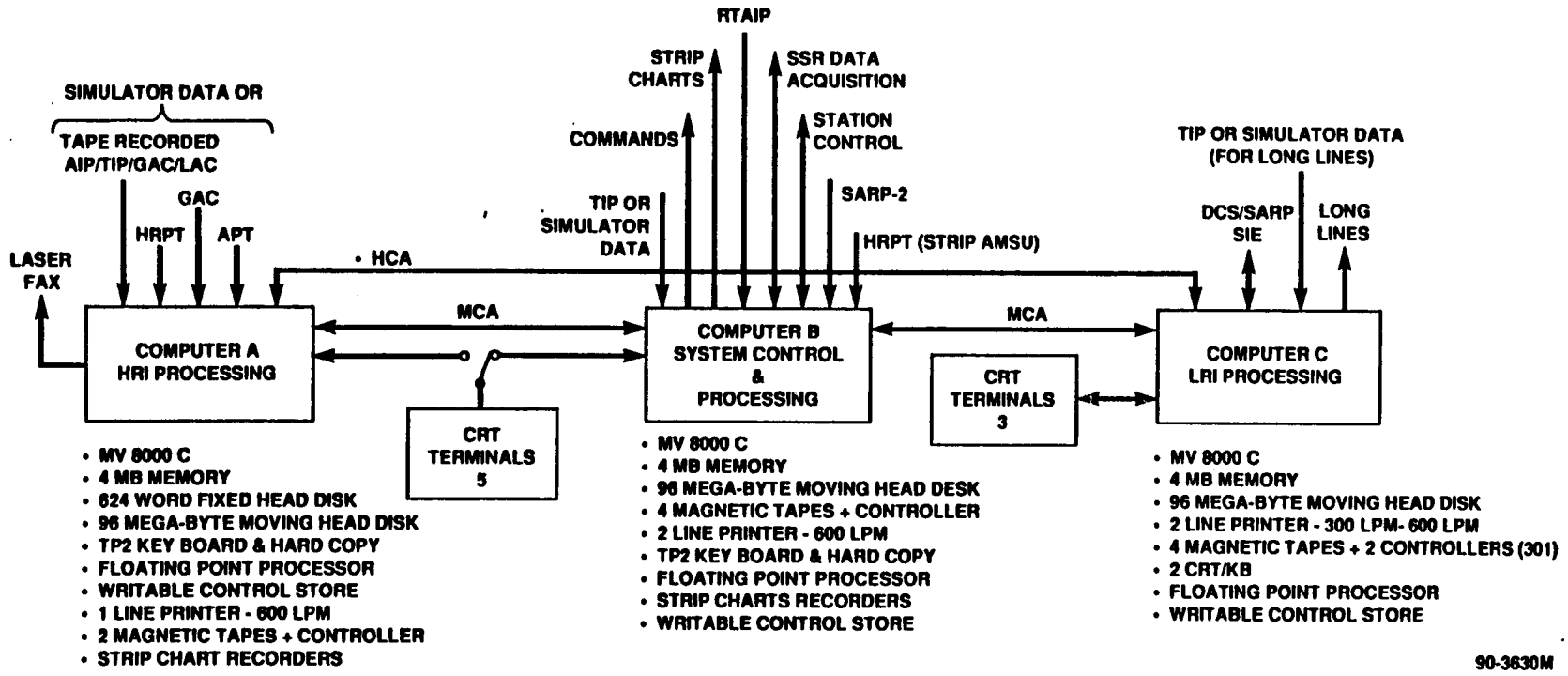

Figure 5.6.1-1a. SAGE Hardware System Configuration

The ATNAGE computer support systems shown in Figure 5.6.1-1b consist of:

(a) Simulator - Consisting of one Data General Corporation MV800C multiprocessing computer with supporting disk storage systems, magnetic tape drives, CRT keyboard terminals and link printers. RF downlink transmitters and pre-modulator filters and modulators are included to support SAGE readiness verification.

(b) Off-line computer - Consisting of one Data General Corporation MV800C multiprocessing computer with supporting disk storage system. Magnetic tape drivers, CRT key board terminal, and line printers. An IBM PC is provided with graphics and long modem capability.

The ATNAGE software is designed to operate under the Advanced Operating System (AOS/VS) which supports a multi-processing environment. The software provides for interprocess, and interprocessor communication; supports shared memory and supports high-level languages such as FORTRAN 7, C and APPLE. The ATNAGE software consists of five subsystems and their corresponding support software. The nominal configuration of these subsystems is as follows:

a. The BUS Subsystem in Computer B
b. The HRI Subsystem in Computer A foreground (real time) and Computer A background (non real-time)
c. The LRI Subsystem in Computer C
d. The Atlas Subsystem in Computer B
e. The ATSIM Subsystem in Simulator Computer

A separate computer is available for ATNAGE off-line software processing and other support functions.

While it is possible to operate ATNAGE in a "reduced" configuration, by not enabling some of the above subsystems, the BUS Subsystem must be active at all times to provide minimal ground support.

The BUS and ATLAS Subsystems are capable of autonomous operation in either Computer A or B. Moreover, the BUS Subsystem can reside in Computer C or the SDC Computer in the non-real time (NRT) mode. In this mode, telemetry data is input through a BUS history tape, and the spacecraft commanding and ATLAS functions are not available.

This overview is concerned solely with the nominal configuration.

The major ATNAGE interfaces with the spacecraft, the ground test equipment and the user are through the BUS Subsystem which acts as an executive to the rest of the system. Real-time operator keyboard inputs are decoded by the BUS and forwarded to the destination subsystem (LRI, HRI or ATLAS) over the MCA lines or interprocess messages. Event messages generated within each subsystem are sent back to the BUS for formatting and eventual dispatch to their destination printer.

The BUS Subsystem builds and sends commands and OBP memory load data to the spacecraft through S-band command uplink. It initiates service requests to the Spacecraft Support Racks (SSR) through the Data Acquisition System (DAS) interface to control and monitor the environmental and special test instrumentation.

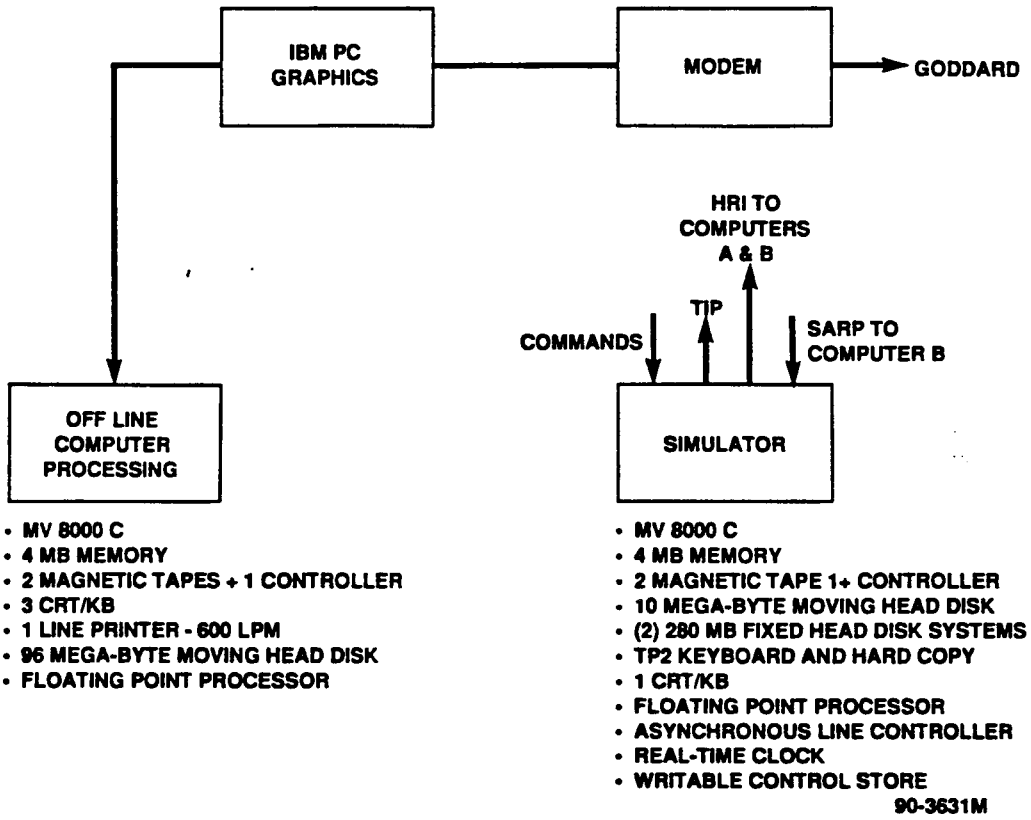

Figure 5.6.1-1b. ATNAGE Computer Support Hardware System Configuration

The ATLAS Subsystem, when running in conjunction with the BUS, acts as a second-order executive; i.e., it automates the scheduling of operator (OPR) commands, spacecraft commands and DAS requests by executing pre-compiled ATLAS test procedures containing the above. The station control interface software resident in the ATLAS Subsystem will allow the user to configure and/or monitor all of the ground station test equipment and data paths via these ATLAS procedures. ATLAS communicates with the BUS through interprocess messages on Computer B. While the execution of the ATLAS procedure is largely automatic once it is started by the BUS, provisions have been made for operator intervention by means of the keyboard input (from the BUS) or push button switches on the ATLAS Test Panel (ATP).

TIP telemetry data from the spacecraft is available to the ATNAGE from one of three sources: TIP stream, AIP stream, and HRPT data stream. The selection of which source to be used is under the control of the test operator. Data originating from the spacecraft or the simulator is bit and frame synchronized and input into the BUS Subsystem where it is monitored, validated and decommutated into an in-core data store named the Functional (FUN) file.

TIP data contains housekeeping information and data from the following low-rate instruments:

a. Space Environment Monitor (SEM)
b. Data Collection System (DCS)
c. High Resolution Infrared Radiometer Sensor (HIRS/2I)
d. Solar Backscatter Ultraviolet instrument (SBUV/2)

AIP data contains TIP data, AMSU-A2 and AMSU-B data. This data stream originates from the spacecraft or the simulator is bit and frame synchronized and input into the BUS subsystem where it is validated and separated into its components for monitoring and decommutation into the FUN file.

If HRPT is the source of data selected, the AMSU-A1, AMSU-A2, AMSU-B and TIP data is pulled from the HRPT stream and used as the source of data processing.

Other information stored into the FUN file by the BUS include:

a. The Search and Rescue Processor (SARP-2) data From the SARP-2 test point or from the SARR STE

b. The Advanced Very High Resolution Radiometer (AVHRR/2) data extracted by the HRI Subsystem on Computer A and sent to the BUS over the MCS interface

c. The responses to DAS service requests

The BUS saves on a history tape the TIP or AIP, AVHRR/2, SARP-2 and DAS data. Other outputs of the BUS Subsystem include the CRT displays, hard copy snapshots of CRT displays, strip-chart recordings and various printer outputs.

The SARP-2, AVHRR/2 and low-rate instrument (LRI) data are sent over an MCA line to the LRI subsystem every second for further processing.

The HRI subsystem on Computer A can simultaneously process in real time, up to three of the high-rate data streams input to Computer A through three different DMA interfaces. These are:

a. High Resolution Picture Transmission (HRPT) data

b. Global Area Coverage (GAC) data or Automatic Picture Transmission (APT)

c. Tape Recorder playback for Global Area coverage (GAC), Telemetry Information Processor (TIP) or Local Area Coverage (LAC) data AMSU information processor (AIP)

The FG program monitors and stores the above HRI data, under direct control of the BUS Subsystem. The BG program uses the stored HRI data for analysis in non-real time. The two programs communicate with each other through the FG/BG interface. Moreover, the BG program communicates with the LRI Subsystem to generate a special TIP data tape on Computer C from the high-rate data streams received on Computer A. This tape is used for offline comparison ("TIP Compare Process") with the TIP data recorded on the BUS history tape.

The HRI Subsystem sends to the BUS the event messages generated on Computer A, the data files to be printed, the AVHRR/2 data to be stored in the FUN file and recorded on history tape, and the status information to be displayed. It has a 'LASERFAX' interface to generate hard copy printouts of HRPT data.

The LRI Subsystem processes the AVHRR/2 and low-rate instrument data received from the BUS according to the latest OPR commands received from the latter. It has additional interfaces with the DCS/SARP STE's to control and monitor the test equipment. Its outputs are in the form of instrument and calibration tapes, formatted prints, event messages, status data and updates to the FUN file. The last three data types are sent over the MCA link to the BUS Subsystem for displaying, logging and/or hardcopy prints.

The ATSIM Subsystem is a telemetry and command simulator which accepts and responds to spacecraft commands sent by the BUS in the absence of a spacecraft. It is capable of generating programmable-format GAC, HRPT, APT, TIP, AIP and SARP-2 data. It can read low-rate instrument data off a history tape generated by the BUS, and play it back through the telemetry stream for a more "dynamic" simulation of LRI data. Interfaces with the other subsystems are functionally and electrically similar to those of the spacecraft. ATSIM has its own executive, i.e., it accepts operator commands from its own keyboard and/or schedule files and generates its own displays, independent of the rest of the ATNAGE system.

5.7 ATNAGE SUBSYSTEMS

5.7.1 HRI SUBSYSTEM

As in the NAGE, the HRI Subsystem is contained in computer A of the ATNAGE system (see Figure 5.7.1-1). Computer A is a DG MV8000/C computer operating under the DG RDOS 7.2 Operating System. Software for the HRI consists of

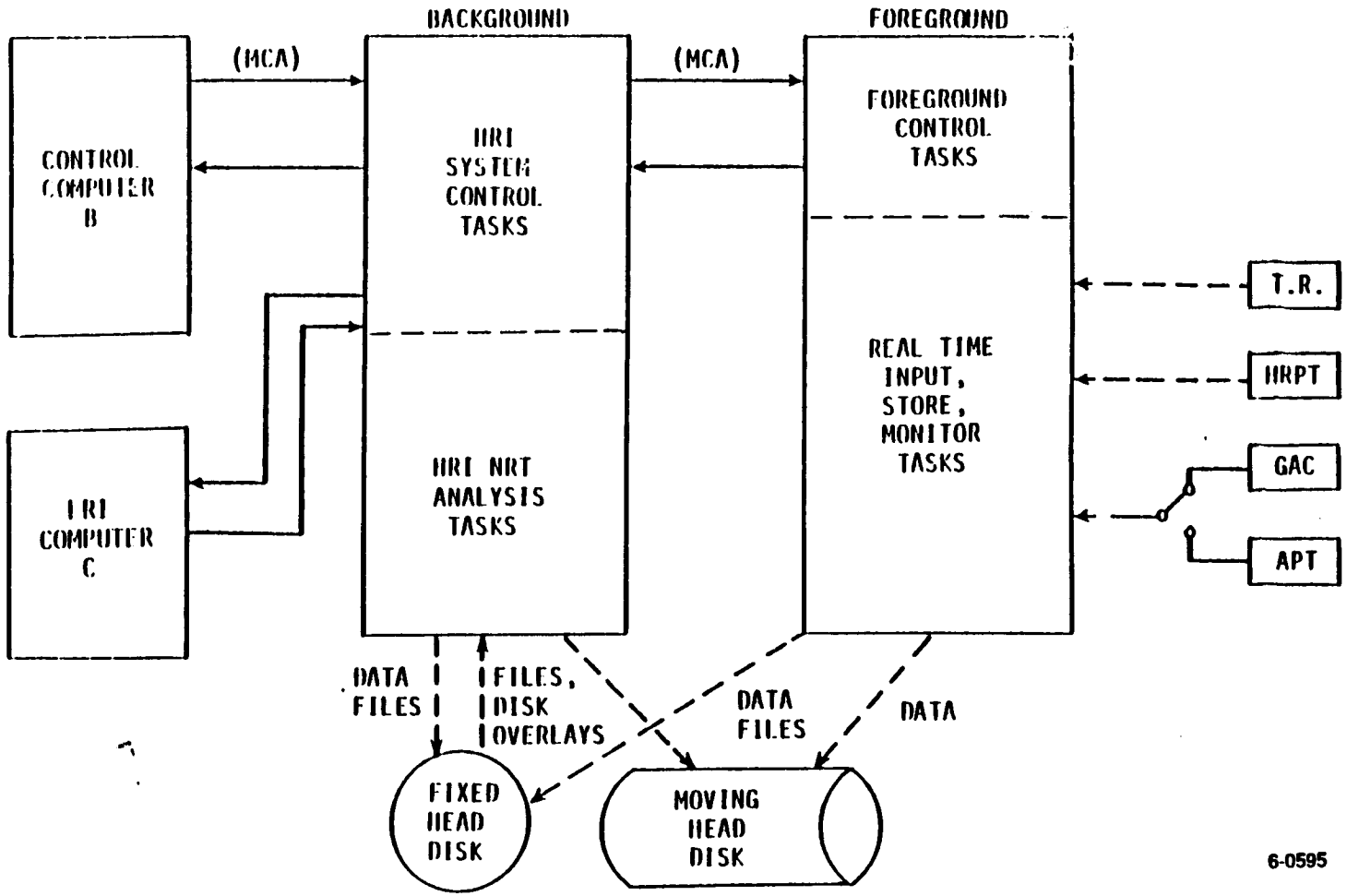

Figure 5.7.1-1. HRI Subsystem Organization

APPLE, FORTRAN 5 and Assembly Language processing routines and RDOS utility routines.

High rate instrument data is received by Computer A in four distinct data streams:

(a) High Resolution Picture Transmission (HRPT) full resolution digital video data from the Advanced Very High Resolution Radiometer (AVHRR/2) with frames of data from the TIROS Information Processor (TIP) inserted.

(b) Global Area Coverage (GAC), compressed AVHRR/2 digital video data with embedded frames of TIP data.

(c) Automatic Picture Transmission (APT), digital video data from the AVHRR/2, averaged in a scan position way so as to correct for the geometric distortion caused by the curvature of the earth.

(d) Spacecraft Tape Recorder data, high rate reserve replays of real-time Local Area Coverage (LAC), GAC, TIP, and AIP data.

Computer A processing of these data streams consists of real time monitoring of the non-video portion of these data streams and on-line disk storage of large samples of these data. In addition, non-real time analysis functions are performed for each data stream.

All operation of the HRI is controlled via OPR commands (executive messages) from Computer B over the Multi-processor Communications Adapter (MCA). These messages control:

a. which input data streams to process
b. the extent of real time monitoring to be performed
c. the amount of data input to on-line disk storage
d. the non-real time data analysis functions performed
e. The HRI system support functions performed in the BG.

The software for the processing of the HRI is structured such that all real time processing functions are performed in the Foreground of computer A, and the non-real time functions are performed in the Background of the computer. In addition to non-real time processing, the BG also controls the execution of the overall system. The HRI subsystem's FG and BG programs are two separately loaded programs executing as a single system, communicating through a MCA link between the two grounds and through a 256-word common communication area in each ground.

The subsystem configuration is as shown in Figure 5.7.1-1. The moving head disc (DZØ) is used strictly for data storage, while all operation is from the fixed head disc (DKØ). This configuration must be adhered to in order for the HRI software to operate properly.

The Moving Head disc has give continuous files called RTDATA1, RTDATA2, RTDATA3, RTDATA4 and RTDATA5, each file being 29279 blocks long and set up so that each file starts on the first block of a cylinder, and each file is contiguous to the others.

The HRI software runs from the Fixed Head Disc (DKØ). This disc contains the following files necessary for operation of the HRI software:

a. Operating System

SYSH.SV	- Save File
SYSH.OL	- OVERLAY File
SYSHSG	- SYSGEN Dialogue
SYSHLS	- Operating System Load Map

b. HRI Programs

HRI.SV	- Background Save File
HRI.OL	- Background Overlay File
FGP.SV	- Foreground Save File
DATAMON.OL	- Foreground Overlay File
PREBGP.SV	- Background Data Base Generator
TGEN.SV	- Foreground Data Base Generator
START	- System Startup Indirect File

c. Contiguous File

See Table 5.7.1-1.

TABLE 5.7.1-1. DKØ CONTIGUOUS FILES

Filename	Size (Blocks)	Description
DISKINDX	11	Disk Index File
FNAMINDX	4	Filename Index File
INDEX	4	(Linked to FNAMINDX)
EXTRACT	1	Extracted Data File
BERFIL	101	Bit Error File
FGTBLZ	4	Foreground Tables
BGDATA.BD	4	Background Tables

5.7.1.1 Background Program Description

The software for the BG of the HRI system perform the following functions:

a. Control the overall executive operation of the HRI system.
b. Handle all interfacing with the BUS software in Computer B.
c. Handle the maintenance of the disk storage index tables.
d. Perform HRI status report processing.
e. Perform non-real time HRPT analysis.
f. Perform non-real time GAC analysis.
g. Perform non-real time APT analysis.
h. Perform non-real time tape recorder data analysis.

A detailed description of the HRI background software can be found in the GE Performance Specification PS-2291682.

5.7.1.2 Foreground Program Description

The Foreground software of the HRI system perform the following functions:

a. HRPT data input and real-time data checking

b. GAC data input and real-time data checking

c. APT data input and real-time data checking

d. Tape Recorder data input and real-time data checking

e. Real-time data storage of HRPT, GAC or APT, and Tape Recorder Playback data to disk.

f. Tape Recorder BER checking

g. AVHRR/2 extracted data.

5.7.2 BUS AND SUPPORT

The BUS subsystem receives TIP, AIP, and SARP-2 data, sends DAS requests and processes DAS responses, sends spacecraft commands, controls the operation of the other subsystems, and provides various run time support functions. BUS subsystem functions include: .

a. Checking data validity
b. Formatting the data for storage in the FUN file
c. Limit checking the data
d. Status checking the data
e. Converting raw analog telemetry into engineering units
f. Loading the CPU's
g. Evaluating the CPU dumps
h. Spacecraft command generation and verification
i. Requesting DAS data, and processing responses
j. Gathering and reporting system events
k. Communicating with the A and C computers
l. Interfacing with the ATLAS run time subsystem
m. Outputting to the CRT's, strip charts, data and events printers, and history tape
n. Accepting operator input commands
o. Producing a history tape
p. Running in non-real time from history tape data.

The BUS support subsystem consists of generator and print programs for BUS data base files.

5.7.3 ATLAS AND SUPPORT

5.7.3.1 ATLAS System

The ATLAS Runtime Subsystem executes the interpretive code produced by the ATLAS compiler. It interprets each opcode (operation code) in sequence. (The Runtime Subsystem is designed to handle all the commands as set forth in document CL2291762 THE NAGE ATLAS USERS MANUAL.)

Figure 5.7.3-1 is a block of the RTS. The Runtime Interpreter (RTI) module gets each opcode and then passes control to the appropriate processor. There are four groups of opcode processors:

a. Arithmetic - All arithmetic and logical functions

b. General - Data movement, comparisons, branching, delays, waits, etc.

c. I/O - All input/output, channel, and file operations

d. Device Control - All test system stimuli and measurements.

The Device Control Module communicates with the individual device drivers.

An initialization module starts the system and validates test program entry points.

When the RTI requires a device, it uses a general purpose Device Control Procedure to interface with the individual software device drivers or with the BUS subsystem.

The following four arguments are given to a device driver by the Device Control Procedure:

a. DEVICE CODE (DEVCDE)
b. Action to be Performed (VERB)
c. Parameter Pointer Array (PARAM)
d. Error Return Location.

For a more detailed description of the ATLAS runtime subsystem see "ATLAS Runtime Process Top-Level Design Specification," ATL-ATRT-3282757.

5.7.3.2 ATLAS Support Subsystem

This subsystem consists of the ATLAS compiler and an accompanying equipment definition table. The ATLAS compiler translates ATLAS procedures into interpretive code executed by the runtime system. It is written in C.

The ATLAS compiler consists of a nucleus core resident area plus a separate processor for each type of verb. The nucleus contains routines for lexical analysis, arithmetic expression analysis, symbol table manipulations and virtual address space operations.

The compiler uses two temporary disc files for the symbol table and the test step number table. The test system equipment definitions and the interpretive code itself are also disc resident. Since these files support a large virtual address space, there is no practical limit to table or test program size.

Syntax analysis and code generation are performed by the verb processors.

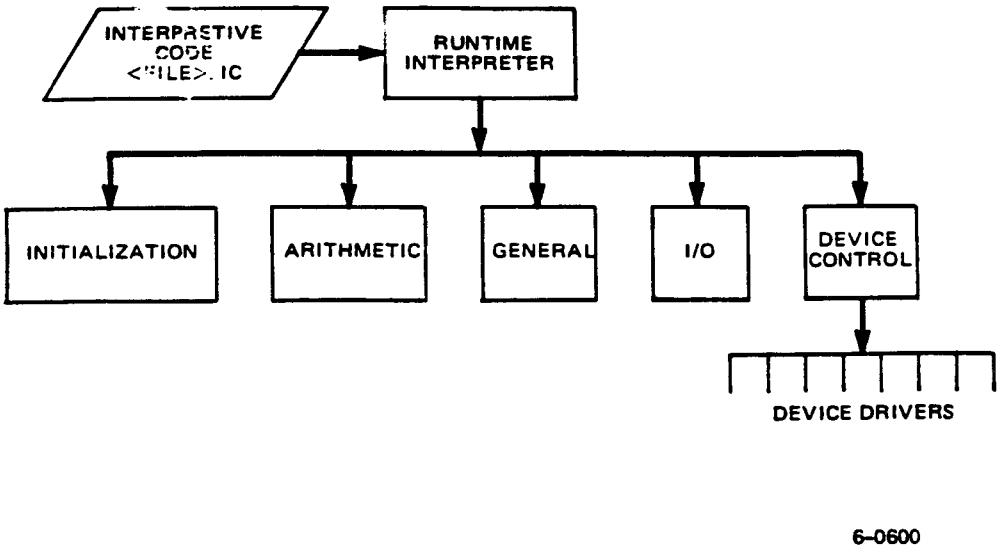

Figure 5.7.3-1. ATLAS Subsystem Organization

For a more detailed description of the ATLAS Compiler subsystem see "ATLAS Compiler Top-Level Design Specification," TL-ATCMP-3282757.

5.7.4 LRI AND SUPPORT SUBSYSTEMS

The LRI and Support Subsystems are comprised of both real time functions in Computer C .

5.7.4.1 Real-Time Low-Rate Instrument Processor

The Computer C low-rate instrument subsystem controls the execution and processing of the Low-Rate Instrument (LRI) data extracted from the spacecraft telemetry.

This consists of the following software processing packages:

a. Advanced Microwave Sounder Unit A1 (AMSU-A1)
b. Advanced Microwave Sounder Unit A2 (AMSU-A2)
c. Advanced Microwave Sounder Unit B (AMSU-B)
d. High Resolution Infrared Sounder 2 (HIRS/2)
e. Space Environment Monitor (SEM)
f. Data Collection System 2 (DCS-2)
g. Search and Rescue Processor 2 (SARP-2)
h. Solar Backscatter Ultra-violet Spectral Radiometer 2 (SBUV/2)
i. Advanced Very High Resolution Radiometer 2 (AVHRR/2)

In addition, a main C computer handler package is supplied with ACT as the executive of Computer C.

The low rate instrument processing software runs in th ATNAGE Computer C. This consists of the following software processes:

1. LRI Main Control Process
2. High Resolution Infrared Sounder (HIRS/2I) process
3. Advanced Microwave Sounder Unit-A1 (AMSU-A1) process
4. Advanced Microwave Sounder Unit-A2 (AMSU-A2) process
5. Advanced Microwave Sounder Unit-B (AMSU-B) process
6. Space Environment Monitor (SEM) process
7. Data Collection System 2 (DCS/2) process
8. Solar Backscatter Infrared Radiometer 2 (SBUV/2) process
9. Advanced Very High Rate Radiometer (AVHRR) process
10. Search and Rescue Processor with Memory 2 (SARPM/2) process

All the LRI software packages operate in Computer C, with data and control supplied by Computer B. The function of each instrument process is described in a separate document.

5.7.4.2 TIP Long Lines

Long lines transmission of TIP data is accomplished in hardware through a GFE supplied CDF rack of equipment and a telephone modem line.

5.7.4.3 DCS/SAP STE

Each NAGE will provide an RS-232 interface with a DCS-2 and a SARP-2 STE. This interface includes control for start and stop of a STE operation. The NAGE to STE interface modules run within the C Computer and accommodate sharing of two STEs.

5.7.4.4 Off-Line (Support) Processing

The off-line analysis program for TIP compare (TIPCOMP) which executes in the background area of Computer C, accepts as input a Computer C CTIP digital magnetic tape generated during real-time operations.

The special support routines for the generation of LRI/BHRI real time instrument software data bases remain as off-line programs.

The specialized off-line programs which require calibration and special instrument digital magnetic tapes generated real time execute in Computer C.

5.7.5 ATSIM AND SUPPORT

The Advanced TIROS-N Simulator (ATSIM) is designed to simulate the telemetry and command functions for the ATN spacecraft, in order to verify the ATNAGE software during the integration and test activities for the previously mentioned missions.

The main functional requirements for ATSIM are:

a. Generate simulated real-time TIP, AIP, SARP-2 and HRI data (HRPT, GAC and APT) to verify the HRI, BUS and LRI subsystems in Computers A, B, and C, respectively.

b. Accept spacecraft commands (stored or real time) originating from the BUS, send command verification and dynamically modify some DIG B TIP data stream and/or the on-board processor models as a result of these commands.

c. Decommutate instrument data (HIRS/2I, AMSU, DCS, SEM, SBUV/2, SARP-2) from history tapes in ATN format, and multiplex it through the TIP and GAC data steams to provide a more meaningful instrument simulation.

d. Allow the user to control and monitor ATSIM functions through a comprehensive set of executive commands, independent of the BUS OPR structure.

ATSIM does not simulate spacecraft dynamics and/or environmental effects, nor does it attempt to emulate the spacecraft hardware and models beyond the level of detail required to test the telemetry and command functions of the ATNAGE.

Due to timing and space considerations, certain options of ATSIM are mutually exclusive. The operator can select one of the following three configurations:

a. Dynamic LRI mode where TIP or AIP data is extracted from a history tape/disk file and inserted into TIP frames. High-rate data generation and OBP processing are not supported in this mode.

b. HRI mode where the HRPT, GAC, or APT data streams are generated, but no dynamic LRI or OBP processing is performed.

c. OBP mode, where OBP load/dumps is supported, but no dynamic LRI or HRI processing is performed.

Moreover, GAC and APT data cannot be generated simultaneously. The other ATSIM capabilities are common to all three configurations.

The ATSIM Subsystem is designed to run under the AOS/VS on a Data General MV8000C minicomputer with its own dedicated peripherals, described in Figures 5.6.1-1a and 5.6.1-1b.

It interfaces with the HRI, BUS, and LRI subsystems through GE customized interfaces described in Sections 5.7.5 through 5.7.7.

A detailed description of the spacecraft simulator software is described in GE ASD Simulator Software System Level Design Specification TL-3274790.

5.8 SUBSYSTEM INTERFACES

5.8.1 HRI/BUS INTERFACE

The HRI subsystem and the BUS communicate through a bi-directional MCA link between the foreground of Computer B (BUS) and the background of Computer A (HRI NRT and control). Computer B sends control and housekeeping messages to Computer A. Computer A sends data files, AVHRR/2 data, status information, error messages and housekeeping messages to Computer B. Comparable modules in the BUS and HRI subsystems handle the sending and receiving of information.

5.8.1.1 Computer B to Computer A

Computer B sends information to Computer A. The ATNAGE sending function from the BUS to the HRI is the same as for the NAGE. The BUS program in Computer B outputs a buffer of up to 258 words to Computer A. This buffer consists of 14-word exe- cutive control and housekeeping messages to the HRI (housekeeping messages are associated with file sending).

A message queue is maintained by the BUS. This queue contains the 14-word executive control and housekeeping messages directed to Computer A (see Figure 5.8.1-1).

5.8.1.2 Computer A to Computer B

Computer A sends information to Computer B. The HRI sending function to Computer B for ATNAGE is the same as for the NAGE.

The HRI sends to Computer B:

a. 14-word housekeeping messages
b. Real-time error messages
c. Extracted data buffers (AVHRR/2 and Status)
d. Disk files (including HRI Disk Directory).

Housekeeping messages are used to manage file sending.

Disk files may be transferred from Computer A to Computer B. The destination file will be an exact copy of source file. The destination file may or may not have the same name as the source file. The following types of files are transferred:

a. NRT analysis print files
b. MIRP data frames (formatted raw data)
c. HRI disk directory.

5.8.2 BUS/LRI INTERFACE

Interaction between the B and C Computers are handled over the MCA device.

The following types of data are transferred from Computer C to Computer B:

a. Housekeeping messages
b. Encoded event messages
c. Computer C status
d. FUN file updates.

The following types of data is transferred from Computer B to Computer C:

a. FUN file data
b. OPR commands and Formatted Event Messages
c. Print files.

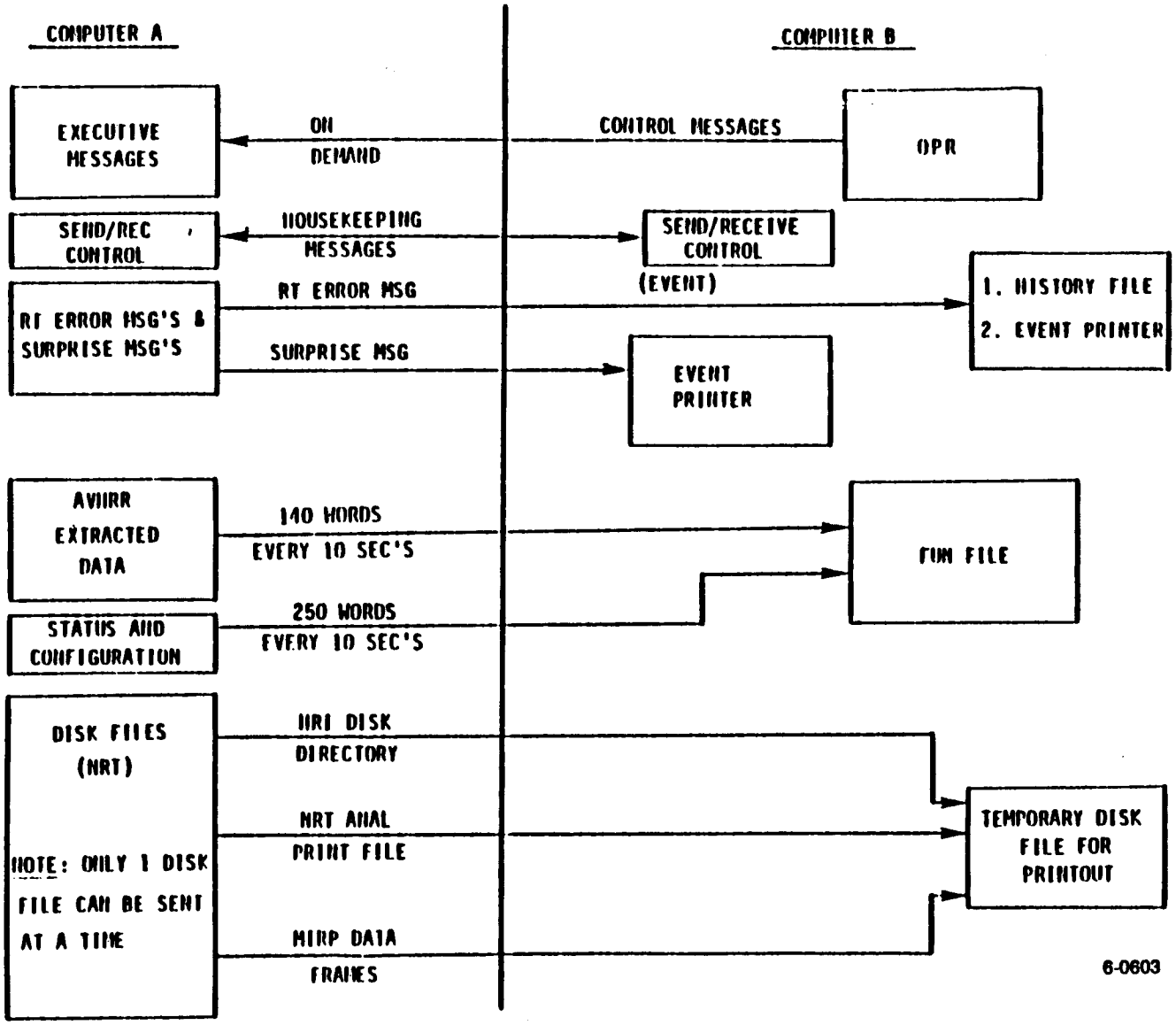

Figure 5.8.1-1. HRI/BUS Interface

5.8.3 HRI/LRI INTERFACE

The HRI/LRI interface is a computer-to-computer interface to support the TIP Compare Process requirements for ATNAGE. TIP data, by command from Computer B, is extracted from previously stored data and sent to Computer C for storage on magnetic tape. Computer A controls the activity.

Start/stop control commands are received from Computer B. Computer A processes these commands and sends housekeeping directives to Computer C accordingly. Messages from C are interpreted by A to continue the data sending or to stop the process.

5.8.4 BUS/ATLAS INTERFACE

ATLAS to BUS (IPC) interfacing is accomplished via standard DC interprocess communication in Computer B. Data request packets are sent from ATLAS to the BUS and data packets returned to ATLAS by the BUS.

5.8.5 ATSIM/BUS INTERFACES

The BUS Subsystem sends spacecraft commands to ATSIM and receives TIP, AIP, HRPT, APT and GAC frames in return. These streams are bit and frame synchronized before being input to the BUS. Table 5.8.5-1 summarizes the data rates and type of I/O for each interface.

5.8.6 ATSIM/HRI INTERFACES

The ATSIM/HRI interfaces are all unidirectional. ATSIM sends HRPT, GAC or APT frames to the HRI. GAC and APT data use the same interface hardware, therefore, they cannot be sent simultaneously. HRPT and GAC data are bit and frame synchronized. Table 5.8.5-1 summarizes the data rates and type of I/O for each interface.

TABLE 5.8.5-1. INPUT/OUTPUT INTERFACE CHARACTERISTICS

Data Type	Input/Output	Type of I/O	Bit Rate (BPS)	Word Length (Bits)	Minor Frame Length (Words)	Minor Frame Rate (MS)	Minor Frame/ Major Frame
HRPT	OUTPUT	DMA SERIAL	665.4 kbs	10	11090	166.67	6
GAC	OUTPUT	DMA SERIAL	66.54 kbs	10	3327	500	1
APT	OUTPUT	DMA PARALLEL	33.28 kbs	8	2080	500	128
TIP OPERATIONAL	OUTPUT	DMA SERIAL	8.32 kbs	16	52	100	320
TIP BOOST	OUTPUT	DMA SERIAL	16.64 kbs	16	52	50	320
DAS	INPUT/OUTPUT	QTY	--	--	--	--	--
COMMANDS	INPUT	SERIAL	40 cps	23	--	--	--
AIP	OUTPUT	SERIAL	16.64 kbs	16	--	--	--