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Specification Number 142068
12 July 1985
(4602B)

INTERFACE SPECIFICATION

SATELLITE DATA HANDLING SYSTEM PRIME ITEM

TO

AUTOMATED DIGITAL FACSIMILE SUBSYSTEM

CONTRACT NUMBER: F04701-79-C-0055

(CDRL 016A2)

SATELLITE DATA HANDLING SYSTEM (SDHS)

APPROVAL/CONCURRENCE

	ORGANIZATION	SIGNATURE	DATE
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INTERFACE CONTROL CONTRACTOR	HARRIS GCSD	[illegible] for CEJones	11/21/85
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH TOLERANCES
2 PLACE ± 3 PLACE ± ANGLES ±

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HARRIS GOVERNMENT SYSTEMS SECTOR
MELBOURNE, FLORIDA 32901

TITLE
SATELLITE DATA HANDLING SYSTEM PRIME ITEY TO AUTOMATED DIGITAL FACSIMILE SUBSYSTEM

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1.0 SCOPE

This Interface Specification (IFS) establishes the performance, design and development requirements for the interface between the Automated Digital Facsimile Subsystem (ADFS) and the Satellite Data Handling System (SDHS).

1.1 Item Description

The Automated Digital Facsimile Subsystem consists of a transmitter terminal and up to six receiver/reproducer terminals. The transmitter terminal consists of a scanner subsystem, data formatting subsystem, communications subsystem, and two computer interfaces.

One computer interface is Univac compatible and shall be disabled by setting a'manual switch; this interface shall not be used by SDHS. The second computer interface shall be 16-bit parallel compatible.

The transmitter terminal generates and transmits high resolution imagery, which is either encoded or nonencoded, to receiver terminal,, and is capable of establishing full duplex voice and teletype communications with each receiver terminal. The ADFS shall provide the capability to select, via the computer interface, the receiver site(s) to which the data is routed and shall provide for automatic synchronization of the transmission modem equipment. Characteristics of the ADFS are shown in Table I.

Table I. ADFS Characteristics

Characteristic	Computer/Transmitter Interface	Transmitter/Receiver Interface	[illegible]
Image Width	NA	NA	[illegible] inches
Image Length	NA	NA	[illegible] inches
Pixels/Inch	Nh	NA	256 128 64
Pixels/Line	3584 1792 896	3584 1792 896	[illegible] [illegible] 3584
Lines/Image	7168 (Max)	7168 (Max)	[illegible] (Max)
Lines/Second	10.2 (Max)	10.2 (Max)	[illegible]
Coding Type	NA	Huffman Differential	NA

Table I. ADFS Characteristics (Continued)

Characteristic	Computer/Transmitter Interface	Transmitter/Receiver Interface	Received copy
Compression	NA	2.5:1 (Avg) 6.0:1 (Max)	NA
Gray Scale	64 Shades 32 Shades 16 Shades	64 Shades 32 Shades 16 Shades	64 Shades 32 Shades 16 Shades
Processing Time	NA	NA	5 Minutes
Terrestrial Line	NA	D1 Conditioned 9600 Bits/Second or 4800 Bits/Second	NA

1.2 Contractors

The interface requirements documented by this IFS have been defined and agreed upon by the following:

Interface Control Contractor	Harris Corporation Government Systems Group
Participating Agency	Air Force Global Weather Central (AFGWC)
Procuring Activity	U.S. Air Force Headquarters (AFSC) Space Division (SD)

2.0 APPLICABLE DOCUMENTS

2.1 Government Documents

None

2.2 Non-Government Documents

Gevelopment Specifications:

HGSG 144198	Prime Item Development Specification for the Satellite Data Handling System (SDHS)

Standards:

EIA Standard RS-422 April 1975	Electrical Characteristics Balanced Voltage Digital Interface Circuits

3.0 INTERFACE REQUIREMENTS

The ADFS interface, illustrated in Figure 1, shall be a 16-bit parallel, input only, asynchronous transfer channel that operates at any rate up to a maximum of 166,700 transfers/second until the ADFS line buffer is filled.

The number of transfers per line shall be a function of the selected resolution. The ADFS receiver always generates copy at the maximum resolution. If a lower resolution is selected, the ADFS display shall perfon pixel and line replication to fill the image space. The relationship between resolution, transfer rate, and number of transfers per line is defined in Table II. Table II specifies the number of transfers which will be processed by the ADFS following the LINE START function code (see Figure 4). Additional transfers which may occur prior to the END OF LINE function code will be discarded by the ADFS.

Table II. Transfer Rate Versus Resolution at 64 Gray Shades and 9600 Baud

Resolution (Pixels/Inch)	Transfers/Line	Encoded Lines/Second Nominal	Encoded Lines/Second Maximum	Nonencoded Lines/Second Maximum
256	1792	1.1	2.7	0.5
128	896	2.2	5.4	0.9
64	448	4.5	10.7	1.8

3.1 Physical Requirements

The ADFS interface, defined to be at Unit 32, J7 as illustrated in Figure 1, is a parallel 16-bit interface. The connector is pictured in Figure 2. The ADFS physical interface is described in Table III. J7 pin assignments are listed in Table IV; in Table IV, the interface is documented from the SDHS point of view in that signals shown as (OUT) are from SDHS to ADFS and signals shown as (IN) are from ADFS to SDHS.

Table III. ADFS Physical Interface

Driver Type:	Advanced Micro Devices P/N 26LS31
Receiver Type:	Advanced Micro Devices P/N 26LS32
Interface Cable Type:	Beldon P/N 9550
Connector:	Winchester Manufacturing P/N MRAC 104PJT06H or MRAC 104P-J6-436
Backshell:	P/N XMRA104-1000
Pins:	100-1024P

NOTE: Equivalent parts of other manufacturers may be substituted

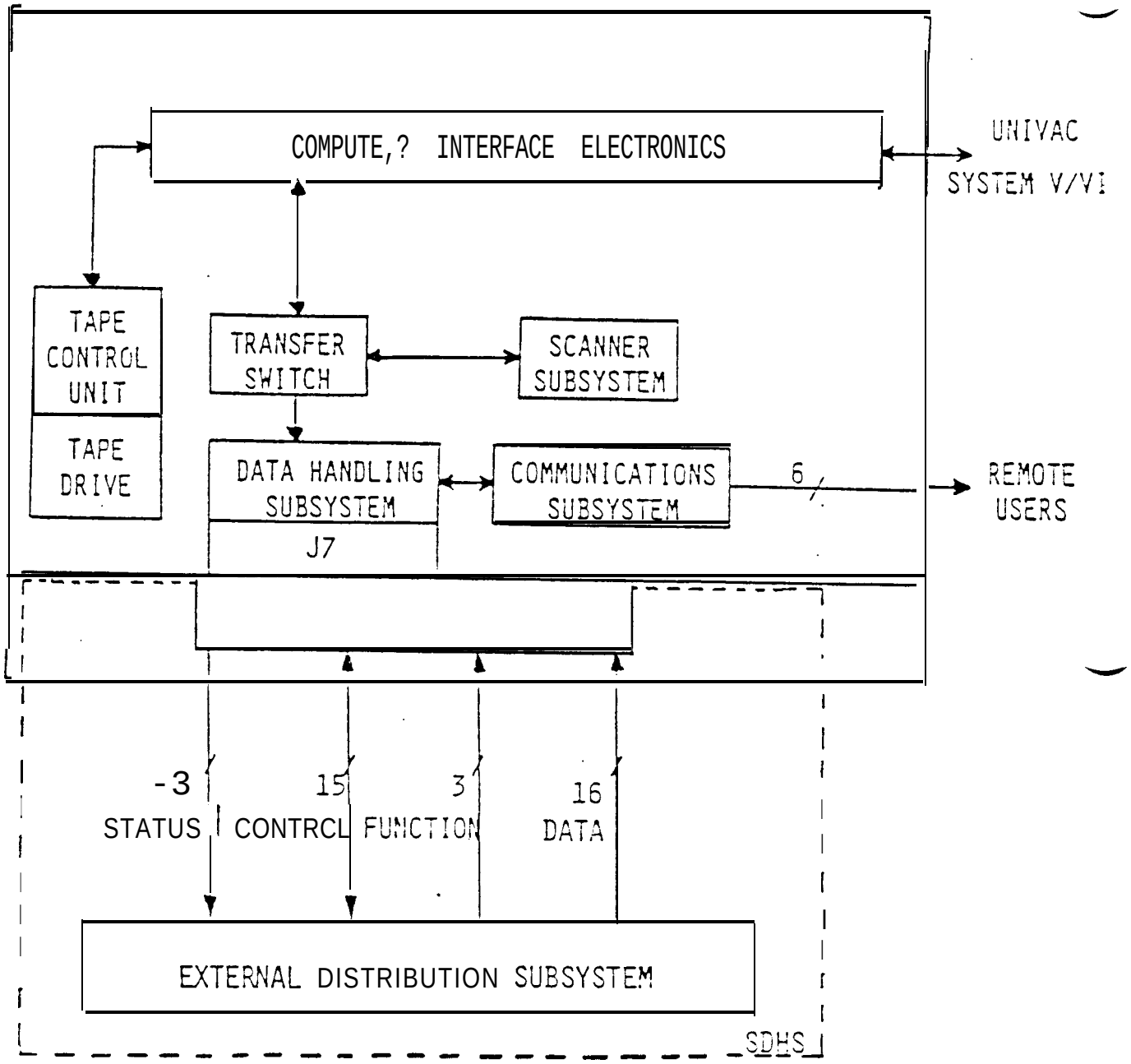


Figure 1. Automated Digital Facsimile Subsystem (ADFS) Interface

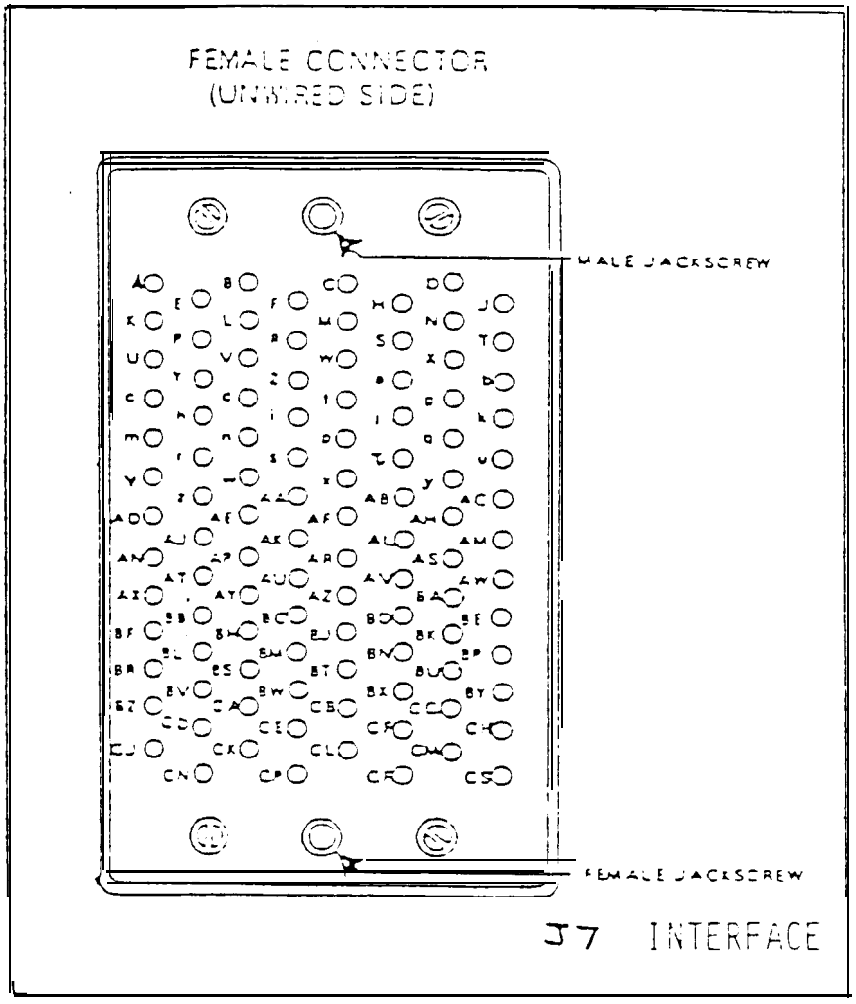


Figure 2. 104 Contact Connector

Table IV. Interface Cable Pin Out

Pin	Signal		Pin	Signal	
A	ODAT (OUT)	00 (+)	AF	C1 CONTROL (IN)	(+)
E	ODAT (OUT)	00 (-)	AL	C1 CONTROL (IN)	(-)
B	ODAT (OUT)	01 (+)	AH	A00 (IN)	(+)
F	ODAT (OUT)	01 (-)	AM	A00 (IN)	(-)
C	ODAT (OUT)	02 (+)	AN	ATTN (IN)	(+)
H	ODAT (OUT)	02 (-)	AT	ATTN (IN)	(-)
D	ODAT (OUT)	03 (+)	AP	BA INC ENB (IN)	(+)
J	ODAT (OUT)	03 (-)	AU	BA INC ENB (IN)	(-)
K	ODAT (OUT)	04 (+)	AR	BUSY (OUT)	(+)
P	ODAT (OUT)	04 (-)	AV	BUSY (OUT)	(-)
L	ODAT (OUT)	05 (+)	AS	STATUS A (IN)	(+)
R	ODAT (OUT)	05 (-)	AW	STATUS A (IN)	(-)
M	ODAT (OUT)	06 (+)	AX	STATUS B (IN)	(+)
S	ODAT (OUT)	06 (-)	BB	STATUS B (IN)	(-)
N	ODAT (OUT)	07 (+)	AY	STATUS C (IN)	(+)
T	ODAT (OUT)	07 (-)	BC	STATUS C (IN)	(-)
U	ODAT (OUT)	08 (+)	AZ	BURST RQL (IN)	(+)
Y	ODAT (OUT)	08 (-)	BD	BURST RCL (IN)	(-)
V	ODAT (OUT)	09 (+)	BA	GO (OUT)'	(+)
Z	ODAT (OUT)	09 (-)	BE	GO (OUT)	(-)
W	ODAT OUT)	10 (+)	BF	CYCLE REQ A (IN)	(+)
a	ODAT OUT)	10 (-)	BL	CYCLE REQ A (IN)	(-)
X	ODAT (OUT)	11 (+)	BH	NOT USED	
b	ODAT (OUT)	11 (-)	BM	NOT USED	
c	ODAT (OUT)	12 (+)	BJ	NOT USED	
h	ODAT (OUT)	12 (-)	BN	NOT USED	
d	ODAT (OUT)	13 (+)	BK	NOT USED	
i	ODAT (OUT)	13 (-)	BP	NOT USED	
f	ODAT (OUT)	14 (+)	BR	NOT USED	
j	ODAT (OUT)	14 (-)	BV	NO? USED	
g	ODAT (OUT)	15 (+)	BS	NOT USED	
k	ODAT (OUT)	15 (-)	BW	NOT USED	
m	INIT (OUT)		BT	NOT USED	
r	INIT (OUT)	I';	BX	NOT USED	
n	WC INC ENB (IN)	(+)	BU	NOT USED	
s	WC INC ENB (IN)	(-)	BY	NOT USED	
p	READY (OUT)	(+)	BZ	NOT USED	
t	READY (OUT)	(-)	CD	NOT USED	
q	NO LOCK	(+)	CA	NOT USED	
u	NO LOCK	(-)	CE	NOT USED	
v	FUNCTION 1 (OUT)	(+)	CB	NOT USED	
z	FUNCTION 1 (OUT)	(-)	CF	NOT USED	
w	FUNCTION 2 (OUT)	(+)	cc	NOT USED	
AA	FUNCTION 2 (OUT)	(-)	CH	NOT USED	
x	FUNCTION 3 (OUT)	(+)	CJ	NOT USED	
AB	FUNCTION 3 (OUT)	(-)	CN	NOT USED	
y	CYCLE REQ B (IN)	(+)	CK	NOT USED	
AC	CYCLE REQ B (IN)	(-)	CP	NOT USED	

Table IV. Interface Cable Pin Out (Continued)

Pin	Signal	Pin	Signal
AD	END CYCLE (OUT) (+)	CL	NOT USED
AJ	END CYCLE (OUT) (-)	CR	NOT USED
AE	CO CONTROL (IN) (+)	CM	NOT USED
AK	CO CONTROL (IN) (-)	cs	NOT USED

3.2 Functional Requirements

3.2.1 Electronic Requirements

The electronic interface requirements for the ADFS interface shall conform to the EIA RS-422 standard. A single balanced voltage interface circuit is illustrated in Figure 3. The circuit consists of three parts: the generator, the balanced interconnecting cable, and the load. The load is comprised of a receiver and a termination resistor.

3.2.1.1 Interchange Voltages

The interface shall be driven by a low impedance (100 ohms or less), balanced voltage source that shall produce a differential voltage in the range of 2 to 6 volts. The signaling sense of the voltages appearing across the interconnection cable are defined as follows:

1. The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 (MARK or OFF) state.

2. The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 (SPACE or ON) state.

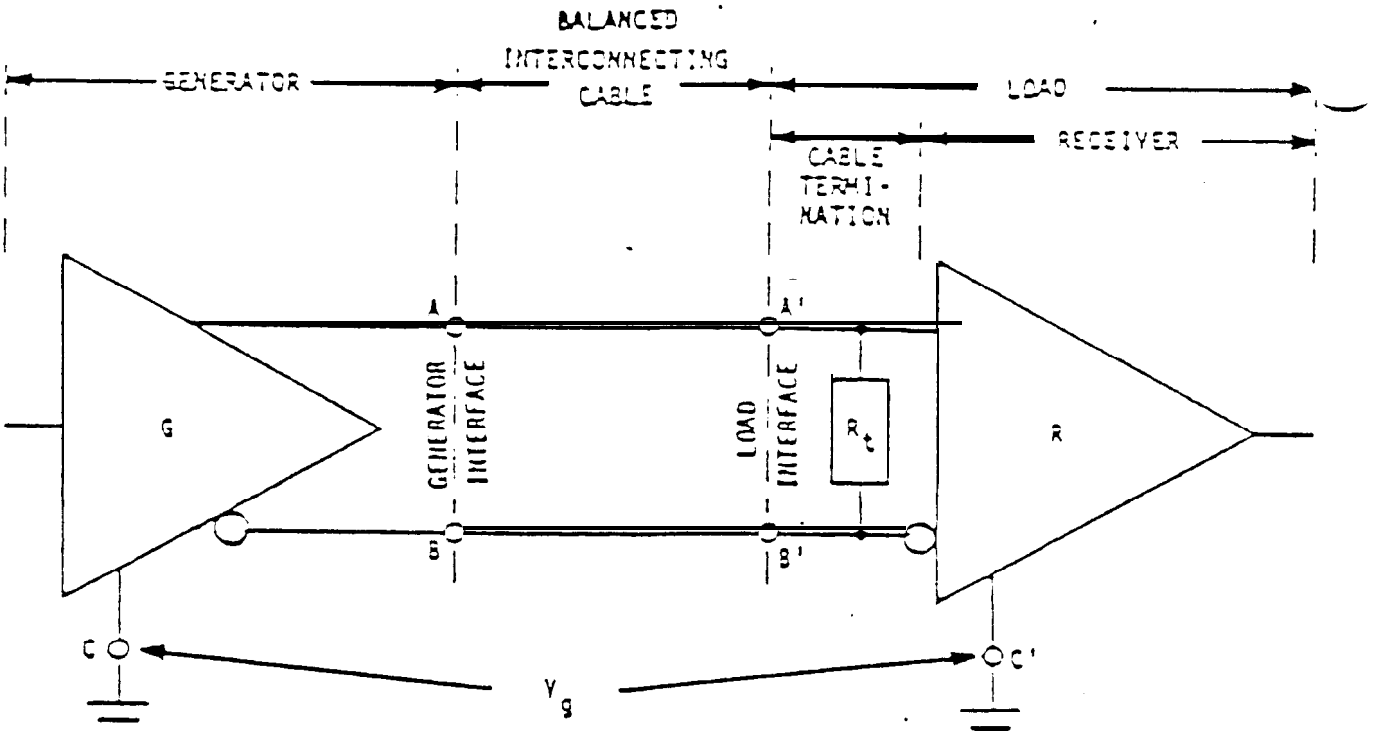
3.2.1.2 Load Characteristics

The electrical characteristics of the receiver shall meet the requirements specified in EIA RS-322. A circuit meeting these requirements results in a differential receiver having a high input impedance (greater than 4K ohms), a small input threshold transition region between -0.2 and +0.2 volts, and allowance for an internal bias voltage not to exceed 3 volts.

The termination resistor (R_t in Figure 3) shall have an impedance of 120 ohms ($\pm$10%).

3.2.1.3 Total Load Characteristic Limits

The total load including termination shall have a resistance greater than 90 ohms between its input points (A' and B', Figure 3) and shall not require a differential input voltage of more than 200 millivolts for the receiver to assume the intended binary state.



Legend:

R_t	=	Cable Termination Resistance
V_g	=	Ground Potential Difference
A,B	=	Generator Interface Points
A',B'	=	Load Interface Points
C	=	Generator Circuit Ground
C'	=	Load Circuit Ground

Figure 3. Balanced **Digital Interface Circuit**

3.2.1.4 Circuit Protection

Balanced voltage digital interface generator and receiver devices, under either the power-on or power-off condition, shall not be damaged under the following conditions:

a. Generator open circuit.

b. Short-circuit across the balanced interconnecting cable.

c. Short-circuit to any other lead using electrical characteristics complying with RS-422 Standards.

d. Short circuit to ground.

3.2.1.5 Signal Definitions

The interface signals specified in Table IV are defined in Table V.

Table V. Interface Signals Definition

Signal	Symbol	Quantity	Definition
Status	STATUS A - C (IN)	3	Computer interface status from ADFS (see Figure 6)
CC Control	CO CONTROL (IN)	1	Used to select byte or word oriented operations; shall be grounded ADFS operation to select word mode
Cl Control	Cl CONTROL (IN)	1	Used to select input or output operation from the computer interface; high equals input operation and iow equals output operation; for ADFS operation, shall be held low
Cycle Request	CYCLE REQ A (IN)		A positive pulse from ADFS requesting bus cycle from the-computer
Cycle Request	CYCLE REQ B (IN)		A positive pulse from ADFS requesting bus cycle from the computer; for ADFS operation, shall be held low
Word Count Increment Enable	WC INC ENB (IN)		In the high state, permits counting of each computer bus cycle; for ADFS operation, shall be held in the high state

Table V. Interface Signals Definition (Continued)

Signal	Symbol	Quantity	Definition
Bus Address Increment Enable	BA INC ENB (IN)	1	In the high state, permits computer bus address register to increment following each bus cycle; for ADFS operation, shall be held in the high state
Bus Address Bit 00	A00 (IN	1	In the low state, allows sequential word addressing; for ADFS operation, shall be held low
Burst Mode	BURST RQL (IN)	1	In the high state, the computer bus is released after each cycle permitting interleaved operation with other devices; for ADFS operation, shall be held in the high state
Attention	ATTN IN)	1	High level causes interrupt if the Interrupt Enable (IE) bit in the computer interface command status register is set; for ADFS operation, ATTN shall be used to notify the computer that ADFS has status data available
output	ODAT 00 - 15 (OUT)	16	Data or control information to ADFS (see Figures 5 and 7)
Initialize	INIT (OUT)	1	Computer interface initialize signal to ADFS
Function	FUNCTION 1 - 3 (OUT)	3	Computer interface function command to ADFS (see Figure 6)
Ready	READY (OUT)	1	Computer interface is ready to transfer data to ADFS
Busy	BUSY (OUT)	1	Indicates computer bus cycle in progress to ADFS; ADFS uses trailing edge to strobe data
End Cycle	END CYCLE (OUT)	1	A positive pulse to indicate current computer bus cycle is complete; not used by ADFS
Go	GO (OUT)	1	A positive pulse indicating the start of a new function to ADFS
No Lock	NO LOCK	1	Not used on DR11-W card

3.2.4.2 **Protocol**

Image transfers to the ADFS shall be line oriented, painting the product from left to right and from top to bottom. Each image transfer shall be initiated and controlled by Control words identified by their Function Code. (See Figure 5.) First a RESET shall clear the ADFS logic, then two CAL control words shall specify gray scale resolution, box start/stop, and data routing; these parameters shall be constant throughout the image. Each image line shall be prefaced by LINE START. Each line shall be terminated by END OF LINE. The image shall be terminated by END OF RUN until completion of processing time when ATTENTION will be asserted accompanied by an AVAILABLE status (see Figure 6). NOT READY shall be returned in response to END OF RUN. If an image is not terminated after 7168 lines (at 256 LPI), the ADFS receiver will automaticall, cut and process the image. Data past 7168 lines will be lost.

If an image transfer is initiated before the ADFS has completed processing the previous image, a NOT READY status (see Figure 6) will be returned

For ADFS operation, Box Start shall be set to 18 anu Box Stop to 78 for full width image reproduction.

ADFS routing control bits shall select receiver site(s) by setting the necessary bit(s) for the selected site(s).

The computer interface FUNCTION bits (Figure 6) shall identify the data content being transferred across the interface as Control or Data words

3.2.5 **Hardware/Software**

3.2.5.1 **Interface Block Diasram**

The interface block diagram is illustrated in Figure 1

3.2.5.2 **Timing and Sequencing**

The timing and sequencing shall be as specified in Paragraphs 3.2.1 and 3.2.4.

3.2.5.3 **Storage Allocation**

Storage allocation will be specified in the appropriate SDHS CPCI product specifications.

3.3 **Environmental Requirements**

The environmental requirements shall be in accordance with the requirements specified in the Satellite Data Handling System Configuration Item Specification.

3.4 Safety

The safety requirements are specified in the Satellite Data Handling System Configuration Item Specification.

4.0 QUALITY ASSURANCE

The interface requirements of this IFS shall be verified in accordance with the verification requirements specified by the CI or CPCI referencing this IFS.

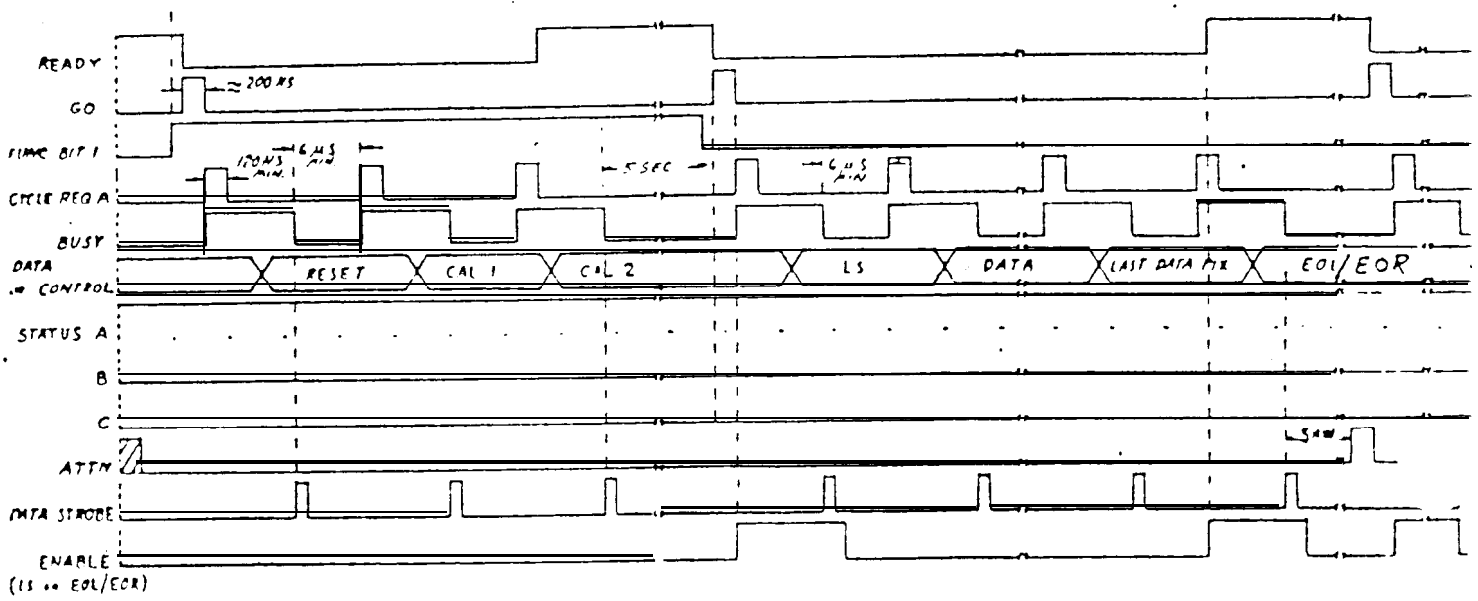


Figure 4. Timing Diagram - Data and Control

3.2.4 Formats and Protocol

3.2.4.1 Formats

The formats for control words are defined in Figure 5. The normal image line is divided into seven 2 inch segments enabling the painting of any width image from 2 to 14 inches by selecting box start and stop codes from 18 to 7_8. The function and status formats are defined in Figure 6. The data format is defined in Figure 7. The ADFS shall always generate copy with 256 pixel/inch -density. If a lower resolution is selected, the ADFS performs pixel and line replication.

If less than 64 gray shades are selected, the 4- or S-bit pixels must be right-justified (aligned with the lower order bits) of each pixel field of Figure 7. The ADFS shall produce clear (white) for pixel values equal to zero (all zeros: 00... 0) and increase in density for increasing binary count. The maximum binary value (all one's: 11...1) shall produce maximum density (black‘:.

The ADFS status format is defined in Table VI.

Table VI. ADFS Status Definition

Status	Word	Definition
NOT READY	000	The internally generated delay that provides time for the receiver to process film has not expired
AVAILABLE	001	Normal status response
OFF LINE	111	DFS is not in Automatic DFS Mode or power is off

The ADFS function format is defined in Table VII.

Table VII. ADFS Function Definition

Function	Word	Definition
DATA WORD	000	Data word (pixel) transfer to ADFS
CONTROL WORD	001	Control word transfer to ADFS

ADFS CONTROL WORD

15 — 3	2 — 0
CALIBRATION DATA	FUNCTION CODE

000 = RESET
001 = LINE START
-010 = END OF LINE
011 = END OF RUN

100 = CAL WORD #1
101 = CAL WORD #2
110 = NOT USED
111 = NOT USED

CALIBRATION DATA FOR CAL WORD #1

15 — 13	11 — 10	8 — 7	5 — 4	3
00	BOX STOP	BOX START	RESOLTUION	QUANTIZATION

111 = BOX STOP

001 = BOX START

00 = 64 GRAY SHADES
01 = 32 GRAY SHADES
10 = 16 GRAY SHADES
11 = NOT USED

000 = 64 LPI
001 = 128 LPI
010 = 256 LPI
011 = NOT USED
100 = NOT USED
101 = NOT USED
110 = NOT USED
111 = NOT USED

CALIBRATION DATA FOR CAL WORD #2

15 — 9	8 — 3
NOT USED	ADFS ROUTING

2^8	2^7	2^6	2^5	2^4	2^3		
X	X	X	X		X1	=	PENTAGON
X	X	X	X	1	X	=	LANGLEY
x	x	x	1	x	x	=	OFFUTT
x	X1	x	x	x		=	SPARE #2
X1	x	x	x	x		=	SPARE #3
1	X	X	X	X	X	=	SPARE #4

Figure 5. ADFS Control Formats

FUNCTION		STATUS	
3 2 1		C B A	
000 = DATA WORD	100 = NOT USED	000 = NOT READY	100 = NOT USED
001 = CONTROL WORD	101 = NOT USED	001 = AYAILABLE	101 = NOT USED
010 = NOT USED	110 = NOT USED	010 = NOT USED	110 = NOT USED
011 = NOT USED	111 = NOT USED	011 = NOT USED	111 = OFF LINE

Figure 6. ADFS Function and Status Formats

15 14 13	8 7	6 5	0
00 PIXEL N	00	PIXEL N + 1	

Figure 7. ADFS Data Word Format